

REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED			
A	Technical changes to table I. Editorial changes throughout.										92-10-27					M.L. Poelking			
<p>THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.</p>																			
REV																			
SHEET																			
REV	A	A	A	A															
SHEET	15	16	17	18															
REV STATUS OF SHEETS				REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Ray Monnin						DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444									
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY D. A. DiCenzo						MICROCIRCUIT, PROGRAMMABLE PERIPHERAL INTERFACE, MONOLITHIC SILICON									
				APPROVED BY N. A. Hauck															
				DRAWING APPROVAL DATE 2 JULY 1987						SIZE A		CAGE CODE 67268		5962-87570					
				REVISION LEVEL A						SHEET 1		OF 18		1					

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Use previous edition until exhausted.

5962-E563-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example.

5962-87570	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8255A	Programmable peripheral interface
02	8255A-5	Programmable peripheral interface

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package
X	C-5 (44-terminal, .650" x .650"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range	- - - - -	-0.5 V dc to +7.0 V dc
Storage temperature range	- - - - -	-65°C to +150°C
Maximum power dissipation (P_D) ^{1/}	- - - - -	1.0 W
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):		
Cases Q and X	- - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J)	- - - - -	+126.9°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	- - - - -	+5 V dc \pm 10 percent
Minimum high level input voltage (V_{IH})	- - - - -	2.2 V dc
Maximum low level input voltage (V_{IL})	- - - - -	0.8 V dc
Minimum low level input voltage (V_{IL})	- - - - -	-0.5 V dc
Maximum high level input voltage (V_{IH})	- - - - -	+5.5 V dc
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C

^{1/} Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	$V_{CC} = 5.5\text{ V}$ $V_{CC} = 4.5\text{ V}$	1, 2, 3	ALL		0.8	V
Input high voltage	V_{IH}	$V_{CC} = 5.5\text{ V}$ $V_{CC} = 4.5\text{ V}$	1, 2, 3	ALL	2.2		V
Output low voltage-DATABUS	V_{OL}	$V_{CC} = 5.5\text{ V}$ $I_{OL} = 2.5\text{ mA}$	1, 2, 3	ALL		.45	V
Output low voltage-PORTS	V_{OL}	$V_{CC} = 5.5\text{ V}$ $I_{OL} = 1.7\text{ mA}$	1, 2, 3	ALL		.45	V
Output high voltage-DATABUS	V_{OH}	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -400\mu\text{A}$	1, 2, 3	ALL	2.4		V
Output high voltage-PORTS	V_{OH}	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -200\mu\text{A}$	1, 2, 3	ALL	2.4		V
Darlington drive current	I_{DAR}	$V_{CC} = 4.5\text{ V}, 5.5\text{ V}$ (port B and C)	1, 2, 3	ALL	-1.0	-4.0	mA
Power supply current	I_{CC}	$V_{CC} = 5.5\text{ V}$ 1/	1, 2, 3	ALL		120	mA
Input load current	I_{IL}	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 5.5\text{ V to } 0\text{ V}$	1, 2, 3	ALL	-10	+10	μA
Output float leakage	I_{OFL}	$V_{CC} = 5.5\text{ V}$ $V_{OUT} = 5.5\text{ V to } .45\text{ V}$	1, 2, 3	ALL	-10	+10	μA
Input capacitance	C_{IN}	$T_C = +25^\circ\text{C}$ $F_C = 1\text{ MHz}$ See 4.3.1d	4	ALL		25	pF
I/O capacitance	$C_{I/O}$	$T_C = +25^\circ\text{C}$, see 4.3.1d Unmeasured pins are returned to ground $V_{CC} = \text{GND} = 0\text{ V}$	4	ALL		25	pF
Functional test		See 4.3.1c	7,8	ALL			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Address stable before READ	t _{AR}	V _{CC} = 5.5 V, 4.5 V V _{IH} = 2.4 V V _{IL} = 0.45 V V _{OH} = 2.0 V V _{OL} = 0.8 V (See figures 4 and 5)	9, 10, 11	ALL	0		ns	
Address stable after READ	t _{RA}		9, 10, 11	ALL	0		ns	
READ pulse width	t _{RR}		9, 10, 11	ALL	300		ns	
Data valid from READ	t _{RD}	C _L = 100 pF	9, 10, 11	01		250	ns	
				02		200		
Data float after READ	t _{DF} 2/		9, 10, 11	01	10 3/	150	ns	
				02	10	100		
Time between READS and/or WRITES	t _{RV}		9, 10, 11	ALL	850 3/		ns	
Address stable before WRITE	t _{AW}		9, 10, 11	ALL	0		ns	
Address stable after WRITE	t _{WA}		9, 10, 11	ALL	20		ns	
WRITE pulse width	t _{WW}		9, 10, 11	01	400		ns	
				02	300			
Data valid to WRITE (T.E.)	t _{DW}		9, 10, 11	ALL	100		ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid after WRITE	t_{WD}	$V_{CC} = 5.5\text{ V}, 4.5\text{ V}$ $V_{IH} = 2.4\text{ V}$ $V_{IL} = 0.45\text{ V}$ $V_{OH} = 2.0\text{ V}$ $V_{OL} = 0.8\text{ V}$ $C_L = 100\text{ pF}$ (See figures 4 and 5)	9, 10, 11	ALL	30		ns
Write = 1 to output	t_{WB}		9, 10, 11	ALL		350	ns
Peripheral data before READ	t_{IR}		9, 10, 11	ALL	0		ns
Peripheral data after READ	t_{HR}		9, 10, 11	ALL	0		ns
ACK pulse width	t_{AK}		9, 10, 11	ALL	300		ns
STB pulse width	t_{ST}		9, 10, 11	ALL	500		ns
Peripheral data before T.E. of STB	t_{PS}		9, 10, 11	ALL	0		ns
Peripheral data after T.E. of STB	t_{PH}		9, 10, 11	ALL	180		ns
ACK = 0 to output	t_{AD}		9, 10, 11	ALL		300	ns
ACK = 1 to output float	$t_{KD\frac{3}{}}$		9, 10, 11	ALL	20 $\frac{3}{}$	250 $\frac{3}{}$	ns
WRITE = 1 to OBF = 0	t_{WOB}		9, 10, 11	ALL		650	ns
ACK = 0 to OBF = 1	t_{AOB}		9, 10, 11	ALL		350	ns
STB = 0 to IBF = 1	t_{SIB}		9, 10, 11	ALL		300	ns
READ = 1 to IBF = 0	t_{RIB}		9, 10, 11	ALL		300	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V \leq V _{CC} \leq 5.5 V -55°C \leq T _C \leq +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ = 0 to INTR = 0	t _{RIT}	V _{CC} = 5.5 V, 4.5 V V _{IH} = 2.4 V V _{IL} = 0.45 V	9, 10, 11	ALL		400	ns
STB = 1 to INTR = 1	t _{SIT}	V _{OH} = 2.0 V V _{OL} = 0.8 V C _L = 100 pF (See figures 4 and 5)	9, 10, 11	ALL		300	ns
ACK = 1 to INTR = 1	t _{AIT}		9, 10, 11	ALL		350	ns
WRITE = 0 to <u>4</u> / INTR = 0	t _{WIT}		9, 10, 11	ALL		850	ns

1/ I_{CC} test conditions: The supply current is measured with loaded outputs while running ac patterns.

2/ AC float timing parameters t_{DF} and t_{KD} are tested logic 0 to float only.

3/ Guaranteed if not tested.

4/ When measured from WRITE = 0 to INTRO = 0: The limits shall be as follows: For device type 01, maximum limit shall be as specified at 850 ns; for device type 02, limit shall be as specified at 750 ns maximum.

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 sufficient to verify the truth table on figure 2.

d. Subgroup 4 (C_{IN} and C_{I/O} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

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Case X

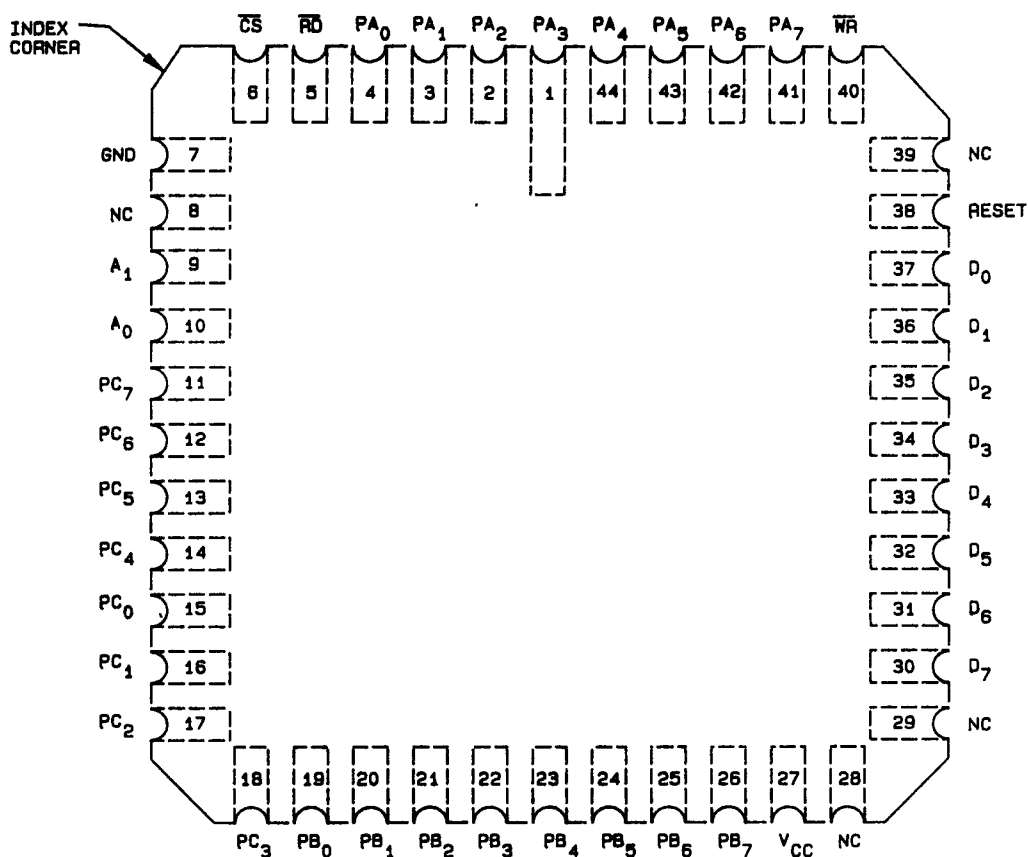
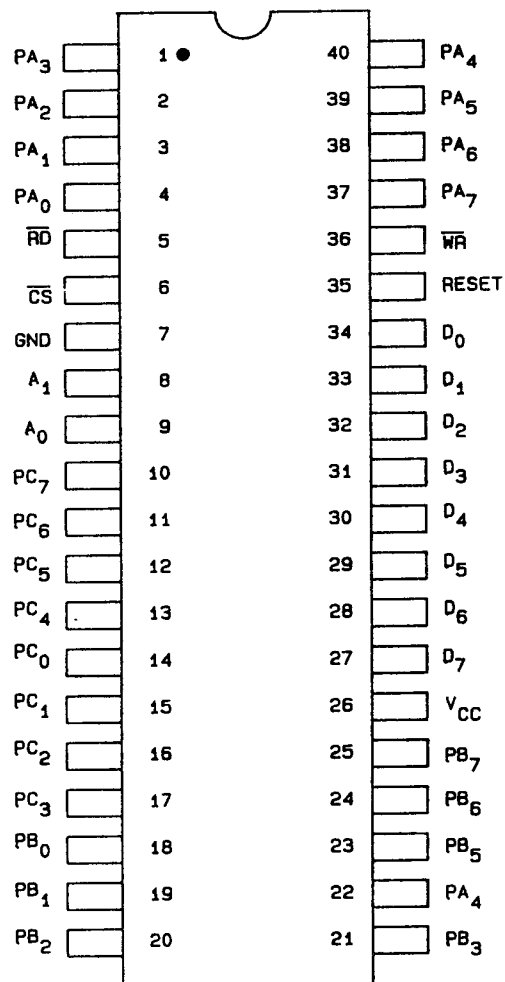


FIGURE 1. Terminal connections.

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NOTE: Pin 1 is marked for orientation.

FIGURE 1. Terminal connections - Continued.

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A ₁	A ₀	\overline{RD}	\overline{WR}	\overline{CS}	Input operation (read)
0	0	0	1	0	Port A-data bus
0	1	0	1	0	Port B-data bus
1	0	0	1	0	Port C-data bus
					Output operation (write)
0	0	1	0	0	Data bus-port A
0	1	1	0	0	Data bus-port B
1	0	1	0	0	Data bus-port C
1	1	1	0	0	Data bus-control
					Disable function
X	X	X	X	1	Data bus-three-state
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data bus-three-state

FIGURE 2. Truth table.

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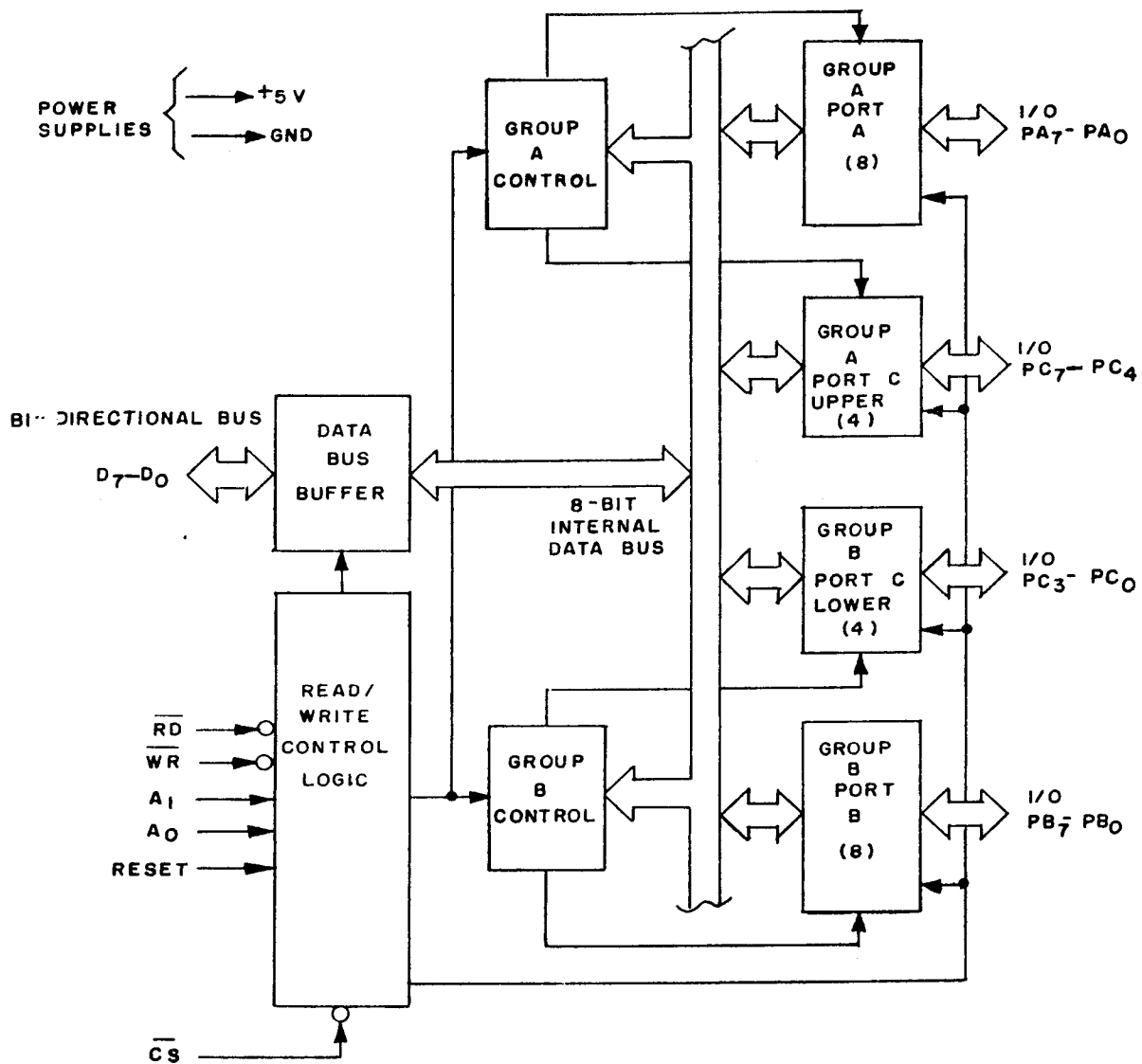
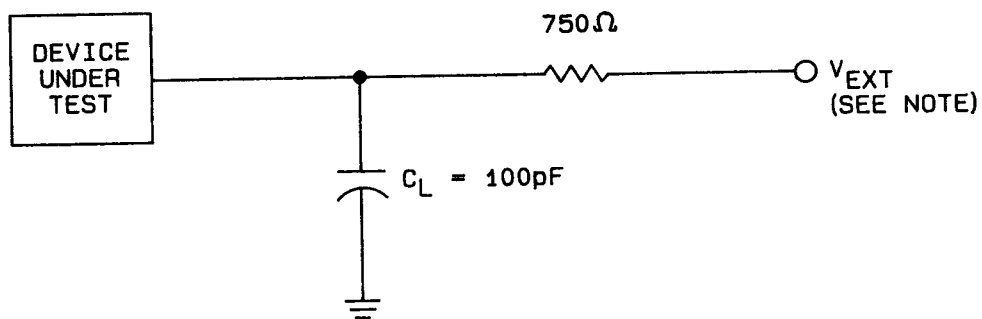


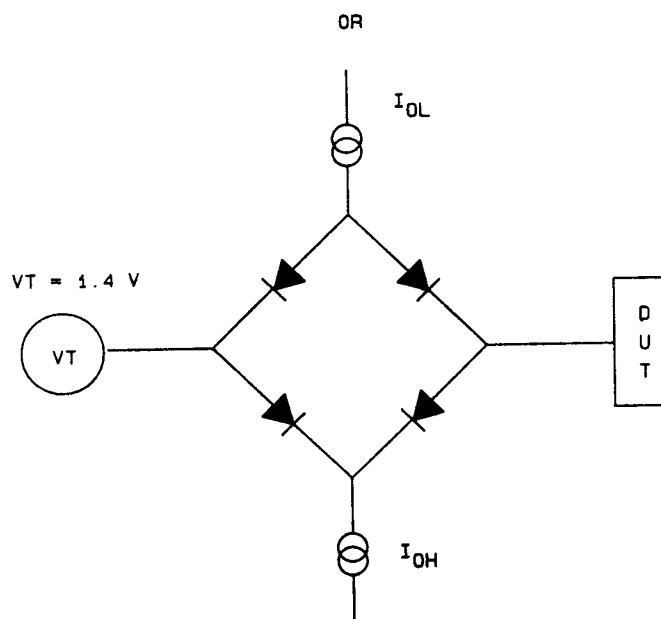
FIGURE 3. Block diagram.

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NOTE: V_{EXT} is set at various voltages during testing to guarantee the specification.

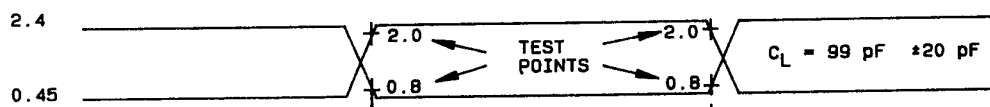


NOTE: test circuit is the dynamic load of a Teradyne J941 or equivalent.

FIGURE 4. AC testing load circuits.

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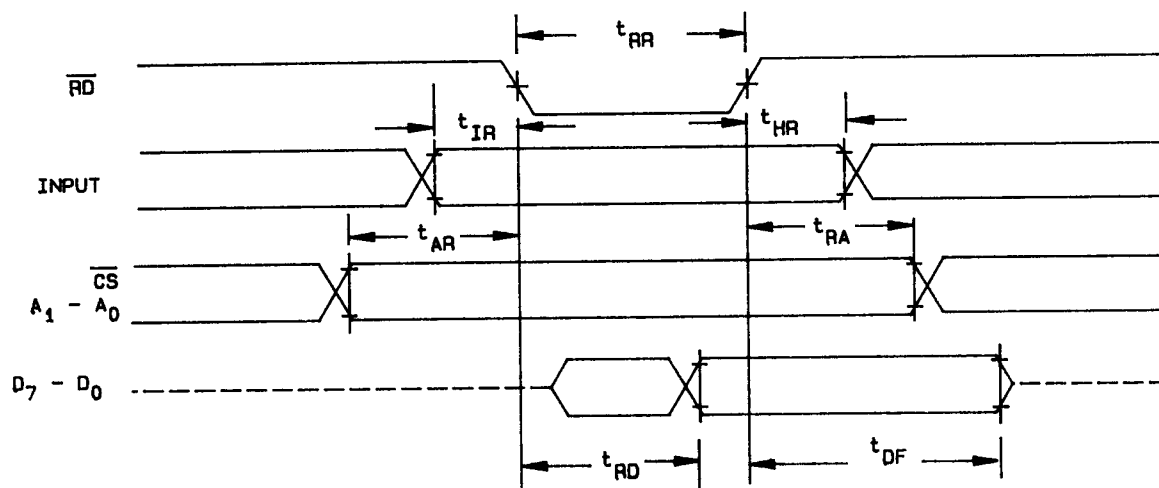


NOTE: AC testing. Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

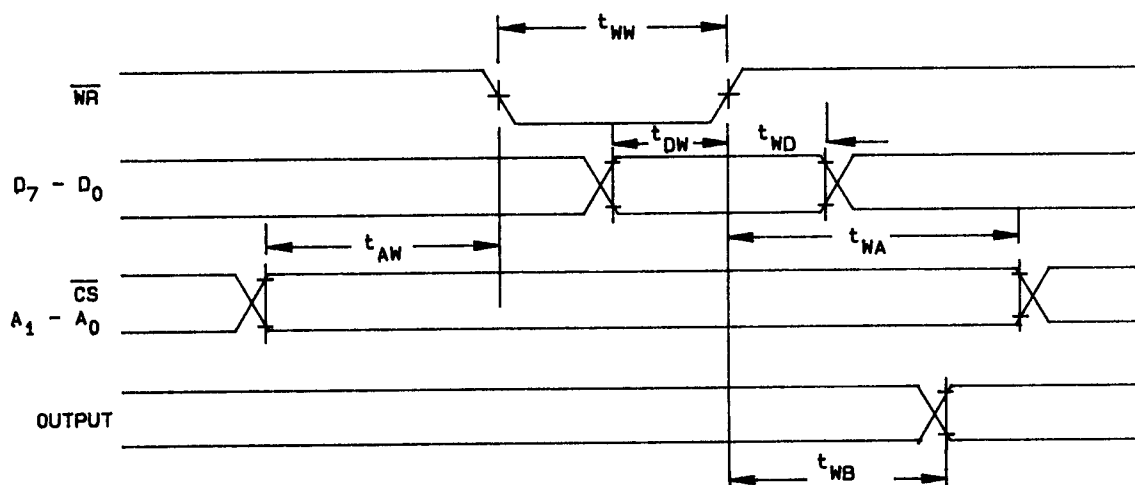
FIGURE 5. AC testing input and output waveform.

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MODE 0
(BASIC INPUT)



MODE 0
(BASIC OUTPUT)

FIGURE 6. Switching waveforms.

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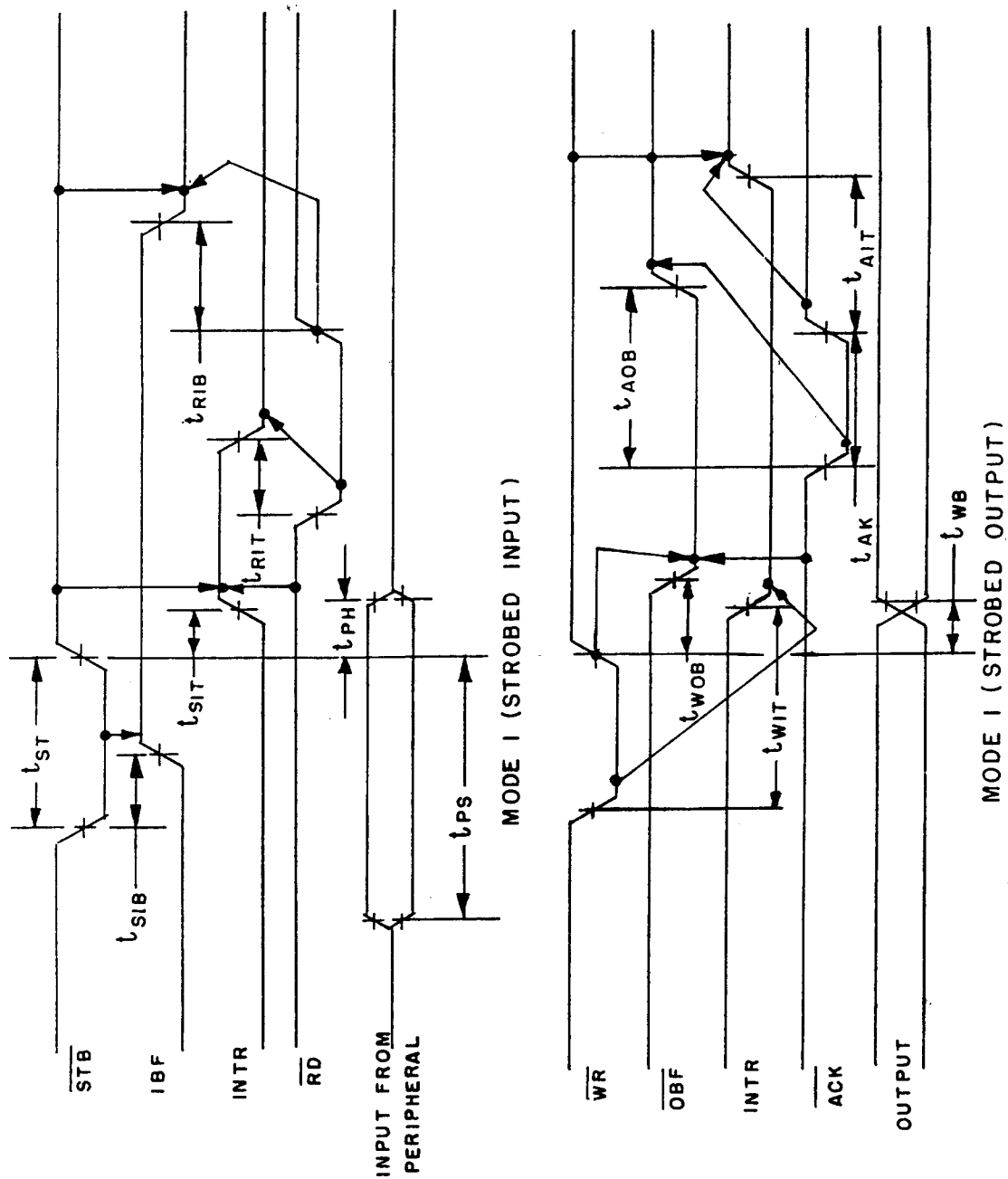


FIGURE 6. Switching waveforms - Continued.

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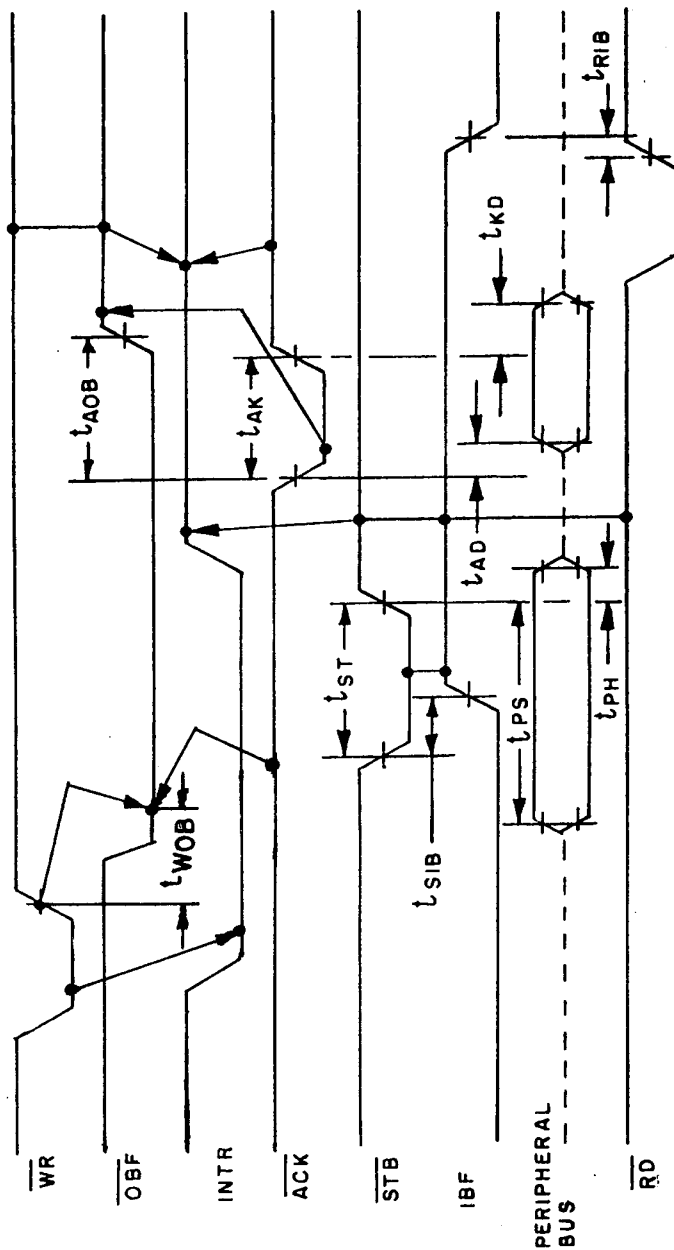
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MODE 2
(BIDIRECTIONAL)

NOTE: Any sequence where \overline{WR} occurs before \overline{ACK} and \overline{STB} occur before \overline{RD} is permissible
($\overline{INTR} = \overline{IBF} \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$).

FIGURE 6. Switching waveforms - Continued.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8a, 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

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6.6 Pin description. The following pin descriptions are applicable to this drawing.

Pin no. case X	Pin no. case Q	Name	I/O	Pin description
30-37	27-34	D7-D0	I/O	Data bus (bidirectional)
38	35	Reset	I	Reset input
6	6	\overline{CS}	I	Chip select
5	5	\overline{RD}	I	Read input
40	36	\overline{WR}	I	Write input
10, 9	9, 8	A0, A1	I	Port address
41-44, 1-4	37-40, 1-4	PA7-PA0	I/O	Port A (bit)
26-19	25-18	PB7-PB0	I/O	Port B (bit)
11-15, 18-16	10-13, 17-14	PC7-PC0	I/O	Port C (bit)
27	26	V _{CC}		+5 V
7	7	GND		0 V

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

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