PI74FCT16501T
PI74FCT162501T
PI74FCT162H501T

Fast CMOS 18-Bit Registered Transceivers

Product Features

Common Features:

- PI74FCT16501T, PI74FCT162501T, and PI74FCT162H501T are high-speed, low power devices with high current drive.
- V_{CC} = 5V ±10%
- Hysteresis on all inputs
- Packages available
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 300 mil wide plastic SSOP (V)

PI74FCT16501T Features

- High output drive: I_{OH} = –32 mA; I_{OL} = 64 mA
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C

PI74FCT162501T Features

- Balanced output drivers: ±24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

PI74FCT162H501T Features

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull-up resistors

Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

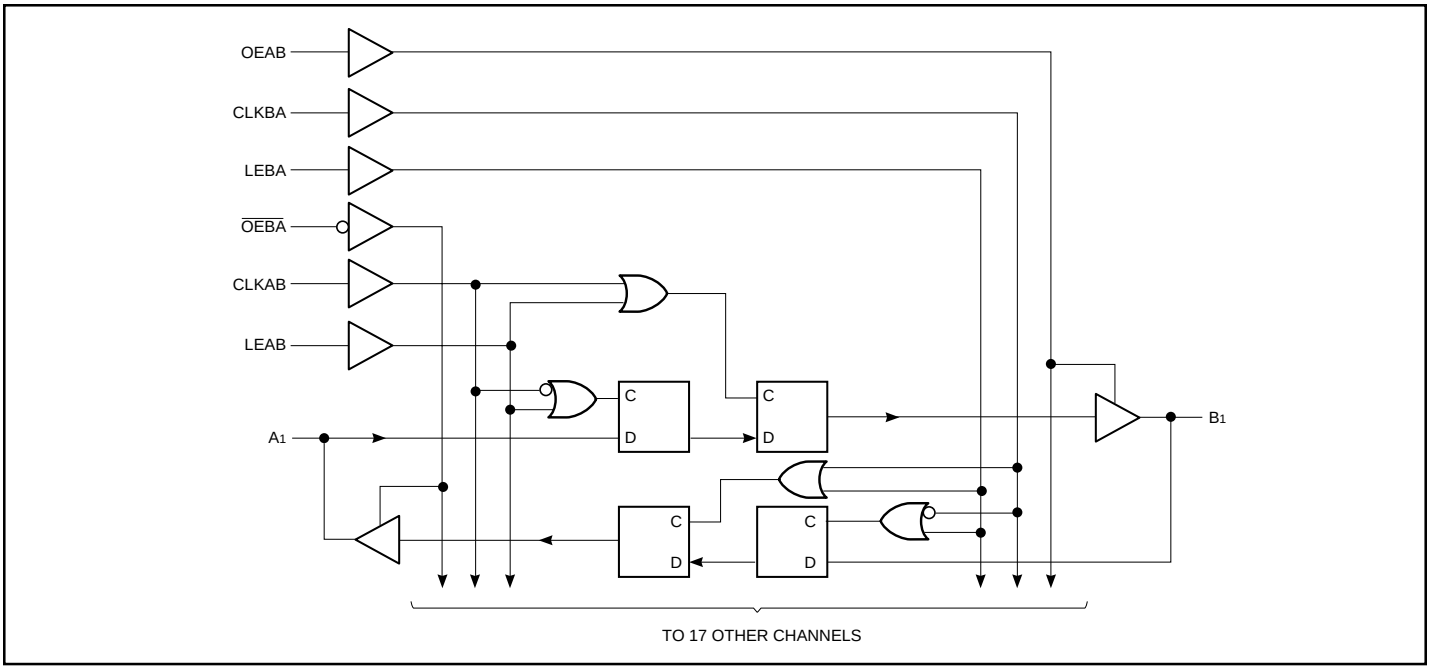
The PI74FCT16501T, PI74FCT162501T, and PI74FCT162H501T are 18-bit registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, $\overline{\text{LEBA}}$ and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The PI74FCT16501T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162501T has ±24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H501T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram



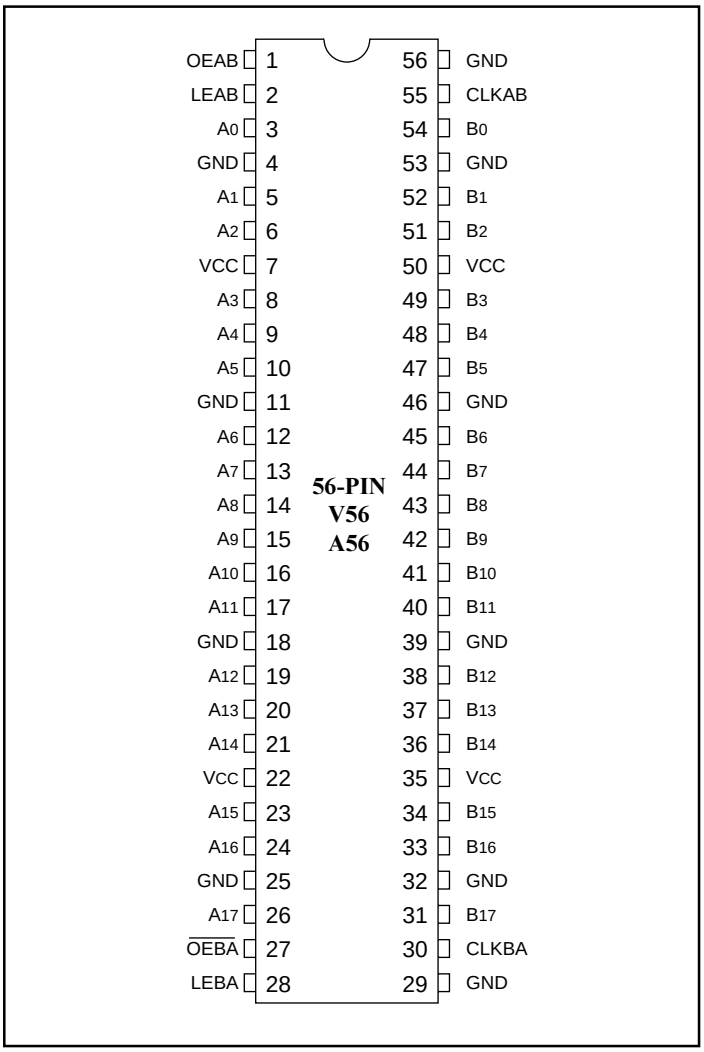
PS2035A 03/11/96

Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs(1)
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs(1)
GND	Ground
VCC	Power

Note: 1. For the PI74FCT162H501T, these pins have "Bus Hold." All other pins are standard, outputs, or I/Os.

Product Pin Configuration



Truth Table(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B(2)
H	L	H	X	B(3)

Notes:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	Standard Input, V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IH}	Input HIGH Current	Standard I/O, V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IH}	Input HIGH Current	Bus Hold Input[4], V_{CC} = Max.	V_{IN} = V_{CC}			±100	µA
I_{IH}	Input HIGH Current	Bus Hold I/O[4], V_{CC} = Max.	V_{IN} = V_{CC}			±100	µA
I_{IL}	Input LOW Current	Standard Input, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Standard I/O, V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{IL}	Input LOW Current	Bus Hold I/O[4], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{BHH}	Bus Hold	Bus Hold Input[4], V_{CC} = Min.	V_{IN} = 2.0V	–50			µA
I_{BHL}	Sustain Current		V_{IN} = 0.8V	+50			
I_{OZH}[5]	High-Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}[5]	Output Current (3-State Outputs)	V_{CC} = Max.	V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

PI74FCT16501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.0 mA	2.5	3.5		V
			I_{OH} = –15.0 mA	2.4	3.5		
			I_{OH} = –32.0 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.2	0.55	V
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		—	—	±100	µA

PI74FCT162501T/162H501T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.8	1.7[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		1.3	4.2[5]	
		V_{CC} = Max., Output Open f_{CP} = 10 MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND Eighteen Bits Toggling f_i = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND		8.5	20.8[5]	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16501T Switching Characteristics over Operating Range

Parameters	Description		Conditions[1]	16501AT Com. Min	16501AT Com. Max	16501CT Com. Min	16501CT Com. Max	16501DT Com. Min	16501DT Com. Max	16501ET Com. Min	16501ET Com. Max	Unit
t_{MAX}	CLKAB or CLKBA frequency		$C_L = 50$ pF	—	150	—	150	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Ax to Bx		$R_L = 500\Omega$	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
t_{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			3.0	—	3.0	—	3.0	—	2.4	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH		3.0	—	3.0	—	3.0	—	2.0	—	ns
		Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	0.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162501T Switching Characteristics over Operating Range

Parameters	Description		Conditions[1]	162501AT Com. Min	162501AT Com. Max	162501CT Com. Min	162501CT Com. Max	162501DT Com. Min	162501DT Com. Max	162501ET Com. Min	162501ET Com. Max	Unit
t_{MAX}	CLKAB or CLKBA frequency		C_L = 50 pF	—	150	—	150	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Ax to Bx		R_L = 500Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
t_{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			3.0	—	3.0	—	3.0	—	2.4	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH		3.0	—	3.0	—	3.0	—	2.0	—	ns
		Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	0.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162H501T Switching Characteristics over Operating Range (Advance Information)

Parameters	Description		Conditions[1]	162H501AT Com. Min	162H501AT Com. Max	162H501CT Com. Min	162H501CT Com. Max	162H501DT Com. Min	162H501DT Com. Max	162H501ET Com. Min	162H501ET Com. Max	Unit
t_{MAX}	CLKAB or CLKBA frequency		C_L = 50 pF	—	150	—	150	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Ax to Bx		R_L = 500Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
t_{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			3.0	—	3.0	—	3.0	—	2.4	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	ns
t_{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH		3.0	—	3.0	—	3.0	—	2.0	—	ns
		Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	0.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.