DS04-21204-6aE

FUJITSU

DATA SHEET

MB87006A *Frequency Synthesizer*

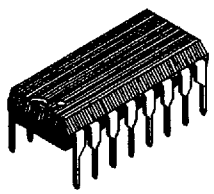
CMOS Serial Input Phase Locked Loop (PLL)

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

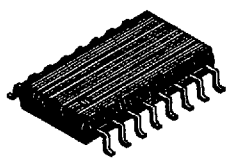
The Fujitsu MB87006A, fabricated in CMOS technology, is a serial input Phase Locked Loop (PLL) frequency synthesizer.

The MB87006A contains an inverter for connection to an external oscillator, programmable reference divider (binary 14-bit programmable reference counter), 14-bit shift register, 14-bit latch, phase detector, charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter) and control generator for dual modulus prescaler.
When supplemented with a loop filter and VCO, the MB87006A contains the necessary circuitry to make up a Phase Locked Loop (PLL). Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1GHz.

- Wide range power supply voltage: V_{CC} = 3.0 to 6.0V
- Wide temp range: Ta = −40 to 85°C
- 17MHz typical input capability @5V (fin input)
- On-chip inverter for oscillator
- Programmable divider with input amplifier consisting of:
  - Binary 7-bit swallow counter
  - Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of:
  - Binary 14-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input (The last data bit is a control bit)
- 2-types of phase detector output
  - On-chip charge pump output
  - Output for external charge pump
- Easy interface with Fujitsu prescalers
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)

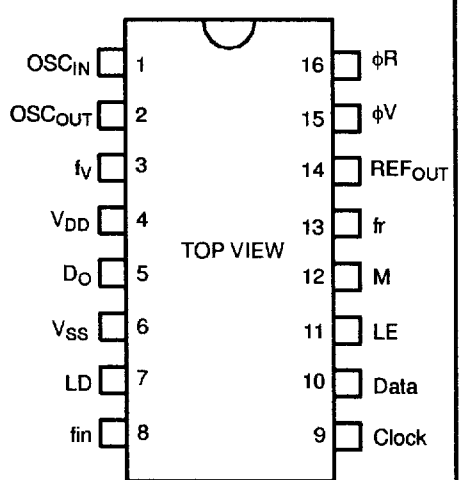


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



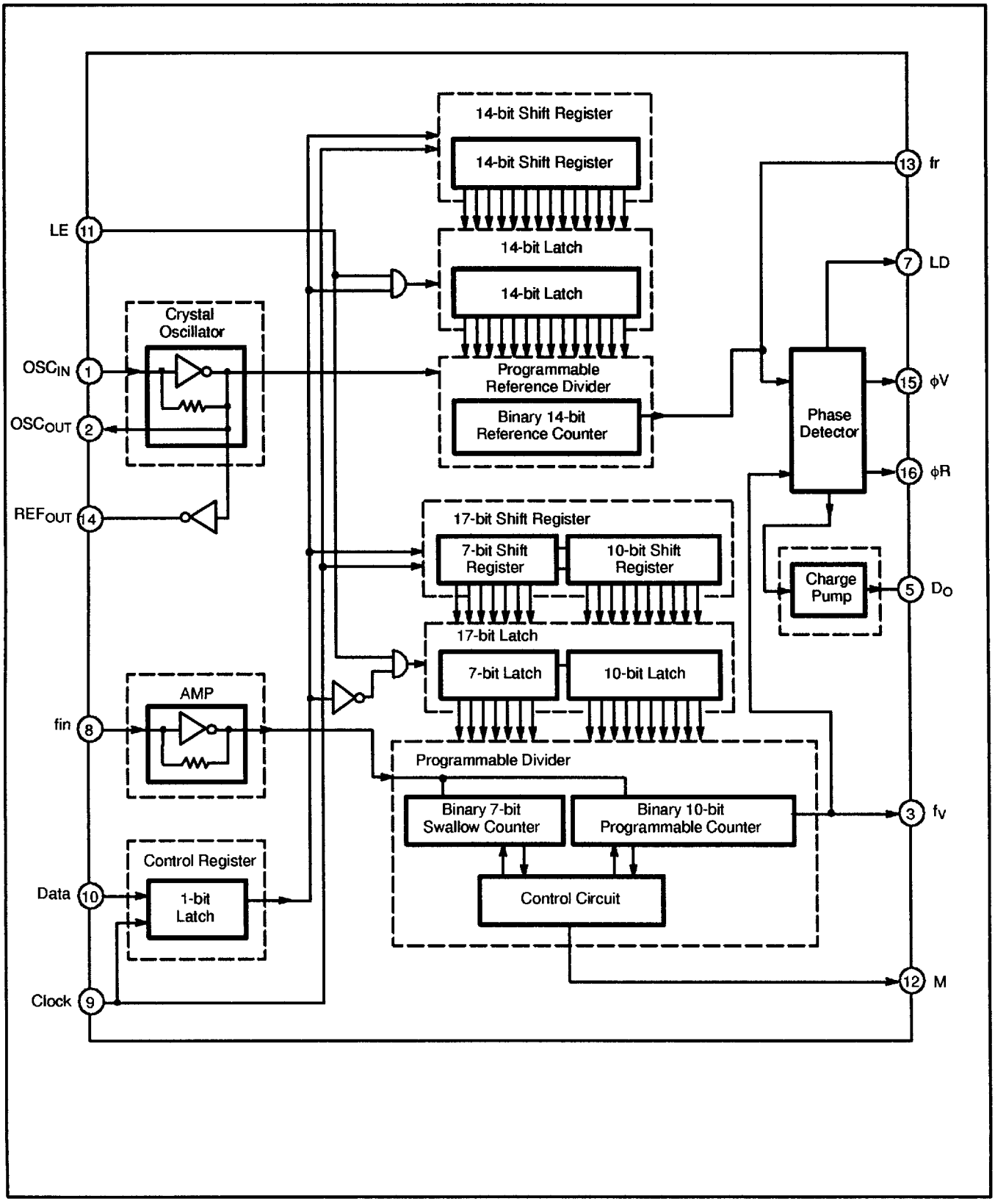
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} −0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	Ta	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTION

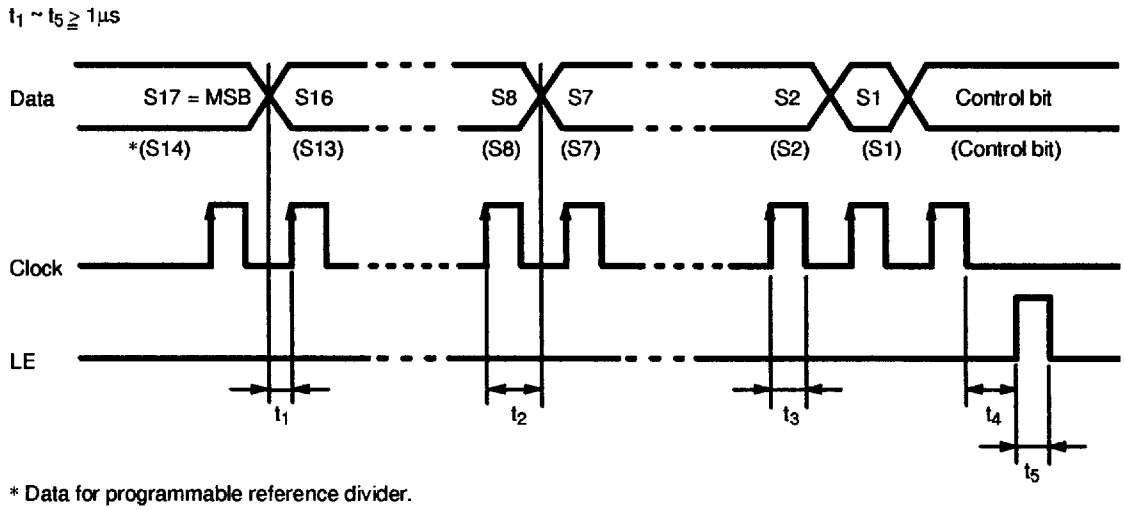
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	O	Monitor output of the phase detector. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_O	O	Three-state charge pump output of phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: $fr > f_V$: Drive mode (D_O = High level) $fr = f_V$: High impedance $fr < f_V$: Sink mode (D_O = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are equal, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	fin	I	Clock input for programmable divider. This input contains internal bias circuit and amplifier. The connection with an external dual-modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 17-bit shift register and 14-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for programmable divider and programmable reference divider. The last bit of the data is the control bit. Control bit determines which latch is activated. The data stored in the shift register is transferred to the 14-bit latch when the bit is high, and to 17-bit latch when low.
11	LE	I	Load enable input with internal pull up resistor. When this pin is high (active high), the data stored in shift register is transferred to 14-bit latch or 17-bit latch depending on the control bit data.
12	M	O	Control output for an external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #8). Pulse swallow function: e.g. MB501L: M = High: Preset modulus factor 64 or 128 M = Low Preset modulus factor 65 to 129

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
13	fr	O	Monitors output of phase detector input. This pin is tied to the programmable reference divider output.
14	REF_{OUT}	O	Monitor output pin of the reference frequency. This output can be used as system clock for microprocessor, or reference oscillator for another PLL frequency synthesizer.
15 16	ϕV ϕR	O O	Output for external charge pump. The mode of ϕR and ϕV are changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency f_V as listed below. ϕR ϕV $fr > f_V$: Low-level High-level $fr = f_V$: High-level High-level $fr < f_V$: High-level Low-level

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT TIMING



* Data for programmable reference divider.

Notes: Data: Serial data input is used for setting divide factor of programmable reference divider and progranmable divider.
Data is input from MSB, and last bit data is a control bit.
Control bit is set high when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Data is input to internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data stored in shift register is transferred to 14-bit latch, or 17-bit latch depending on the control bit setting.

PULSE SWALLOW FUNCTION

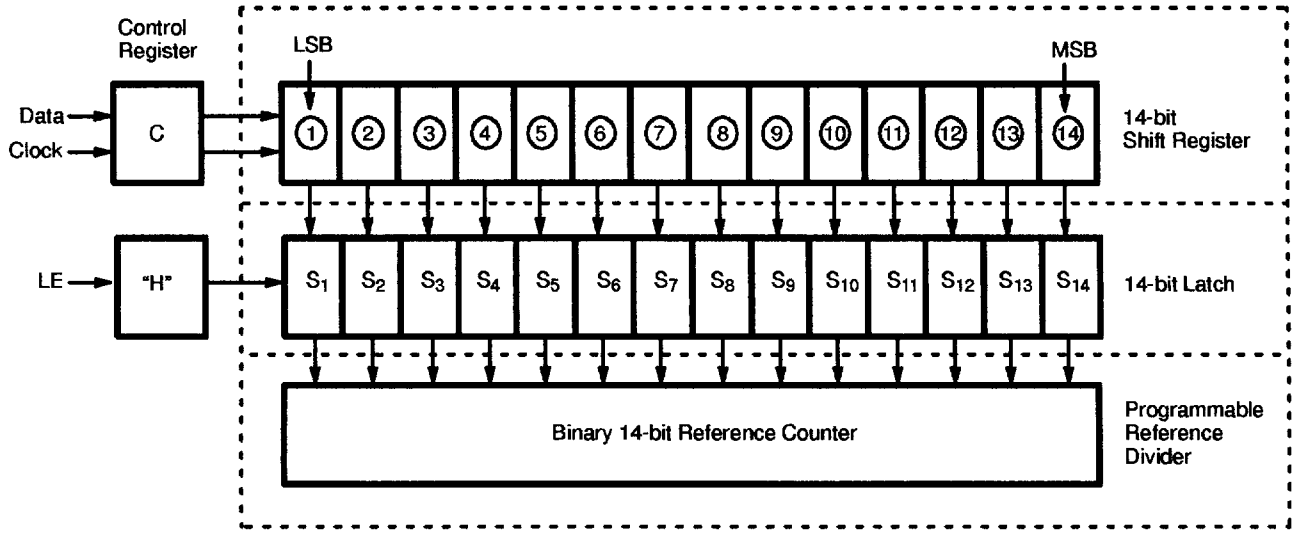
$$f_{VCO} = [(N \times M) + A] \times f_{OSC} \div R \quad (N > A)$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler
(e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit programmable counter (0 to 127, A < N)
f_{OSC} : Output frequency of external oscillator
R : Preset divide factor of binary 14-bit programmable reference counter (5 to 16383)

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

Serial data consists of 14-bit data, which is used for setting divide factor of programmable reference counter, and 1-bit control data. In this case, control bit is set high level.

The data format is shown below.



BINARY 14-BIT REFERENCE COUNTER DATA INPUT

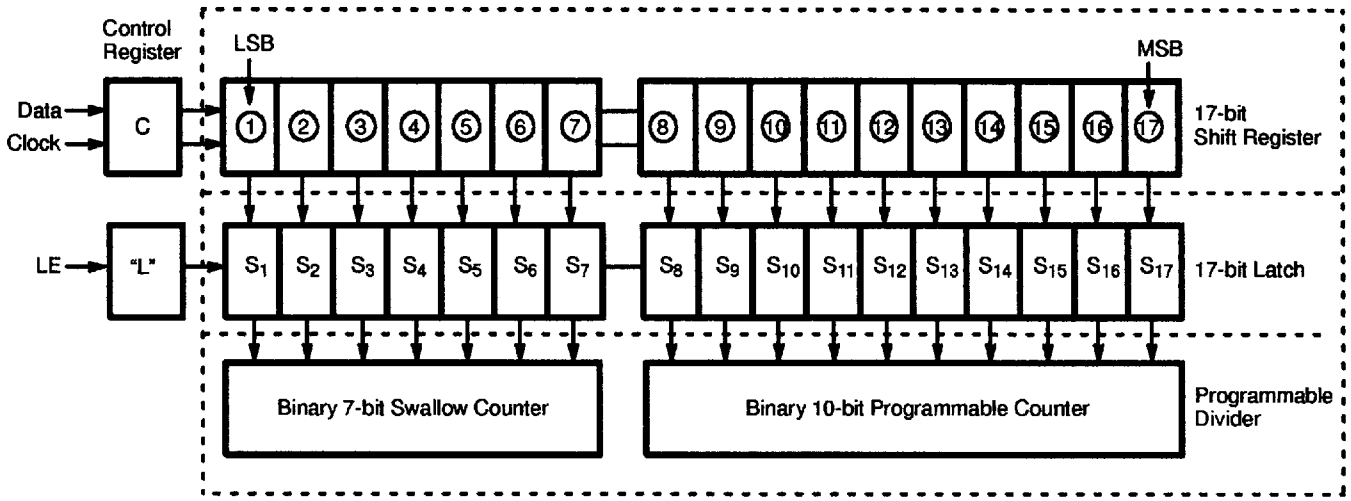
(14)	(13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 16383

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data consists of 17-bit data, which is used for setting divide factor of programmable divider, and 1-bit control data. In this case, control bit is set low level. The data ① to ⑦ set a divide factor of 7-bit swallow counter and data ⑧ to ⑰ set divide factor of 10-bit programmable counter.

The data format is shown below.



BINARY 7-BIT SWALLOW COUNTER DATA INPUT

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

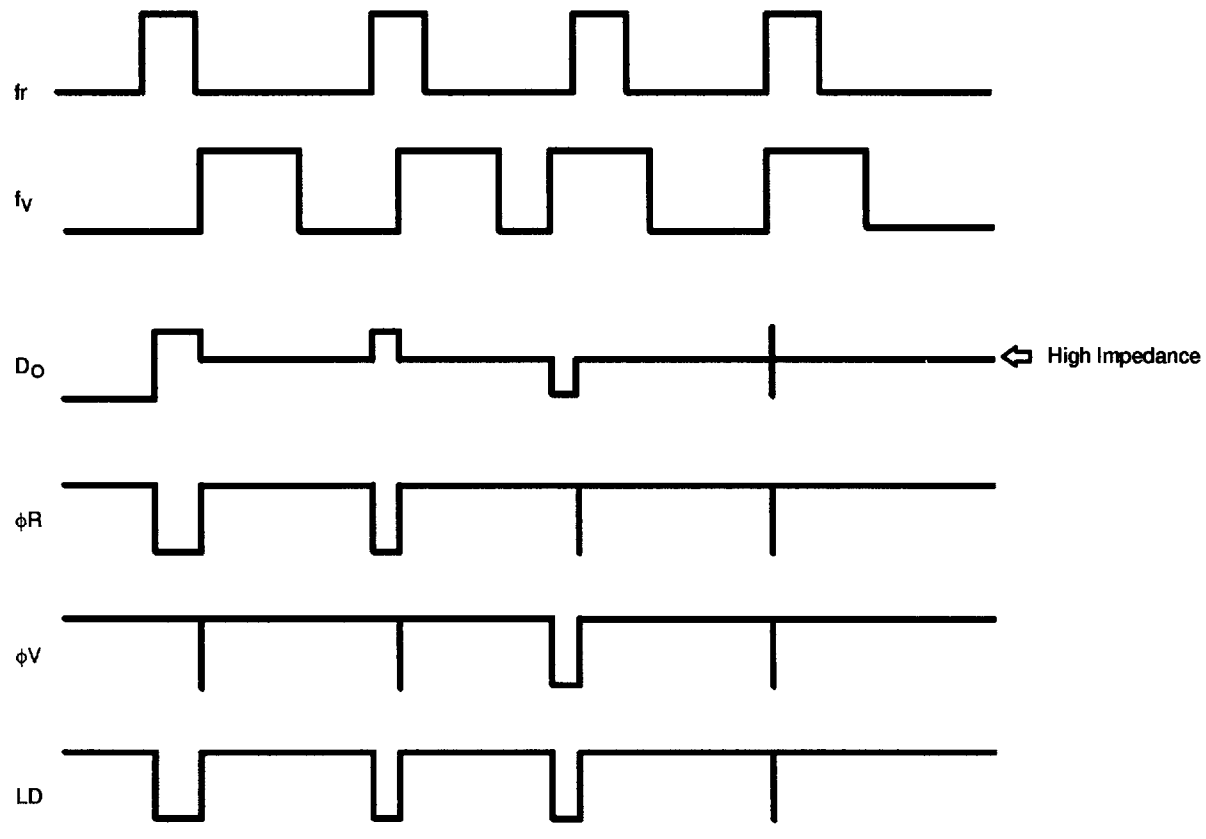
Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
e.g. MB501L (÷65/65)prescaler
SW = H (64/65): Bit 7 to shift register ⑦ should be zero.

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited.
Divide factor N : 5 to 1023

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	3.0	-	6.0	V
Input Voltage	V_{IN}	V_{SS}	-	V_{DD}	V
Operating Temperature	Ta	-40	-	+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5	–	–	V_{P-P}
	OSC_{IN}	Vsin		0.5	–	–	
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	–	1.0	–	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	–	–1.0	–	
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
	LE	I_{LE}	$V_{IN} = V_{SS}$	–	–40	–	µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95	–	–	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	–	–	0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 2.6V	–0.5	–	–	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	0.5	–	–	
High-level Output Current	M	I_{OHM}	V_{OH} = 2.6V	–0.7	–	–	mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	1.5	–	–	
Power Supply Current *1		I_{DD}		–	2.5	–	mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	20	–	MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		10	20	–	MHz

Notes: *1: fin = 8.0MHz 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except for fin and OSC_{IN}. Output are open.

ELECTRICAL CHARACTERISTICS (continued)

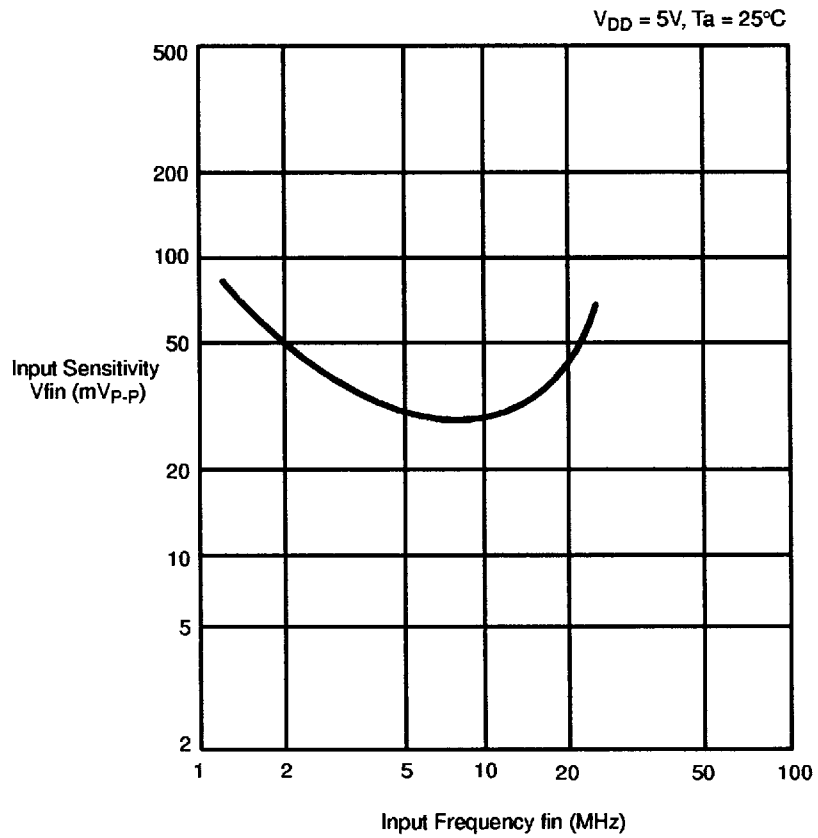
(V_{DD} = 5.0V, V_{SS} = 0V, Ta = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5	–	–	V_{P-P}
	OSC_{IN}	Vsin		0.5	–	–	
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	–	1.0	–	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	–	–1.0	–	
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}	–	±50	–	µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}	–	±50	–	µA
	LE	I_{LE}	$V_{IN} = V_{SS}$	–	–60	–	µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	–	–	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	–	–	0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	–1.0	–	–	mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0	–	–	
High-level Output Current	M	I_{OHM}	V_{OH} = 4.6V	–1.5	–	–	mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	3.0	–	–	
Power Supply Current *1		I_{DD}		–	3.5	–	mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	25	–	MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		17	25	–	MHz

Note: *1. fin = 8.0MHz, 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}. Inputs are ground except for fin and OSC_{IN}. Outputs are open.

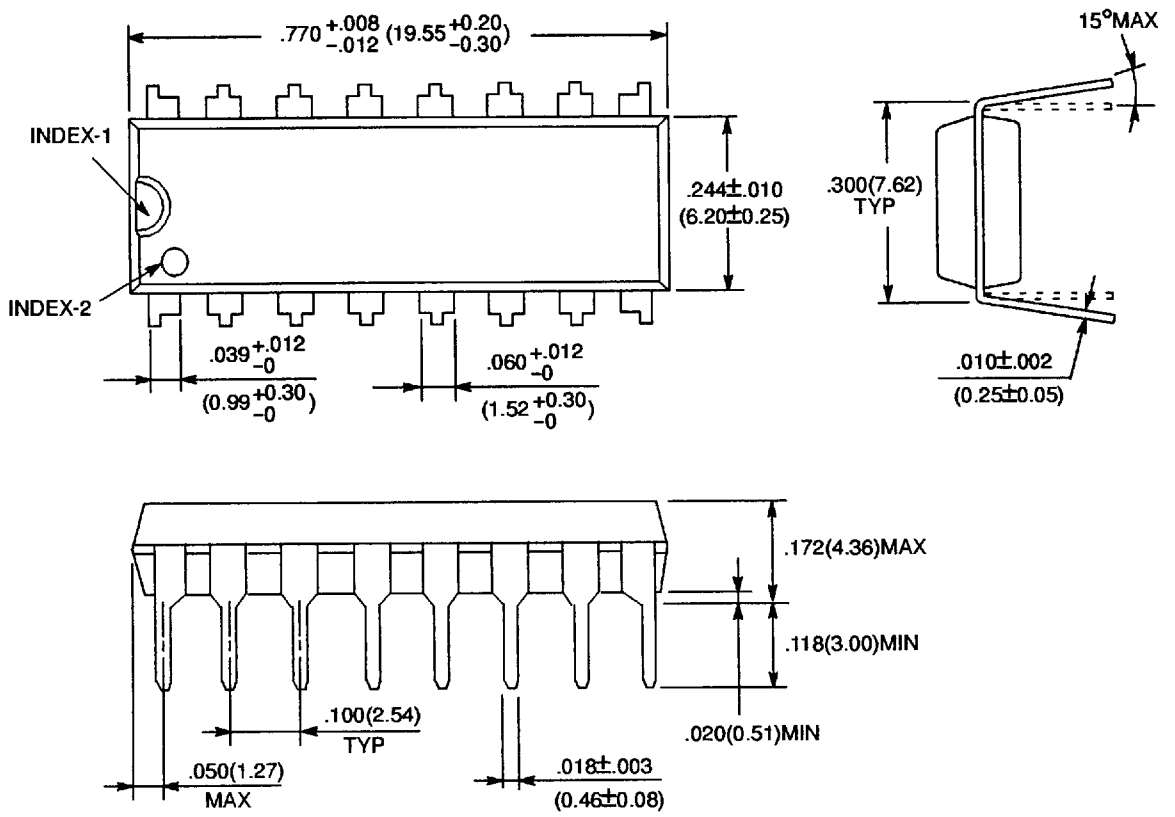
TYPICAL CHARACTERISTICS CURVE

INPUT SEVSITIVITY CHARACTERISTICS (fin Section)



PACKAGE DIMENSIONS

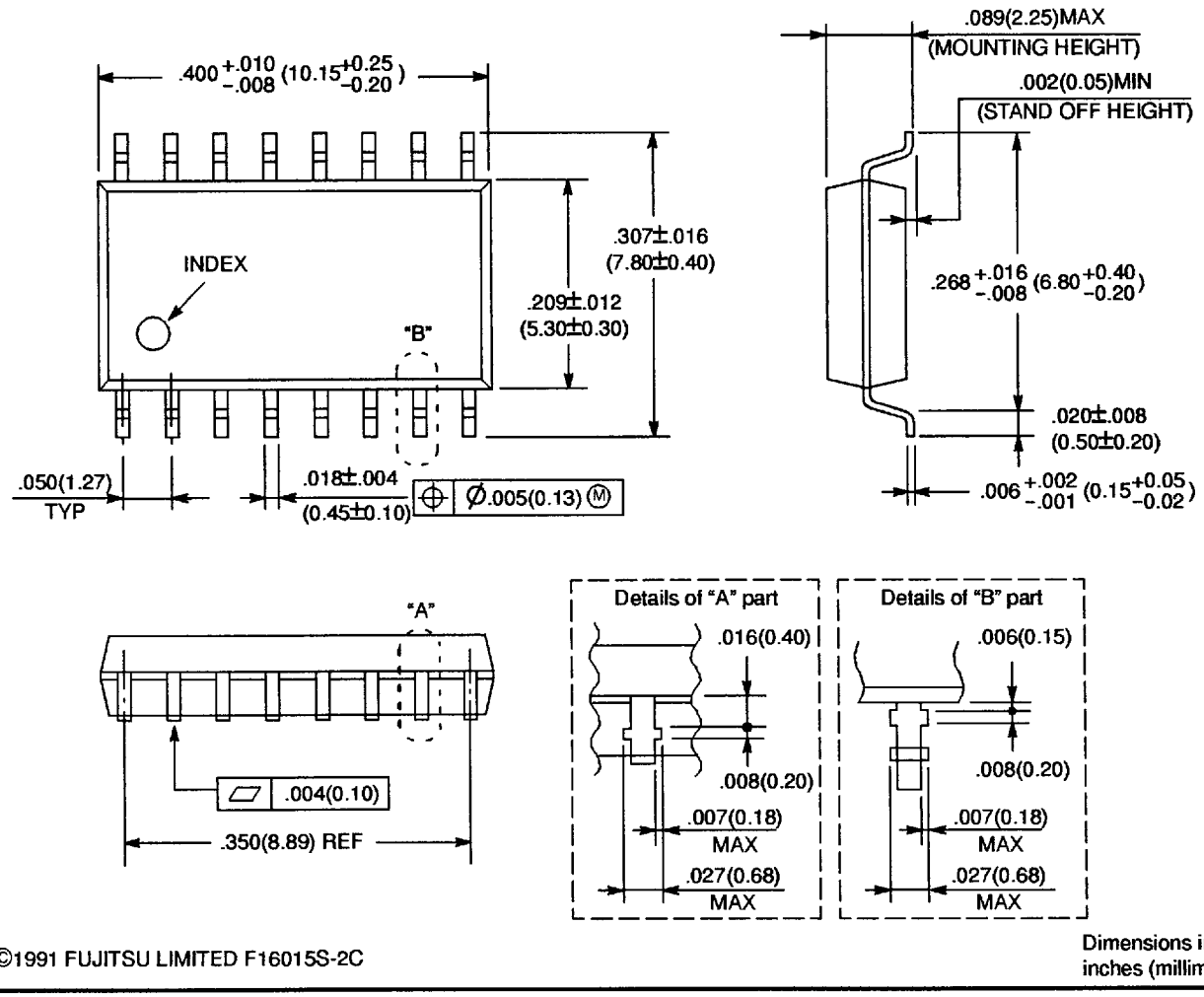
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Electronic Devices
International Operations Department
KAWASAKI PLANT, 1015 Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211, Japan
Tel: (044) 754-3753
FAX: (044) 754-3332

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
FAX: (408) 432-9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
FAX: (06103) 690-122

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
No. 51 Bras Basah Road,
Plaza By The Park,
#06-04 to #06-07
Singapore 0718
Tel: 336-1600
FAX: 336-1609

I9411