

FSFR-XS Series — Fairchild Power Switch (FPS™) for Half-Bridge Resonant Converters

Features

- Variable Frequency Control with 50% Duty Cycle for Half-Bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Internal UniFET™ with Fast-Recovery Body Diode
- Fixed Dead Time (350ns) Optimized for MOSFETs
- Up to 300kHz Operating Frequency
- Auto-Restart Operation for All Protections with External LV_{CC}
- Protection Functions: Over-Voltage Protection (OVP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies

Description

The FSFR-XS series includes highly integrated power switches designed for high-efficiency half-bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FSFR-XS series simplifies designs while improving productivity and performance. The FSFR-XS series combines power MOSFETs with fast-recovery type body diodes, a high-side gate-drive circuit, an accurate current controlled oscillator, frequency limit circuit, soft-start, and built-in protection functions. The high-side gate-drive circuit has common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. The fast-recovery body diode of the MOSFETs improves reliability against abnormal operation conditions, while minimizing the effect of reverse recovery. Using the zero-voltage-switching (ZVS) technique dramatically reduces the switching losses and significantly improves efficiency. The ZVS also reduces the switching noise noticeably, which allows a small-sized Electromagnetic Interference (EMI) filter.

The FSFR-XS series can be applied to resonant converter topologies such as series resonant, parallel resonant, and LLC resonant converters.

Related Resources

[AN4151 — Half-bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch \(FPS™\)](#)

Ordering Information

Part Number	Package	Operating Junction Temperature	R _{DS(ON_MAX)}	Maximum Output Power without Heatsink (V _{IN} =350~400V) ^(1,2)	Maximum Output Power with Heatsink (V _{IN} =350~400V) ^(1,2)
FSFR2100XS	9-SIP	-40 to +130°C	0.51Ω	180W	400W
FSFR1800XS			0.95Ω	120W	260W
FSFR1700XS			1.25Ω	100W	200W
FSFR1600XS			1.55Ω	80W	160W
FSFR2100XSL	9-SIP L-Forming		0.51Ω	180W	400W
FSFR1800XSL			0.95Ω	120W	260W
FSFR1700XSL			1.25Ω	100W	200W
FSFR1600XSL			1.55Ω	80W	160W

Notes:

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.

Application Circuit Diagram

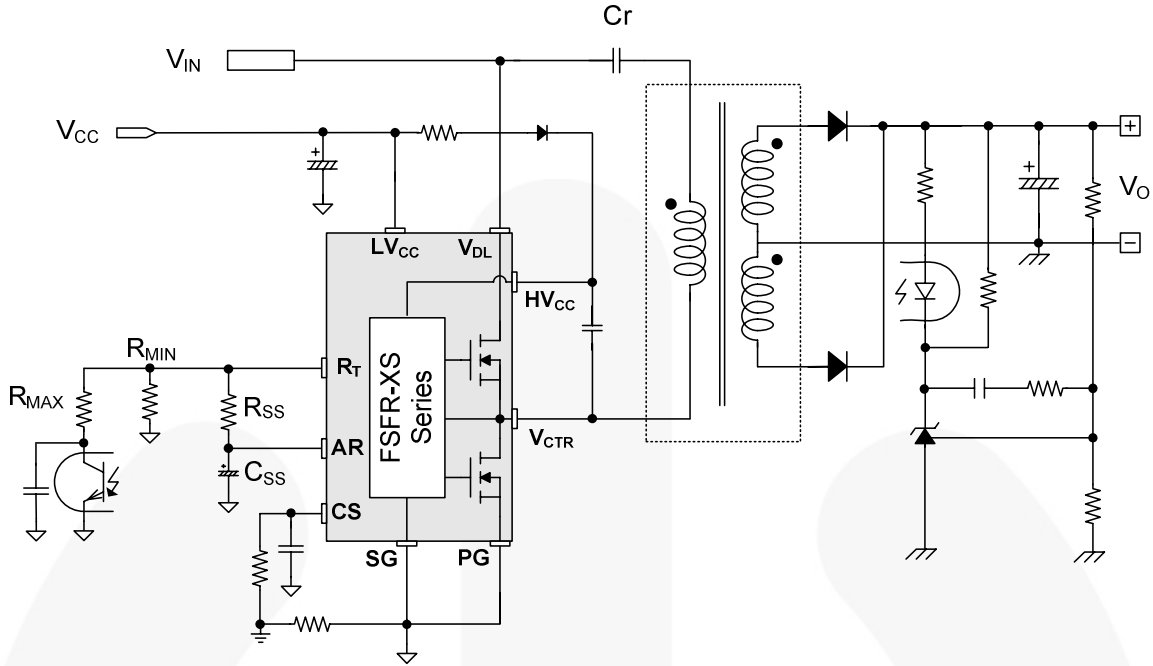


Figure 1. Typical Application Circuit (LLC Resonant Half-Bridge Converter)

Block Diagram

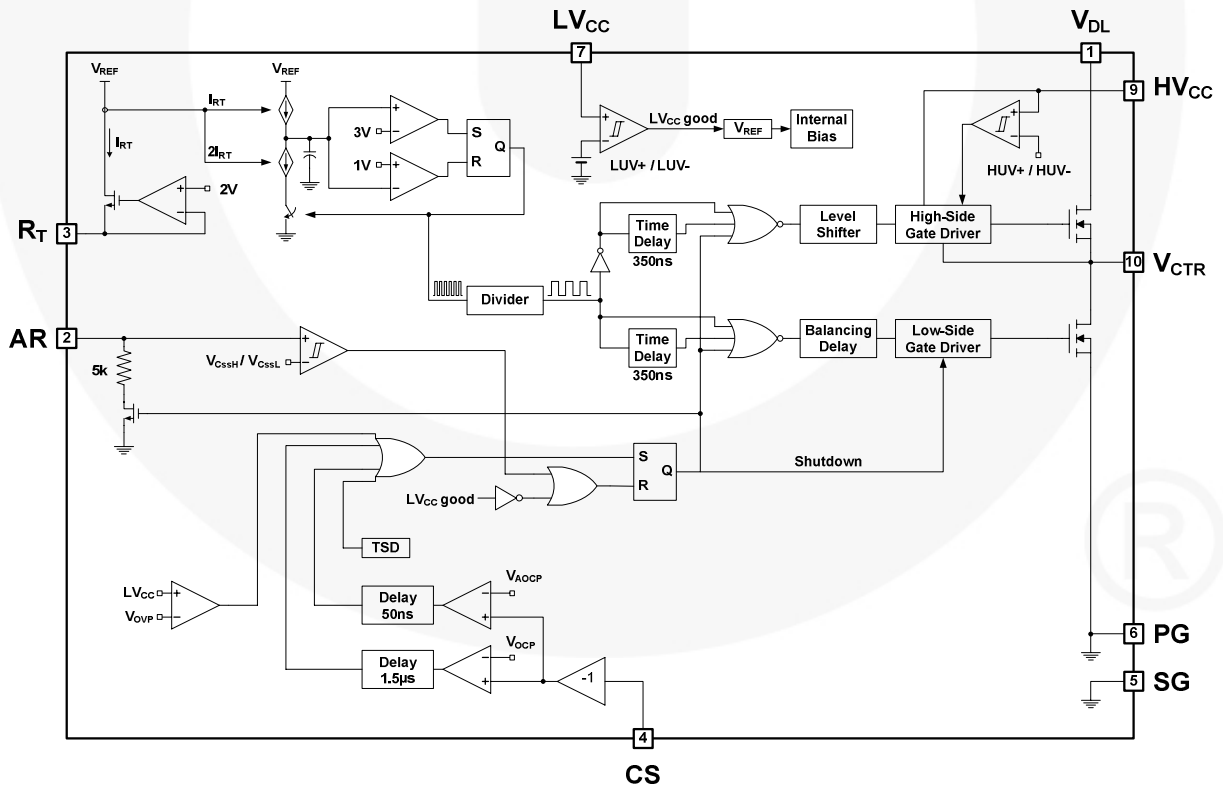


Figure 2. Internal Block Diagram

Pin Configuration

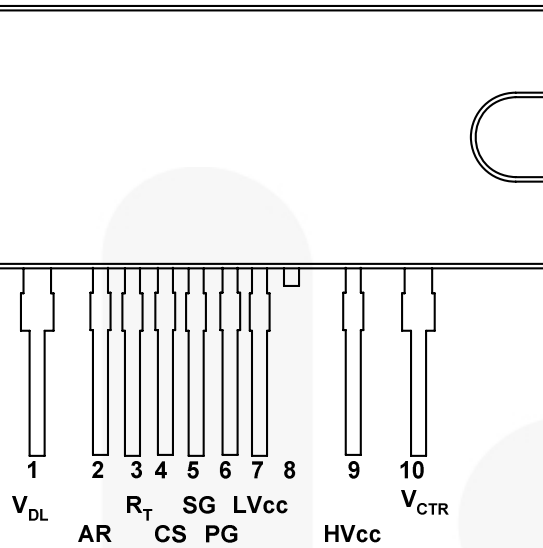


Figure 3. Package Diagram

Pin Definitions

Pin #	Name	Description
1	V_{DL}	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	AR	This pin is for discharging the external soft-start capacitor when any protections are triggered. When the voltage of this pin drops to 0.2V, all protections are reset and the controller starts to operate again.
3	R_T	This pin programs the switching frequency. Typically, an opto-coupler is connected to control the switching frequency for the output voltage regulation.
4	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LV_{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HV_{CC}	This is the supply voltage of the high-side gate-drive circuit IC.
10	V_{CTR}	This is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	
V_{DS}	Maximum Drain-to-Source Voltage ($V_{DL}-V_{CTR}$ and $V_{CTR}-PG$)	500		V	
LV_{CC}	Low-Side Supply Voltage	-0.3	25.0	V	
HV_{CC} to V_{CTR}	High-Side V_{CC} Pin to Low-Side Drain Voltage	-0.3	25.0	V	
HV_{CC}	High-Side Floating Supply Voltage	-0.3	525.0	V	
V_{AR}	Auto-Restart Pin Input Voltage	-0.3	LV_{CC}	V	
V_{CS}	Current-Sense (CS) Pin Input Voltage	-5.0	1.0	V	
V_{RT}	R_T Pin Input Voltage	-0.3	5.0	V	
dV_{CTR}/dt	Allowable Low-Side MOSFET Drain Voltage Slew Rate		50	V/ns	
P_D	Total Power Dissipation ⁽³⁾	FSFR2100XS/L	12.0	W	
		FSFR1800XS/L	11.7		
		FSFR1700XS/L	11.6		
		FSFR1600XS/L	11.5		
T_J	Maximum Junction Temperature ⁽⁴⁾		+150	$^{\circ}\text{C}$	
	Recommended Operating Junction Temperature ⁽⁴⁾	-40	+130		
T_{STG}	Storage Temperature Range	-55	+150	$^{\circ}\text{C}$	
MOSFET Section					
V_{DGR}	Drain Gate Voltage ($R_{GS}=1M\Omega$)	500		V	
V_{GS}	Gate Source (GND) Voltage		± 30	V	
I_{DM}	Drain Current Pulsed ⁽⁵⁾	FSFR2100XS/L	32	A	
		FSFR1800XS/L	23		
		FSFR1700XS/L	20		
		FSFR1600XS/L	18		
I_D	Continuous Drain Current	FSFR2100XS/L	$T_C=25^{\circ}\text{C}$	10.5	A
			$T_C=100^{\circ}\text{C}$	6.5	
		FSFR1800XS/L	$T_C=25^{\circ}\text{C}$	7.0	
			$T_C=100^{\circ}\text{C}$	4.5	
		FSFR1700XS/L	$T_C=25^{\circ}\text{C}$	6.0	
			$T_C=100^{\circ}\text{C}$	3.9	
FSFR1600XS/L	$T_C=25^{\circ}\text{C}$	4.5			
	$T_C=100^{\circ}\text{C}$	2.7			
Package Section					
Torque	Recommended Screw Torque		5~7	kgf-cm	

Notes:

- Per MOSFET when both MOSFETs are conducting.
- The maximum value of the recommended operating junction temperature is limited by thermal shutdown.
- Pulse width is limited by maximum junction temperature.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ _{JC}	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	FSFR2100XS/L	10.44
		FSFR1800XS/L	10.68
		FSFR1700XS/L	10.79
		FSFR1600XS/L	10.89
			°C/W

Electrical Characteristics

T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Section						
BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D =200μA, T _A =25°C	500			V
		I _D =200μA, T _A =125°C		540		
R _{DS(ON)}	On-State Resistance	FSFR2100XS/L V _{GS} =10V, I _D =6.0A		0.41	0.51	Ω
		FSFR1800XS/L V _{GS} =10V, I _D =3.0A		0.77	0.95	
		FSFR1700XS/L V _{GS} =10V, I _D =2.0A		1.00	1.25	
		FSFR1600XS/L V _{GS} =10V, I _D =2.25A		1.25	1.55	
t _{rr}	Body Diode Reverse Recovery Time ⁽⁶⁾	FSFR2100XS/L V _{GS} =0V, I _{Diode} =10.5A, dI _{Diode} /dt=100A/μs		120		ns
		FSFR1800XS/L V _{GS} =0V, I _{Diode} =7.0A, dI _{Diode} /dt=100A/μs		160		
		FSFR1700XS/L V _{GS} =0V, I _{Diode} =6.0A, dI _{Diode} /dt=100A/μs		160		
		FSFR1600XS/L V _{GS} =0V, I _{Diode} =4.5A, dI _{Diode} /dt=100A/μs		90		
Supply Section						
I _{LK}	Offset Supply Leakage Current	HV _{CC} =V _{CTR} =500V			50	μA
I _{qHVCC}	Quiescent HV _{CC} Supply Current	(HV _{CC} UV+) - 0.1V		50	120	μA
I _{qLVCC}	Quiescent LV _{CC} Supply Current	(LV _{CC} UV+) - 0.1V		100	200	μA
I _{oHVCC}	Operating HV _{CC} Supply Current (RMS Value)	f _{OSC} =100KHz		6	9	mA
		No Switching		100	200	μA
I _{oLVCC}	Operating LV _{CC} Supply Current (RMS Value)	f _{OSC} =100KHz		7	11	mA
		No Switching		2	4	mA

Continued on the following page...

Electrical Characteristics (Continued)

 $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
UVLO Section						
LV _{CC} UV+	LV _{CC} Supply Under-Voltage Positive Going Threshold (LV _{CC} Start)		11.2	12.5	13.8	V
LV _{CC} UV-	LV _{CC} Supply Under-Voltage Negative Going Threshold (LV _{CC} Stop)		8.9	10.0	11.1	V
LV _{CC} UVH	LV _{CC} Supply Under-Voltage Hysteresis			2.50		V
HV _{CC} UV+	HV _{CC} Supply Under-Voltage Positive Going Threshold (HV _{CC} Start)		8.2	9.2	10.2	V
HV _{CC} UV-	HV _{CC} Supply Under-Voltage Negative Going Threshold (HV _{CC} Stop)		7.8	8.7	9.6	V
HV _{CC} UVH	HV _{CC} Supply Under-Voltage Hysteresis			0.5		V
Oscillator & Feedback Section						
V _{RT}	V-I Converter Threshold Voltage		1.5	2.0	2.5	V
f _{OSC}	Output Oscillation Frequency	R _T =5.2KΩ	94	100	106	KHz
DC	Output Duty Cycle		48	50	52	%
f _{SS}	Internal Soft-Start Initial Frequency	f _{SS} =f _{OSC} +40kHz, R _T =5.2KΩ		140		KHz
t _{SS}	Internal Soft-Start Time		2	3	4	ms
Protection Section						
V _{CSSH}	Beginning Voltage to Discharge C _{SS}		0.9	1.0	1.1	V
V _{CSSL}	Beginning Voltage to Charge C _{SS} and Restart		0.16	0.20	0.24	V
V _{OVP}	LV _{CC} Over-Voltage Protection	LV _{CC} > 21V	21	23	25	V
V _{AOCP}	AOCP Threshold Voltage		-1.0	-0.9	-0.8	V
t _{BAO}	AOCP Blanking Time ⁽⁶⁾	V _{CS} < V _{AOCP}		50		ns
V _{OCP}	OCP Threshold Voltage		-0.64	-0.58	-0.52	V
t _{BO}	OCP Blanking Time ⁽⁶⁾	V _{CS} < V _{OCP}	1.0	1.5	2.0	μs
t _{DA}	Delay Time (Low Side) Detecting from V _{AOCP} to Switch Off ⁽⁶⁾			250	400	ns
T _{SD}	Thermal Shutdown Temperature ⁽⁶⁾		120	135	150	°C
Dead-Time Control Section						
D _T	Dead Time ⁽⁷⁾			350		ns

Notes:

6. This parameter, although guaranteed, is not tested in production.
7. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

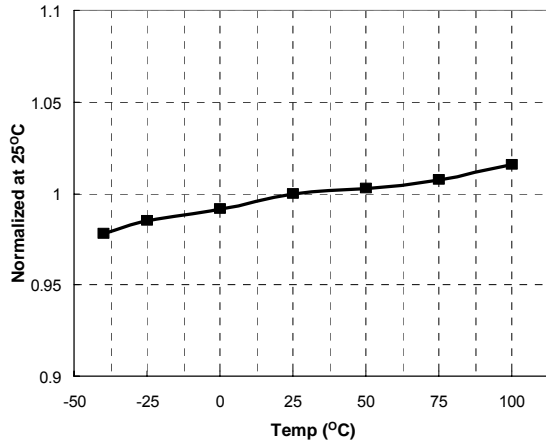


Figure 4. Low-Side MOSFET Duty Cycle vs. Temperature

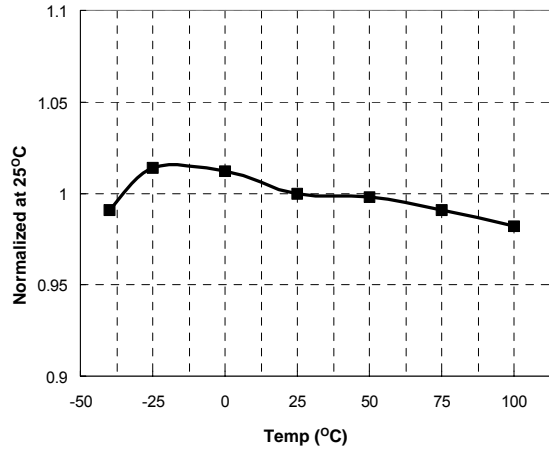


Figure 5. Switching Frequency vs. Temperature

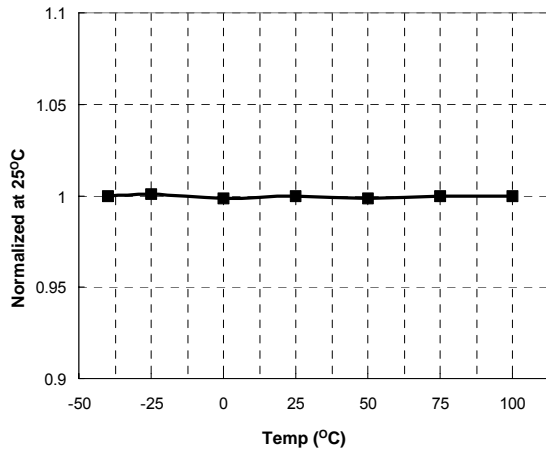


Figure 6. High-Side V_{CC} (HV_{CC}) Start vs. Temperature

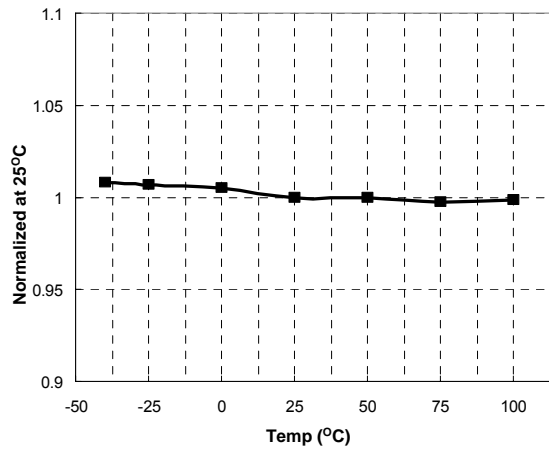


Figure 7. High-Side V_{CC} (HV_{CC}) Stop vs. Temperature

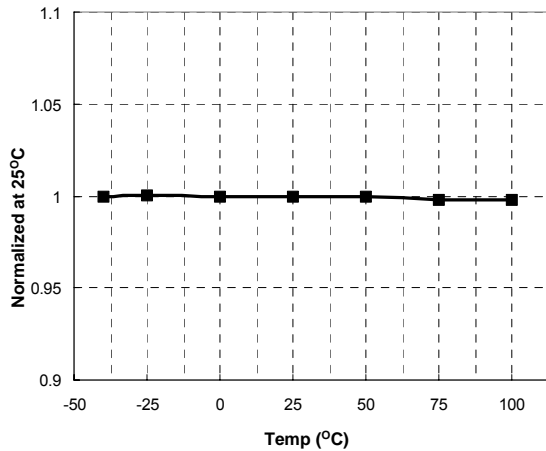


Figure 8. Low-Side V_{CC} (LV_{CC}) Start vs. Temperature

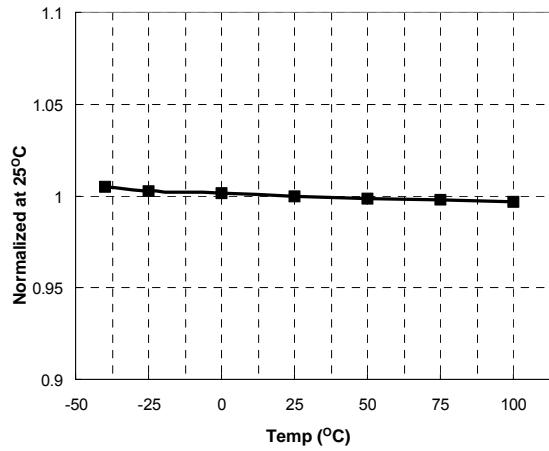


Figure 9. Low-Side V_{CC} (LV_{CC}) Stop vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

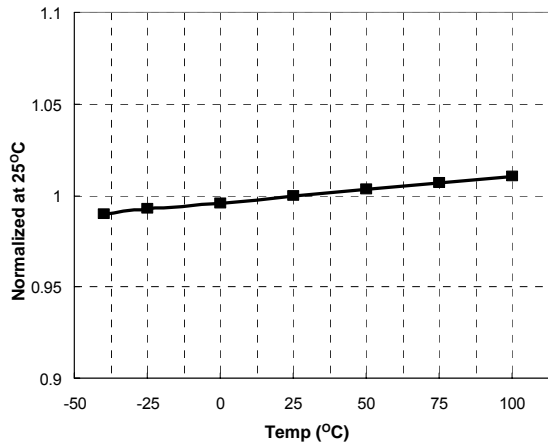


Figure 10. LVCC OVP Voltage vs. Temperature

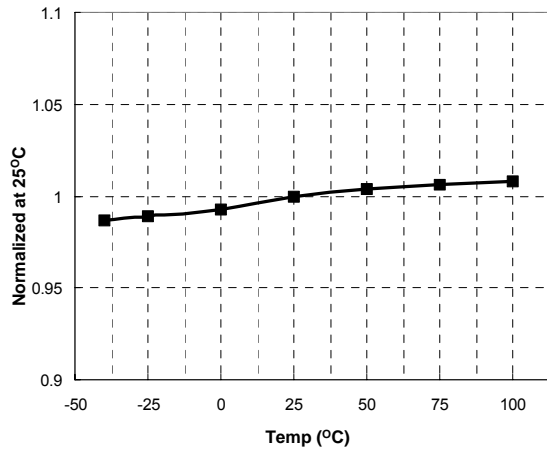


Figure 11. R_T Voltage vs. Temperature

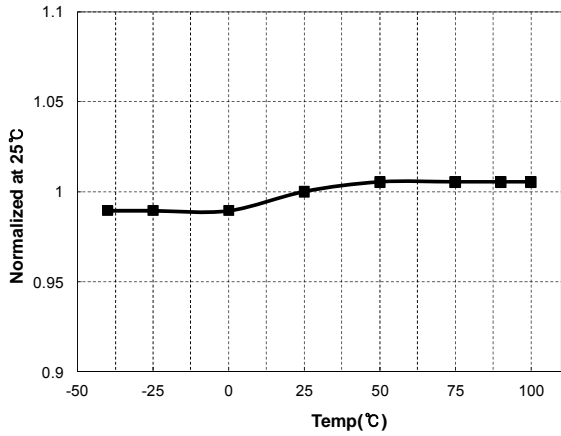


Figure 12. V_{CSL} vs. Temperature

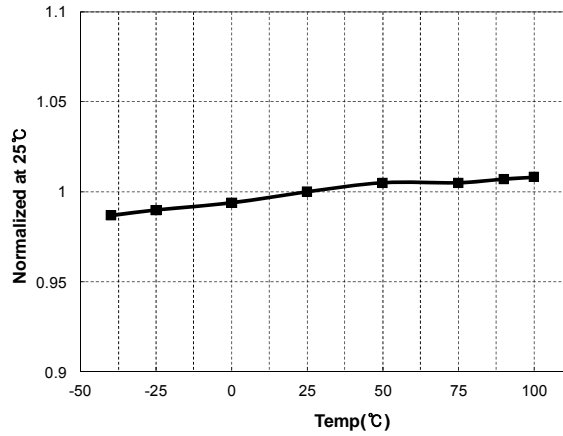


Figure 13. V_{CSH} vs. Temperature

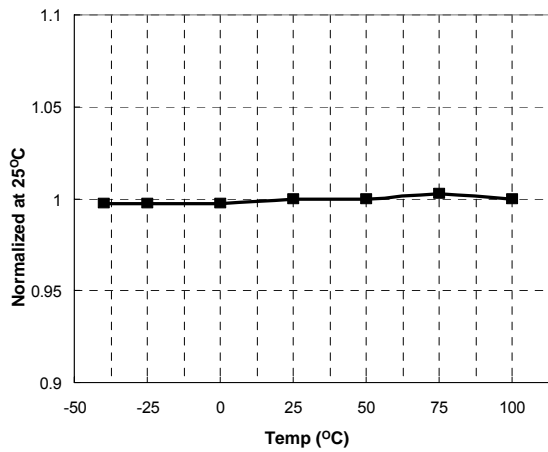


Figure 14. OCP Voltage vs. Temperature

Functional Description

1. Basic Operation. FSFR-XS series is designed to drive high-side and low-side MOSFETs complementarily with 50% duty cycle. A fixed dead time of 350ns is introduced between consecutive transitions, as shown in Figure 15.

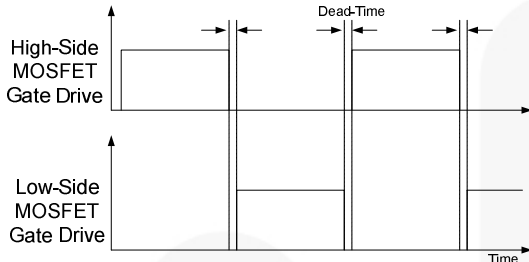


Figure 15. MOSFETs Gate Drive Signal

2. Internal Oscillator: FSFR-XS series employs a current-controlled oscillator, as shown in Figure 16. Internally, the voltage of R_T pin is regulated at 2V and the charging / discharging current for the oscillator capacitor, C_T , is obtained by copying the current flowing out of the R_T pin (I_{CTC}) using a current mirror. Therefore, the switching frequency increases as I_{CTC} increases.

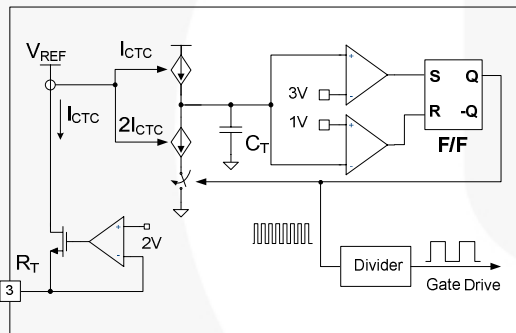


Figure 16. Current-Controlled Oscillator

3. Frequency Setting: Figure 17 shows the typical voltage gain curve of a resonant converter, where the gain is inversely proportional to the switching frequency in the ZVS region. The output voltage can be regulated by modulating the switching frequency. Figure 18 shows the typical circuit configuration for the R_T pin, where the opto-coupler transistor is connected to the R_T pin to modulate the switching frequency.

The minimum switching frequency is determined as:

$$f_{min} = \frac{5.2k\Omega}{R_{min}} \times 100(kHz) \quad (1)$$

Assuming the saturation voltage of opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f_{max} = \left(\frac{5.2k\Omega}{R_{min}} + \frac{4.68k\Omega}{R_{max}} \right) \times 100(kHz) \quad (2)$$

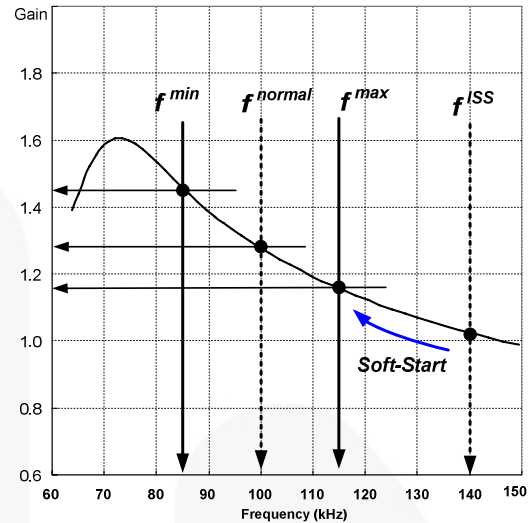


Figure 17. Resonant Converter Typical Gain Curve

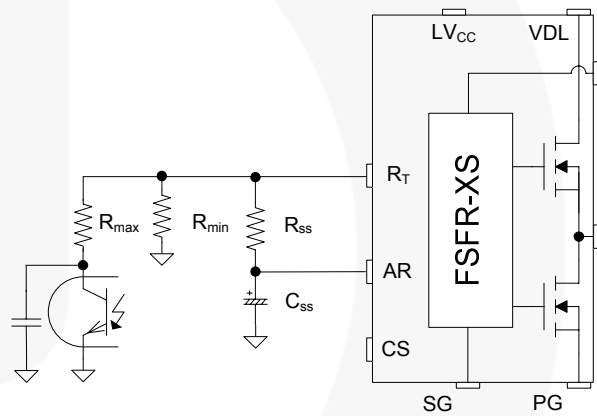


Figure 18. Frequency Control Circuit

To prevent excessive inrush current and overshoot of output voltage during startup, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, the soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established. The soft-start circuit is made by connecting R-C series network on the R_T pin, as shown in Figure 18. FSFR-XS series also has a 3ms internal soft-start to reduce the current overshoot during the initial cycles, which adds 40kHz to the initial frequency of the external soft-start circuit, as shown in Figure 19. The initial frequency of the soft-start is given as:

$$f^{ISS} = \left(\frac{5.2k\Omega}{R_{min}} + \frac{5.2k\Omega}{R_{SS}} \right) \times 100 + 40(kHz) \quad (3)$$

It is typical to set the initial frequency of soft-start two to three times the resonant frequency (f_0) of the resonant network. The soft-start time is three to four times the RC time constant. The RC time constant is:

$$\tau = R_{SS} \cdot C_{SS} \quad (4)$$

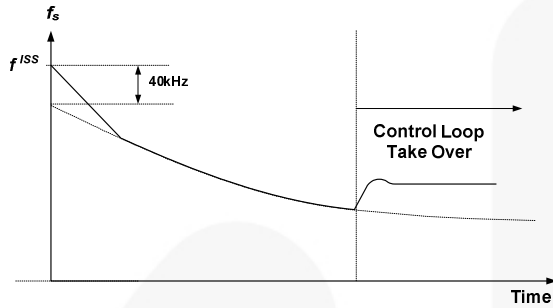


Figure 19. Frequency Sweeping of Soft-Start

4. Self Auto-Restart: The FSFR-XS series can restart automatically even though any built-in protections are triggered with external supply voltage. As can be seen in Figure 20 and Figure 21, once any protections are triggered, the M1 switch turns on and the V-I converter is disabled. C_{SS} starts to discharge until $V_{C_{SS}}$ across C_{SS} drops to $V_{C_{SSL}}$. Then, all protections are reset, M1 turns off, and the V-I converter resumes at the same time. The FSFR-XS starts switching again with soft-start. If the protections occur while $V_{C_{SS}}$ is under $V_{C_{SSL}}$ and $V_{C_{SSH}}$ level, the switching is terminated immediately, $V_{C_{SS}}$ continues to increase until reaching $V_{C_{SSH}}$, then C_{SS} is discharged by M1.

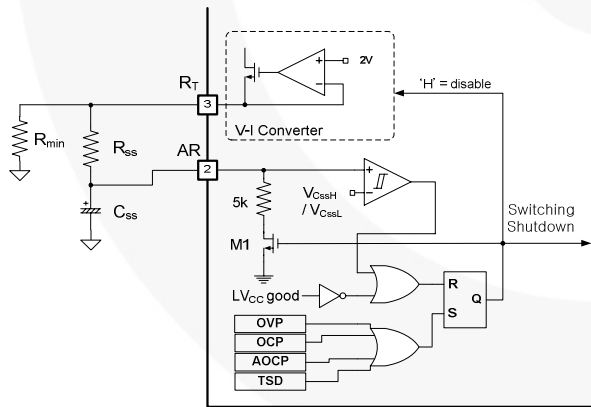


Figure 20. Internal Block of AR Pin

After protections trigger, FSFR-XS is disabled during the stop-time, t_{stop} , where $V_{C_{SS}}$ decreases and reaches to $V_{C_{SSL}}$. The stop-time of FSFR-XS can be estimated as:

$$t_{STOP} = C_{SS} \cdot \{(R_{SS} + R_{MIN}) \parallel 5k\Omega\} \quad (5)$$

The soft-start time, $t_{s/s}$ can be set as Equation (4).

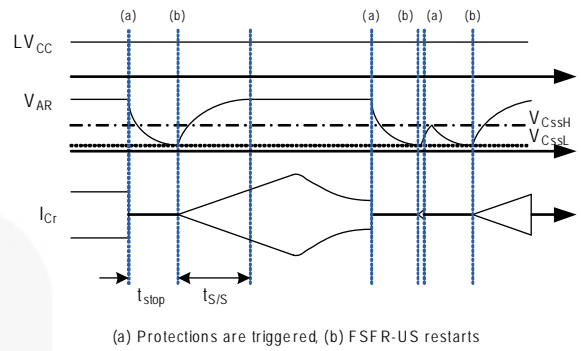


Figure 21. Self Auto-Restart Operation

5. Protection Circuits: The FSFR-XS series has several self-protective functions, such as Over-Current Protection (OCP), Abnormal Over-Current Protection (AOC), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). These protections are auto-restart mode protections, as shown in Figure 22.

Once a fault condition is detected, switching is terminated and the MOSFETs remain off. When LV_{CC} falls to the LV_{CC} stop voltage of 10V or AR signal is HIGH, the protection is reset. The FSFR-XS resumes normal operation when LV_{CC} reaches the start voltage of 12.5V.

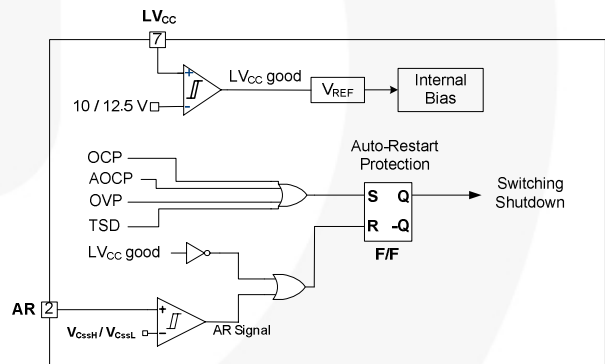


Figure 22. Protection Blocks

5.1 Over-Current Protection (OCP): When the sensing pin voltage drops below $-0.58V$, OCP is triggered and the MOSFETs remain off. This protection has a shutdown time delay of $1.5\mu s$ to prevent premature shutdown during startup.

5.2 Abnormal Over-Current Protection (AOC): If the secondary rectifier diodes are shorted, large current with extremely high di/dt can flow through the MOSFET before OCP is triggered. AOC is triggered without shutdown delay if the sensing pin voltage drops below $-0.9V$.

5.3 Over-Voltage Protection (OVP): When the LV_{CC} reaches 23V, OVP is triggered. This protection is used when auxiliary winding of the transformer to supply V_{CC} to the FPS™ is utilized.

5.4 Thermal Shutdown (TSD): The MOSFETs and the control IC in one package makes it easier for the control IC to detect the abnormal over-temperature of the MOSFETs. If the temperature exceeds approximately 130°C, thermal shutdown triggers.

6. Current Sensing Using a Resistor: FSFR-XS series senses drain current as a negative voltage, as shown in Figure 23 and Figure 24. Half-wave sensing allows low power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal.

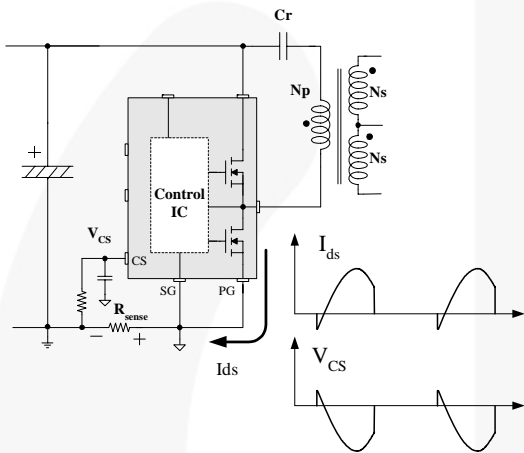


Figure 23. Half-Wave Sensing

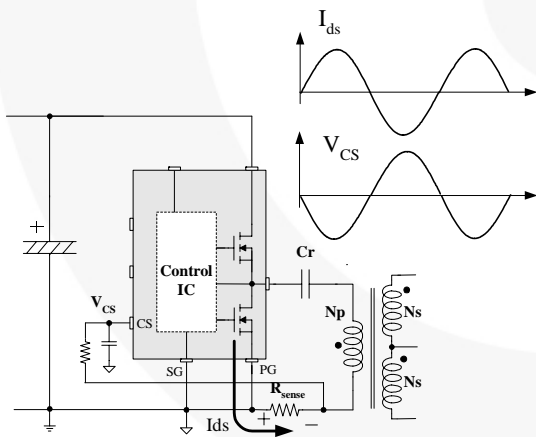


Figure 24. Full-Wave Sensing

7. PCB Layout Guidelines: Duty imbalance problems may occur due to the radiated noise from the main transformer, the inequality of the secondary side leakage inductances of main transformer, and so on. This is one of the reasons that the control components in the vicinity of R_T pin are enclosed by the primary current flow pattern on PCB layout. The direction of the magnetic field on the components caused by the primary current flow is changed when the high- and low-side MOSFET turn on by turns. The magnetic fields with opposite directions induce a current through, into, or out of the R_T pin, which makes the turn-on duration of each MOSFET different. It is strongly recommended to separate the control components in the vicinity of R_T pin from the primary current flow pattern on PCB layout. Figure 25 shows an example for the duty-balanced case.

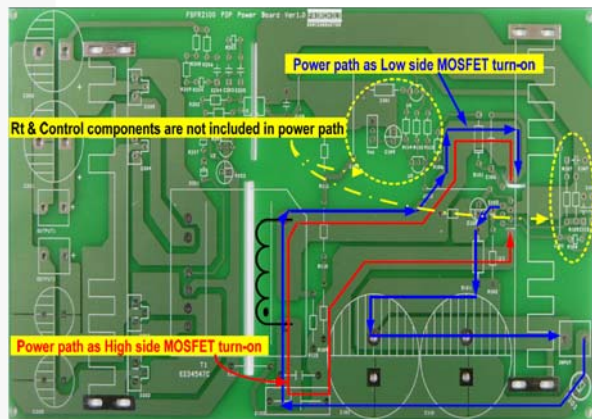
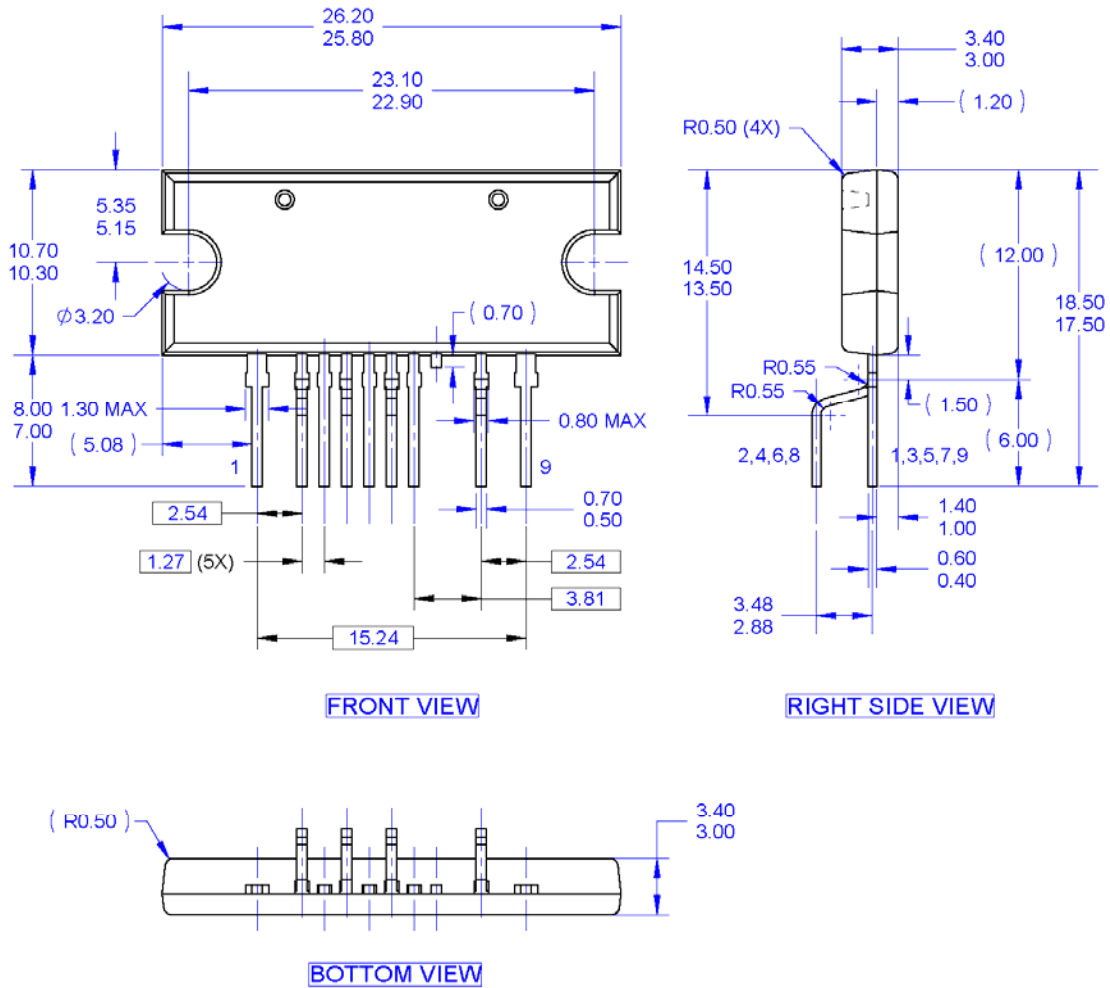


Figure 25. Example for Duty Balancing

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

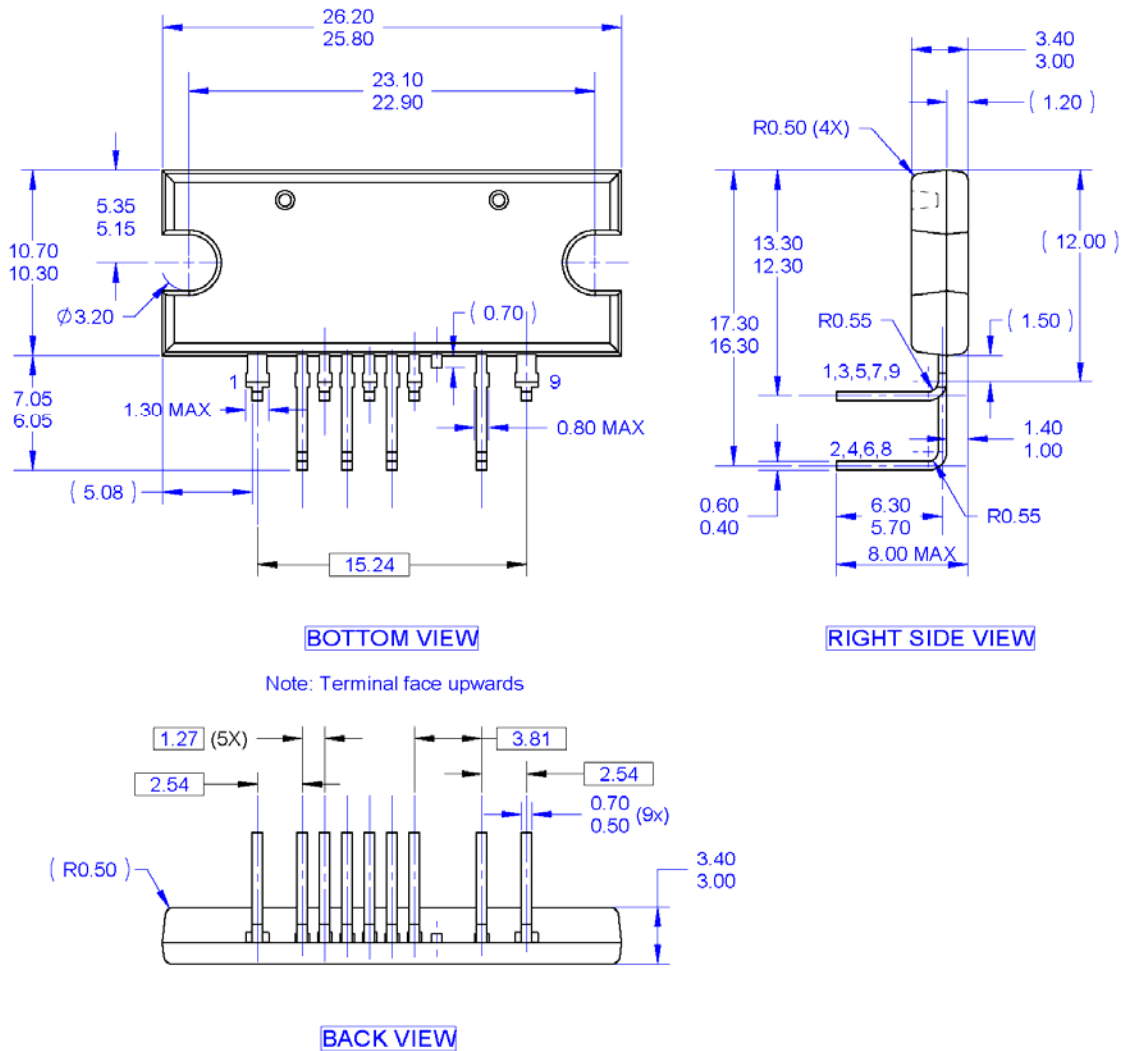
- A. THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- D. DRAWING FILE NAME: MOD09ACREV2

Figure 26. 9-Lead Single In-line Package (SIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.

Physical Dimensions



Note: Terminal face upwards

NOTES: UNLESS OTHERWISE SPECIFIED

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Figure 27. 9-Lead Single Inline Package (SIP) L-Forming

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