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DESCRIPTION

The EM78P247/447A/B/C is an 8-bit microprocessor with low-power, high speed CMOS technology. There are 4Kx13 bits Electical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides 1 Protect bit and 6 One-time Programmable Option bits to protect the OTP memory code from any external access as well as the user's options.

The OTP ROM will be incorporated into EM78P247/447A/B/C 8-bit microcontroller instead of it's original memory. The user's development program can be easily programmed into or verify from this OTP memory by using EMC OTP PROGRAMMER.

FEATURES

- Operating voltage range: 2.5V~5.5V
- Available in temperature range: 0°C~70°C
- Operating frequency range:
  Crystal Type: DC~20MHz at 5V DC~8MHz at 3V
  RC Type: DC~4MHz at 5V DC~4MHz at 3V
- 2Kx13 on chip ROM (EM78267A/B/C)
- 4Kx13 on chip ROM (EM78467A/B/C)
- 9 special function registers
- 148x8 general purpose registers (SRAM)
- 3 bi-directional tri-state I/O ports (20 I/O pins for EM78P247/447A) (24 I/O pins for EM78P247/447B) (22 I/O pins for EM78247/447C)
- 5 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt
- Selectable oscillator options:
  XTAL1 type (High frequency)
  XTAL2 type (32.768KHz)
  RC type
  External clock input
- Two oscillator periods per instruction cycle
- Power down mode
- Programmable wake up from sleep circuit on I/O ports
- Programmable free running on-chip watchdog timer
- Ten pull-up and wake-up pins
- Two open-drain pins
- Two R-option pins
- Interrupt function available
- 28 pin DIP, SOIC, SSOP (EM78P247/447A)
  28 pin SOIC (EM78P247/447C)

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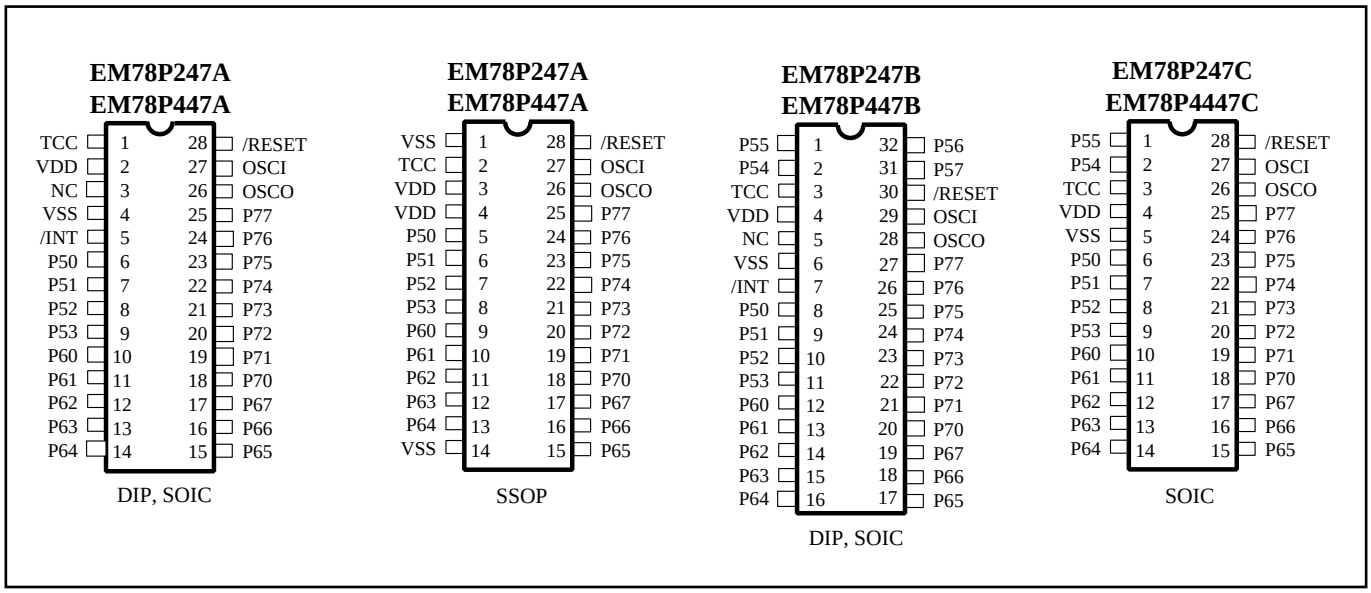
32 pin DIP, SOIC (EM78P247/447B)

- Function compatible with EM78247/447 except OTP memory inside

PIN ASSIGNMENTS



FUNCTIONAL BLOCK DIAGRAM

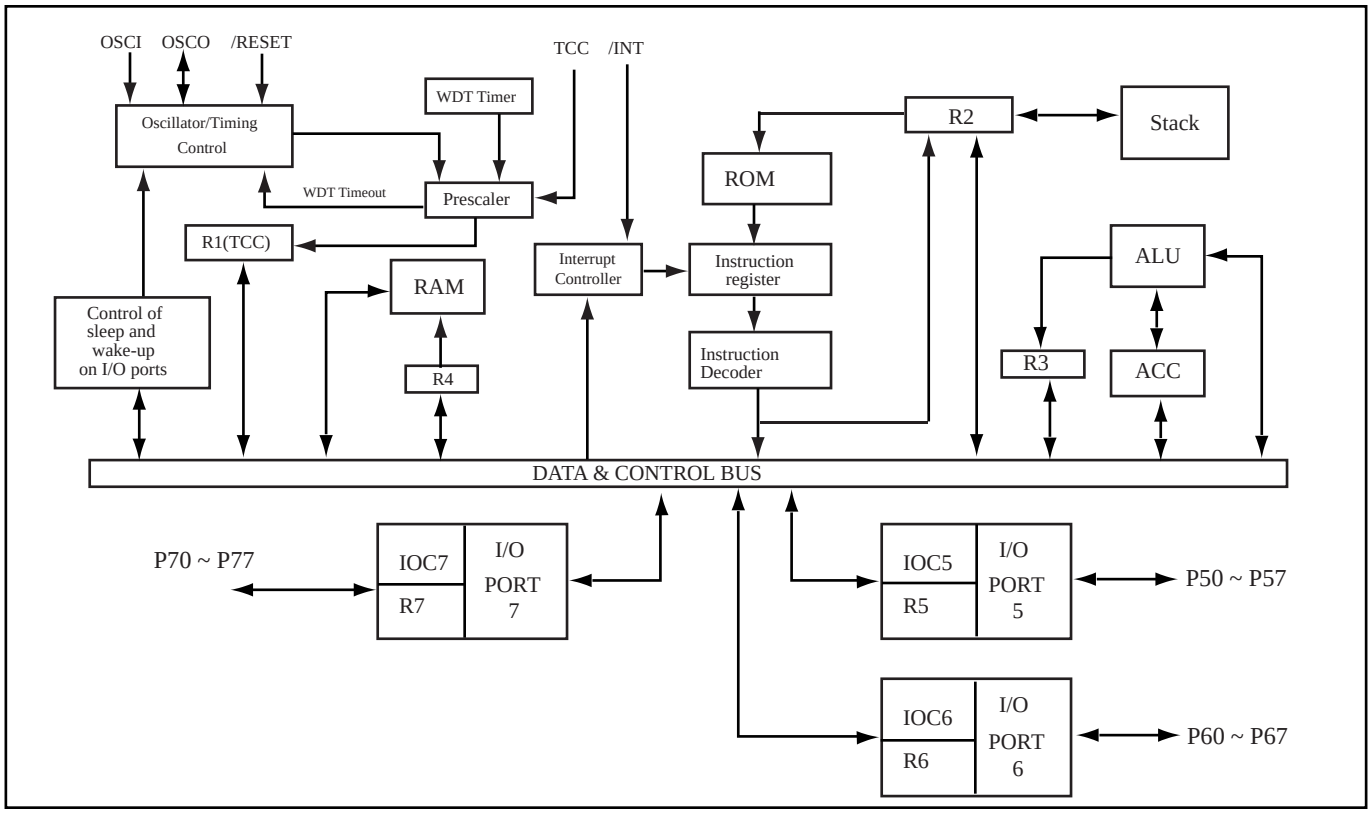


Fig. 2 Functional block diagram

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PIN DESCRIPTION

Symbol	Type	Function
OSCI	I	XTAL Type : Crystal input terminal or external clock input pin. RC type : RC oscillator input pin.
OSCO	I/O	XTAL type : output terminal for crystal oscillator or external clock input pin. RC type : clock output with a period of one instruction cycle is put on this pin.
TCC	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
$\overline{\text{RESET}}$	I	Schmitt trigger input pin. If this pin remains logic low, the controller is resset.
P70~P77	I/O	Port 7 is an 8-bit bi-directional I/O port. P74~P75 can be pulled-high internally by software control. P76~P77 can have open-drain output by software control. P70 and P71 are also the R-option pins.
P60~P67	I/O	Port 6 is an 8-bit bi-direction I/O port. They can be pulled-high internally by software control.
P50~P53	I/O	Low order 4 pins of Port 5. In case of EM78P447A, only low oder 4 pins are used in port 5.
P54~P57	I/O	High order 4 pins od Port 5. In case of EM78P447B, Port 5 is an 8-bit bi-directional I/O port.
$\overline{\text{INT}}$	I	Falling edge triggered interrupt input pin. Indicates an interrupt if interrupt is enabled. It has internal pull-up (50kΩ).
NC	-	no connection.
VDD	-	Power supply pin.
VSS	-	Ground pin.

FUNCTION DESCRIPTIONS

Operational Registers

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

- Increased by an external signal edge applied to TCC pin, or by the instruction cycle clock.
- Written and read by the program as any other register.

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R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 12 bits wide. The structure is depicted in Fig. 3.
- Generates 4Kx13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1K words long.
- R2 is set all "1"s upon a RESET condition.
- "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any location on one page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "MOV R2,A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of PC are cleared.
- "ADD R2,A" allows a relative address be added to the current PC, and the ninth and tenth bits of PC are cleared.
- Any instruction which writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",) (except "TBL") will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address be added to the current PC (R2+AR→2), and contents of the ninth and tenth bits (A8~A9) of PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256 locations on one program page.
- In case of EM78P247/447, the most significant bits (A10~A11) will be loaded with the contents of bits PS0~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any instruction which writes to R2.

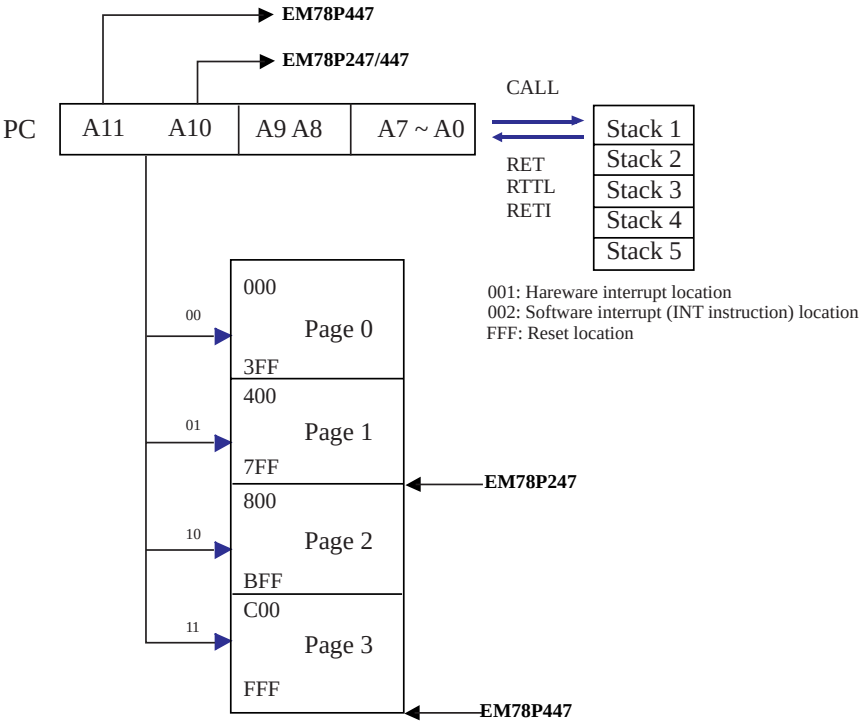

Fig. 3 Program counter organization

R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- **Bit 0 (C)** Carry flag
- **Bit 1 (DC)** Auxiliary carry flag
- **Bit 2 (Z)** Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- **Bit 3 (P)** Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- **Bit 4 (T)** Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT time-out.
- **Bits 5 (PS0) ~ 6 (PS1)** Page select bits. PS0~PS1 are used to preselect a program memory page. When executing a "JMP", "CALL", or other instruction which causes the program counter to be changed (e.g. MOV R2,A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter, selecting one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will be always to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- **Bit 7 (GP)** General read/write bit.

R4 (RAM Select Register)

- Bits 0~5 are used to select the registers (address: 00~3F) in the indirect addressing mode.
- Bits 6~7 determine which bank is activated among the 4 banks.
- If no indirect addressing is used, the RSR can be used as an 8-bit wide general purpose read/write register.
- See the configuration of the data memory in Fig. 4.

R5 (Port 5)

- EM78P247/447A: Only low order 4 bits are used in R5. The high order 4 bits of R5 will be read as "0".
- EM78P247/447B/C: All 8 bits are used in R5.

R6~R7 (Port 6 ~ Port 7)

- Two 8-bit I/O registers.

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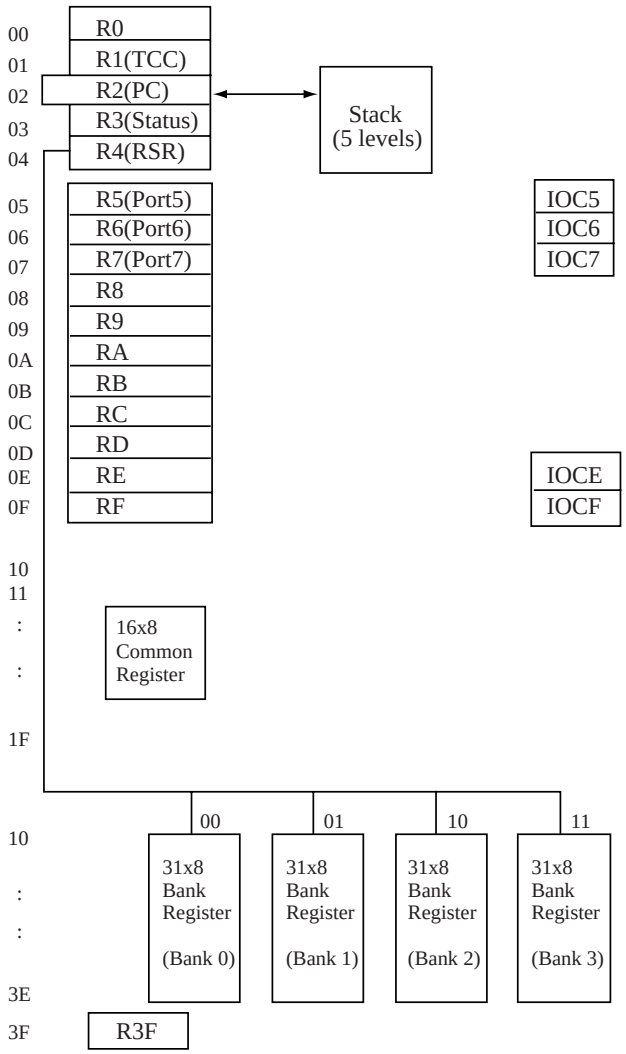

Fig. 4 Data memory configuration

R8~R1F, R20~R3E (General Purpose Register)

- R8~R1F, and R20~R3E (including Banks 0~3) are general purpose registers.

R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIF	-	-	TCIF

- **Bit 0 (TCIF)** TCC timer overflow interrupt flag. Set when TCC timer overflows, reset in software.
- **Bit 3 (EXIF)** External interrupt flag. Set by falling edge on /INT pin, reset in software.
- **Bits 1~2, 4~7** Not used.
- "1" means interrupt request, "0" means non-interrupt
- R3F can be cleared by instruction and cannot be set by instruction.

- IOCF is the interrupt mask register.
- Note that reading R3F by instruction will get the result of "logic AND" of R3F and IOCF.

Special Purpose Registers

A (Accumulator)

- Internal data transfer, or instruction operand holding
- It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
PHEN	INT	TS	TE	PAB	PSR2	PSR1	PSR0

- **Bit 0 (PSR0) ~ Bit 2 (PSR2)** TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- **Bit 3 (PAB)** Prescaler assignment bit.
  0: TCC
  1: WDT
- **Bit 4 (TE)** TCC signal edge
  0: increment from low to high transition on TCC pin
  1: increment from high to low transition on TCC pin
- **Bit 5 (TS)** TCC signal source
  0: internal instruction cycle clock
  1: transition on TCC pin
- **Bit 6 (INT)** Interrupt enable flag which cannot be written by CONTW instruction.
  0: interrupt masked by DISI or hardware interrupt.
  1: interrupt enabled by ENI/RETI instruction.
- **Bit 7 (/PHEN)** I/O pin pull-high enable flag
  0: P60~P67 and P74~P75 have internal pull-high.
  1: pull-high is disabled.

• Bits 0~5, 7 of CONT register are readable and writable.

IOC5 ~ IOC7 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- IOC5 ~ IOC7 are three I/O direction control registers. In case of EM78P247/447A, only IOC7, IOC6 and lower four bits of IOC5 are used.

IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WTE	SLPC	ROC	-	-	$\overline{\text{WUE}}$

Bit 6 (ODE) Open-drain control bit.

0: Both P76 and P77 are normal I/O pins.

1: Both P76 and P77 pins have open-drain output.

ODE bit is readable and writable.

Bit 5 (WTE) Control bit used to enable Watchdog timer.

WTE bit is used only if the CODE Option bit WTC is "1". If WTC bit is "1", then WDT is disabled/enabled by WTE bit.

0: Disable WDT

1: Enable WDT

WTE bit is not used if the CODE Option bit WTC is "0". That is, if WTC bit is "0", WDT is always disabled no matter what the WTE bit is.

WTE bit is readable and writable.

Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared by software. SLPC is used to control the operation of oscillator. The oscillator is disabled (oscillator is stopped, the controller enters the SLEEP2 MODE) on high-to-low transition on SLPC bit and is enabled (the controller is awakened from SLEEP2 MODE) on low-to-high transition on SLPC bit. In order to ensure the stable output of the oscillator, once the oscillator is disabled and is enabled again, there is a delay for approximately 18 ms (oscillator start-up timer, OST) before the next instruction of program being executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit WTC is "0" or not. After waking up, the WDT is enabled if Code Option WTC is "1". The block diagram of SLEEP2 MODE and wake-up caused by input triggered is depicted in Fig. 5.

Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pin (P70, P71) to be read by the controller. Clearing ROC will disable the R-option function. If the R-option function is used, the user must connect the P71 pin or/and P70 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/ disconnected, the status of P70(P71) will be read as "0"/"1" when ROC is set to "1". Refer to Fig. 7(b). ROC bit is readable and writable.

Bit 0 (/WUE) Control bit used to enable wake-up function of P60~P67 and P74~P75.

0: Enable wake-up function

1: Disable wake-up function

WUE bit is readable and writable.

Bits 1~2, 7 Not used.

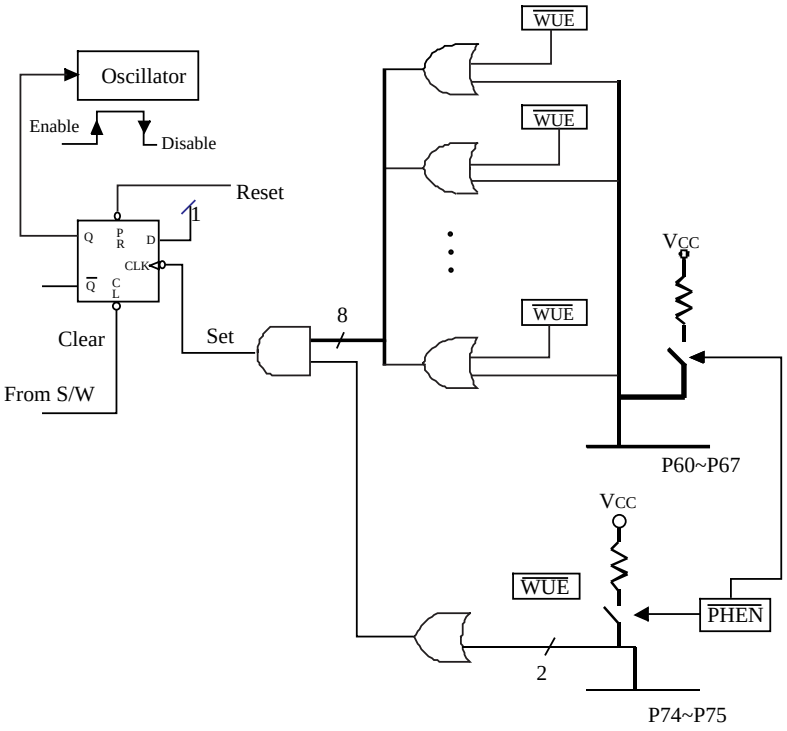

Fig. 5 Block diagram of sleep mode and wake-up circuits on I/O ports

IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIE	-	-	TCIE

Bit 0 (TCIE) TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

Bit 3 (EXIE) EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

Bits 1~2, 4~7 Not used.

- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. Refer to Fig. 9.
- IOCF Register is readable and writable.

TCC/WDT & Presacler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only

or WDT only at the same time and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. The prescaler will be cleared by instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, when assigned to WDT mode, will be cleared by the WDTC and SLEP instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by one in every instruction cycle (without prescaler). If TCC signal source is from external clock input, TCC will increase by 1 on every falling edge or rising edge of TCC pin.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming (if Code Option bit WTC is "1"). Refer to WTE bit of IOCE register. With no presacler, the WDT time-out period is approximately 18 ms.

I/O Ports

The I/O registers, Port 5 ~ Port 7, are bi-directional tri-state I/O ports. P60~P67, P74~P75 can have internal pull-high and wake-up function by software control. P76~P77 can have open-drain output by software control. P70~P71 are the R-option pins which are enabled by software. While R-option function is used, P70~P71 are recommended to be used as output pins. During the period of R-option being enabled, P70~P71 must be programmed as input pins. If external resistor is connected to P70(P71) for R-option function, the current consumption should be noticed in the applications that low power are concerned.

The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC7) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 7. Note that the source is different between the reading path of input and output pin while reading the I/O port.

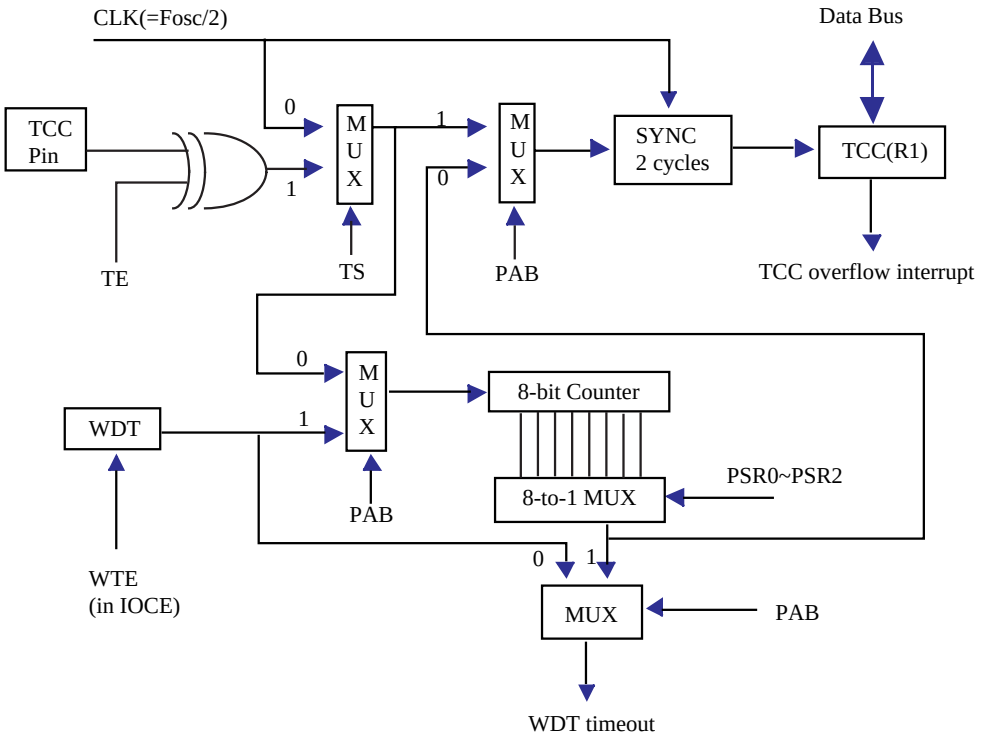

Fig. 6 Block diagram of TCC WDT

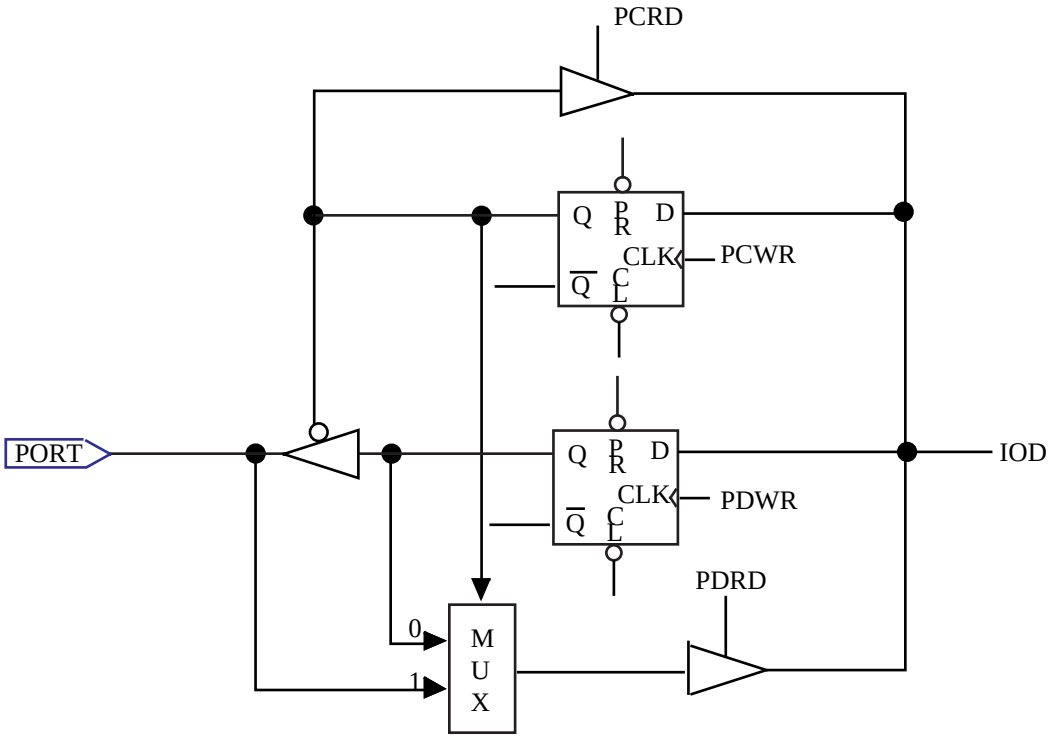

Fig. 7(a) The circuit of I/O port and I/O control register

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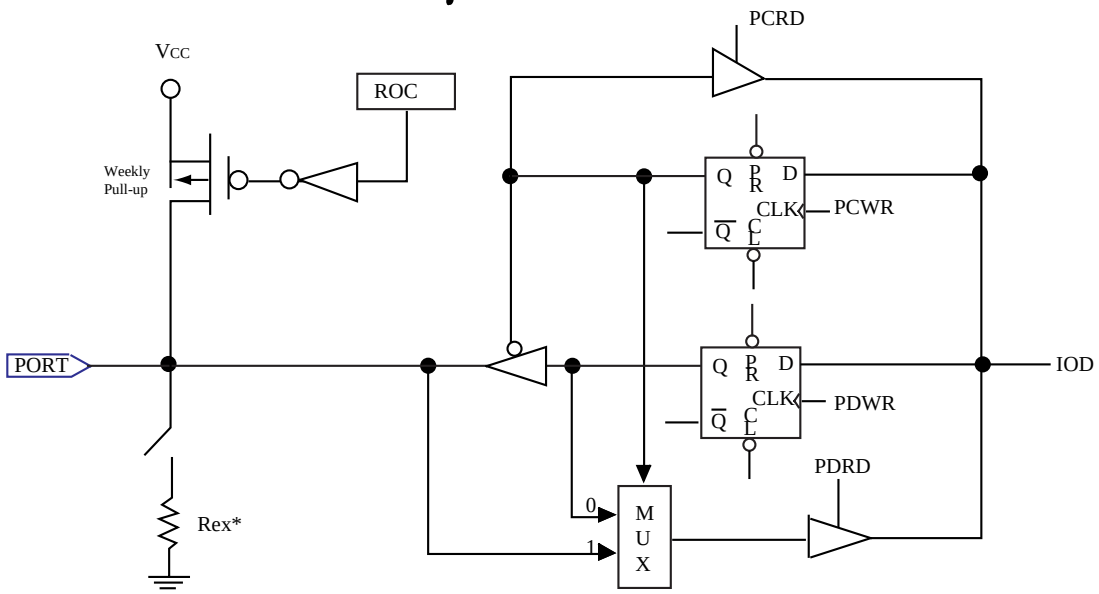

* The Rex is 560K ohm external resistor

Fig. 7(b) The circuit of I/O port with R-option (P70,P71)

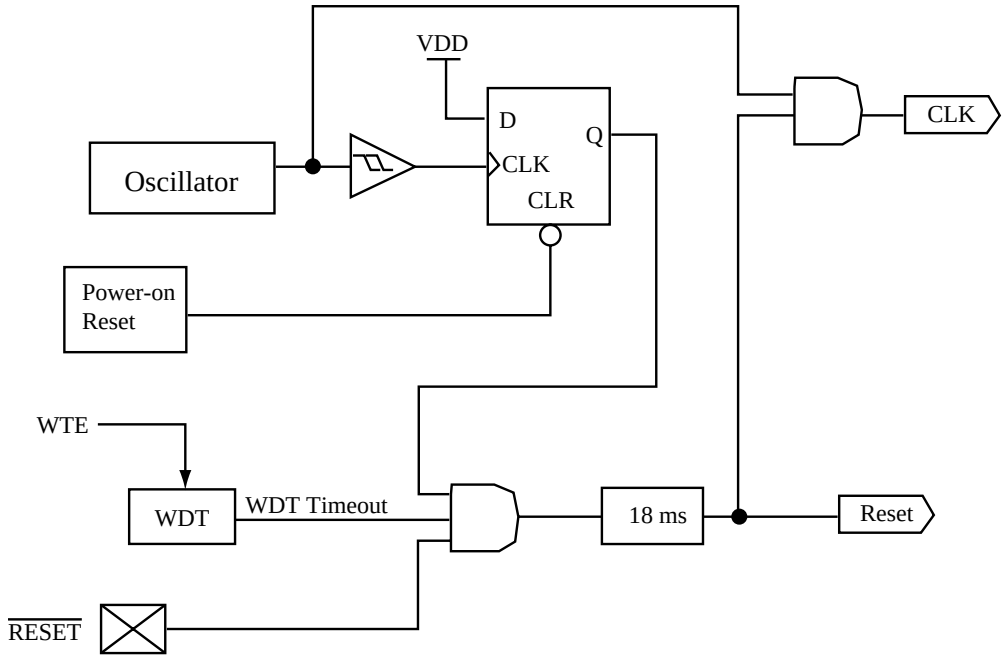

Fig. 8 Block diagram of Reset of controller

RESET and Wake-up

The RESET can be caused by

(1) Power on reset,

(2) /RESET pin input “low”, or

(3) WDT timeout. (if enabled)

The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1".
- When power on, bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is enabled if Code Option bit WTC is "1".
- The CONT register is set to all "1" except bit 6 (INT flag).
- Bits 3,6 of IOCE register are cleared, bits 0,4~5 of IOCE register are set to "1".
- Bits 0,3 of R3F and bits 0,3 of IOCF registers are cleared.

The sleep mode (power down mode) can be entered by executing the SLEP instruction (named as SLEEP1 MODE). While entering sleep mode, the WDT (if enabled) is cleared but keeping running. The controller can be awakened by

(1) WDT timeout (if enabled), or

(2) external reset input on /RESET pin.

The two cases will cause the controller to be reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78P247/447 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, named as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by

(a) input triggered, refer to Fig. 5. When wake-up, the controller will continue to execute program in-line. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, and P74~P75) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled if Code Option bit WTC is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(b) WDT time-out (if enabled) or external reset input on /RESET pin. When wake-up, will cause the controller reset.

Interrupt

The EM78P247/447 has the following interrupts:

(1) TCC overflow interrupt

(2) External interrupt (/INT).

R3F is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 001H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of

ENI instruction. Note that reading R3F will get the output of logic AND of R3F and IOCF. Refer to Fig. 9. The RETI instruction exits interrupt routine and enables the global interrupt (execution of ENI instruction).

When an interrupt is generated by INT instruction (when enabled), causes the next instruction to be fetched from address 002H.

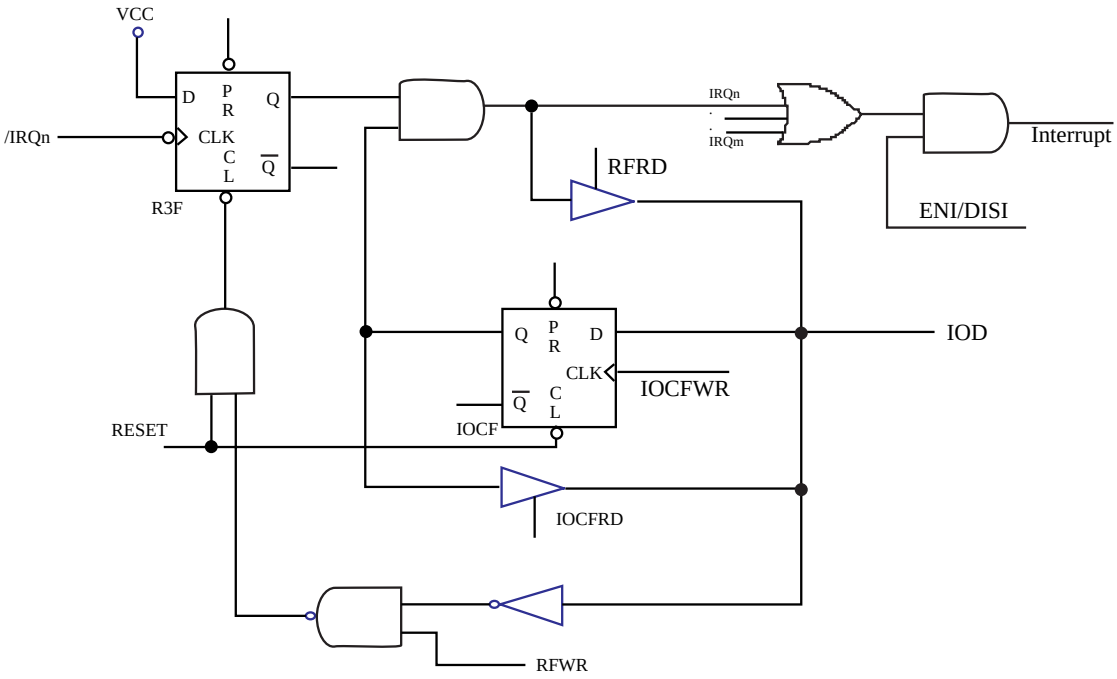

Fig. 9 Interrupt input circuit

Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consists of 2 oscillator periods), unless the program counter is changed by

(a) executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any instruction which write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2",).

(b) CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) tested to be true.

In these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1) . Every bit of any register can be set, cleared, or tested directly.

(2) . The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register. The symbol "R" represents a register designator which specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

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INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C

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INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note1> This instruction can operate on IOC5~IOC7, IOCE~IOCF only.

<Note2> This instruction is not recommended to operate on R3F.

<Note3> This instruction cannot operate on R3F.

CODE Option Register

The EM78P247/447 has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

12	11	10	9	8	7	6	5 -- 0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	-----

Bit 12 (MS): Oscillator type selection.

0: RC type

1: XTAL type

Bit 11 (ENWDTB): WDT option.

0: Enable

1: Disable

Bit 10 (CLKS): Clocks of each instruction cycle

0: Two clocks

1: Four clocks

Bit 9 (/PT): Protect bit
0: Protect enable
1: Protect disable

Bit 8 (HLF): XTAL frequency selection.
0: XTAL2 type (Low frequency, 32.768KHz)
1: XTAL1 type (High frequency)
This bit is useful only when Bit 0 (MS) is "1". When MS is "0", HLF must be "0".

Bit 7 (HLP): Power consumption selection
0: Low power
1: High power

Bit 6 (TYP): EM78P247/447A/B/C selection.
0: EM78P247/447B/C
1: EM78P247/447A

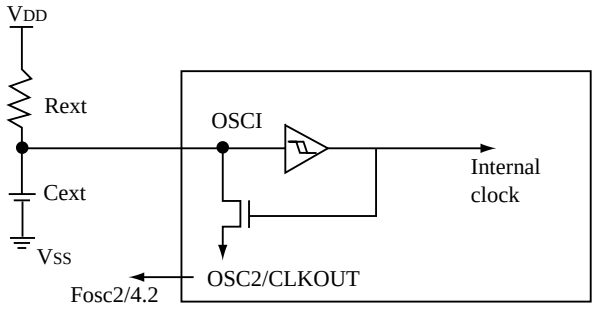
Bits 5~0: Not used. (DEFAULT "000000b").

Oscillator

The EM78P247/447 can be operated in three different oscillator options, there are RC type, low XTAL type and high XTAL type. The user can program three option bits (MS, HLF and HLO) to select one of these three modes If MS=0, HLF=0 RC type oscillator is chose and the frequency is determined by external Rext, Cext which device can offer lots of cost saving in timing insensitive applications.

If MS=1, HLF=0 HLP=0 low XTAL type oscillator is chose, in this case the oscillator is in low power and low frequency operation condition so the frequency should excess only 32.768 KHz and you got the bonus of low current consumption.

If MS=1, HLF=1 HLP=1 high XTAL type oscillator is chose, at this situation the oscillator is in high speed operation condition so the minim frequency should not less than 1 MHz. Because in this mode the current consumption is large than low power mode which in low frequency operation or battery environment should take into consideration.



In most case, the timing accuracy is not vary important. So the "RC oscillator" offers lots of cost savings. But the RC oscillator frequency is a function of the supply voltage, the resistor (Rext), capacitor (Cext) values and the operation temperature. In addition to, the oscillator frequency will vary little from unit to unit due to process parameter variation.

We strongly suggest user should take into account the frequency variation due to tolerance of Rext. Cext values and the voltage temperature effect.

Besides, furthermore stable consideration, the Cext should not less than 20pF and Rext should not great than 1M Ohm. In such case the PCB trace capacitance, package lead frame capacitance and leakage current will become frequency insensitive.

If the Rext become smaller the frequency become faster. However when Rext value less the 1K Ohm there may occur unstable condition due to the NMOS can't discharge the capacitance's current correctly the user should pay attention on it.

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ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

DC ELECTRICAL CHARACTERISTIC (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current for input pins	I_{IL1}	V_{IN} = V_{DD}, V_{SS}			±1	μA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Threshold Voltage	V_{IHT}	$\overline{RESET}$, TCC,$\overline{INT}$	0.85V_{DD}		V_{DD}	V
Input Low Threshold Voltage	V_{ILT}	$\overline{RESET}$, TCC,$\overline{INT}$	V_{SS}		0.15V_{DD}	V
Clock Input High Voltage	V_{IHX}	OSCI	3.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (Port 5,6,7)	V_{OH1}	I_{OH} = -11.0mA	2.4			V
Output Low Voltage (Port 5,6)	V_{OL1}	I_{OL} = 9.0mA			0.4	V
Output Low Voltage (Port 7 only)	V_{OL2}	I_{OL} = 14.0mA			0.4	V
Pull-high current	I_{PH}	Pull-high active, input pin at V_{SS}	-50	-100	-240	μA
Power down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled			10	μA
Operating supply current	I_{CC1}	$\overline{RESET}$='High', Fosc=4MHz (MS="1", HLF="1",CK2="0"), output pin floating			2	mA
Operating supply current	I_{CC2}	$\overline{RESET}$='High', Fosc=10MHz (MS="1", HLF="1",CK2="0"), output pin floating			5	mA
Operating supply current (V_{DD}=3.25V)	I_{CC3}	$\overline{RESET}$='High', Fosc=32.768KHz (MS="1", HLF="0",CK2="0"), output pin floating, WDT disabled			30	μA

AC ELECTRICAL CHARACTERISTICS (T_A=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time (CK2="0")	Tins	XTAL Type	100		DC	ns
		RC Type	500		DC	ns
TCC input period	Ttcc		(Tins+20)/N*			ns
Watchdog timer period	Twdt	Ta = 25°C		18		ms
Device reset hold period	Tdrh	Ta = 25°C		18		ms

* N= selected prescaler ratio.

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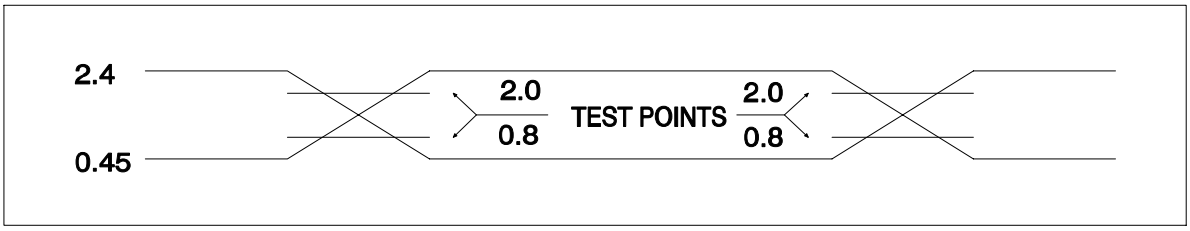
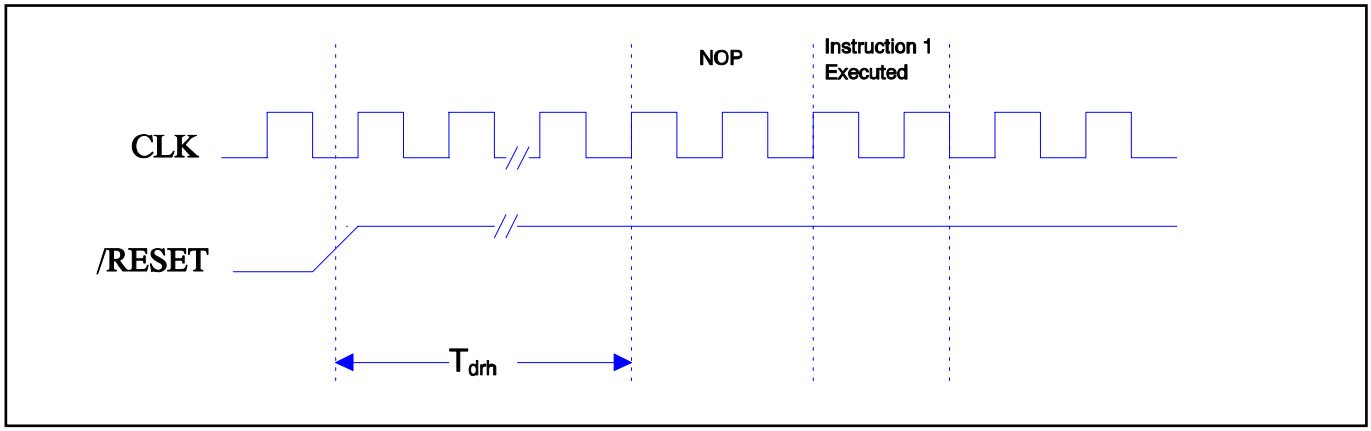
AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CK2="0")



TCC Input Timing (CK2="0")