SONY CXB1536Q-Y

8-bit Universal Counter with Preset and Master Reset

Description

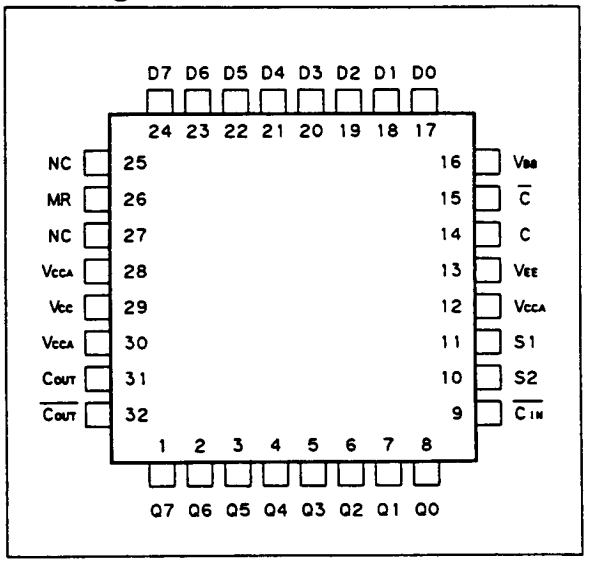
The CXB1536Q-Y is an ultra high speed monolithic ECL 8-bit Universal Counter.

Two Select (S1, S2) inputs select modes: up count, down count, preset and hold. Carry-in ($\overline{C_{IN}}$) and Carry out (C_{OUT}) is provided for the expansion of bit length.

Features

- Typical clock rate up to 1.0GHz
- Up/Down/Preset/Hold modes
- Differential clock input
- Reference voltage output for single ended input operation
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels
- Differential clock input

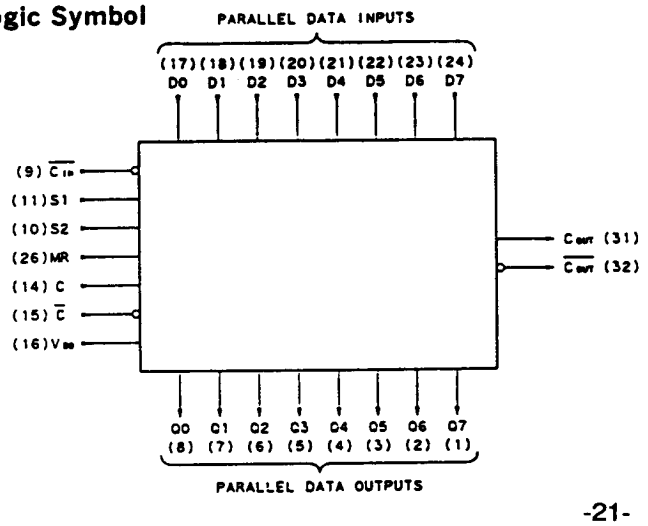
Pin Assignment



Pin Names

Dn	Parallel Data inputs
Sn	Select inputs
MR	Master direct Reset input
$\overline{C_{IN}}$	Carry input
C, $\overline{C}$	Clock inputs (positive edge trigger)
Qn	Parallel data outputs
C_{OUT}, $\overline{C_{OUT}}$	Carry outputs
V_{BB}	Reference voltage output
Vcc	Cirucit ground
V_{CCA}	Cirucit ground for output
V_{EE}	Negative voltage supply

Logic Symbol



DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−194	−143	−100	mA

AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item		Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time		T_{PLH}	C	Qn		770	1070	1400	ps
		T_{PHL}				770	1070	1400	
		T_{PLH}		C_{OUT}		850	1180	1540	
		T_{PHL}				910	1260	1640	
		T_{PLH}	$\overline{C_{IN}}$			1210	1660	2140	
		T_{PHL}				1260	1710	2190	
		T_{PLH}	MR			1130	1550	2000	
		T_{PHL}				1130	1550	2000	
		T_{PHL}		Qn		950	1290	1710	
Set up time		T_S	Dn, C	Qn		530			
			S1, C			900			
			S2, C			870			
			$\overline{C_{IN}}$, C	C_{OUT}		1150			
Hold time		T_h	C, Dn	Qn		200			
			C, S1			−350			
			C, S2			−350			
			C, $\overline{C_{IN}}$	C_{OUT}		−30			
Release time		T_R	MR, C	Qn		370			
Min. Pulse width		T_{PW}	MR			330			
Max. Clock frequency	Count up	f_{MAX}	C			0.8	1.2		GHz
	Count down					0.6	1.0		
Rise time		T_{TLH}			20% to 80%		550	730	ps
Fall time		T_{THL}					450	600	

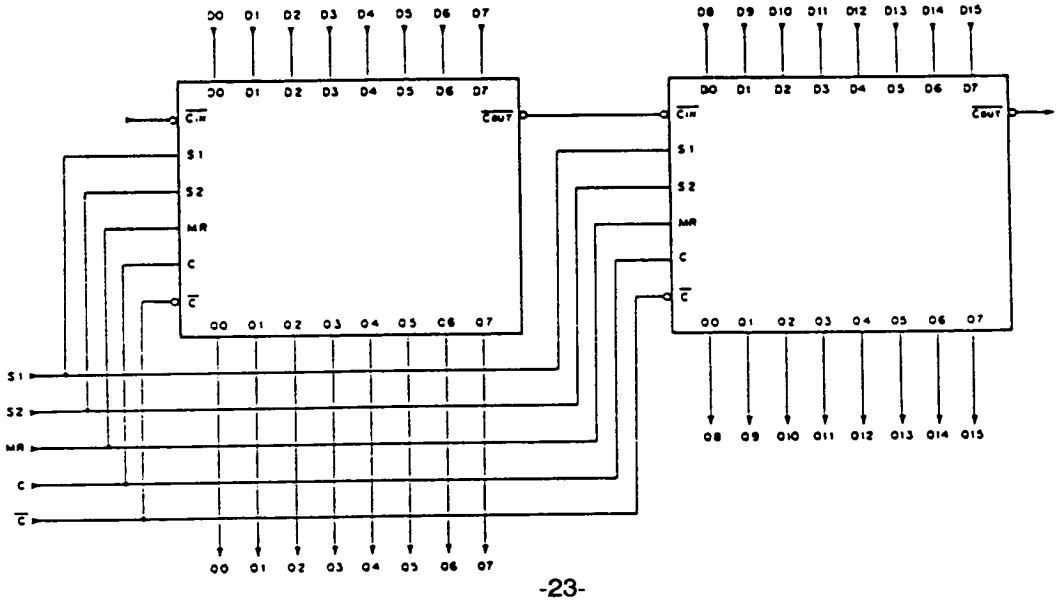
All output pins are left open except measured output pins.

Sequential Truth Table

Mode \ Pin	Inputs													Outputs								
	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7	$\overline{C_{IN}}$	CLK	MR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	$\overline{C_{OUT}}$
Preset	L	L	L	L	H	H	H	H	H	H	×	⎍	L	L	L	H	H	H	H	H	H	L
Count up	L	H	×	×	×	×	×	×	×	×	L	⎍	L	H	L	H	H	H	H	H	H	H
	L	H	×	×	×	×	×	×	×	×	L	⎍	L	L	H	H	H	H	H	H	H	H
	L	H	×	×	×	×	×	×	×	×	L	⎍	L	H	H	H	H	H	H	H	H	L
	L	H	×	×	×	×	×	×	×	×	H	×	L	H	H	H	H	H	H	H	H	H
Hold	H	H	×	×	×	×	×	×	×	×	×	×	L	H	H	H	H	H	H	H	H	H
Preset	L	L	H	H	L	L	L	L	L	L	×	⎍	L	H	H	L	L	L	L	L	L	L
Count down	H	L	×	×	×	×	×	×	×	×	L	⎍	L	L	H	L	L	L	L	L	L	H
	H	L	×	×	×	×	×	×	×	×	L	⎍	L	H	L	L	L	L	L	L	L	H
	H	L	×	×	×	×	×	×	×	×	L	⎍	L	L	L	L	L	L	L	L	L	L
	H	L	×	×	×	×	×	×	×	×	L	⎍	L	H	H	H	H	H	H	H	H	H
	H	L	×	×	×	×	×	×	×	×	H	×	L	H	H	H	H	H	H	H	H	H
Master reset	L	L	×	×	×	×	×	×	×	×	L	×	H	L	L	L	L	L	L	L	L	L
	L	L	×	×	×	×	×	×	×	×	H	×	H	L	L	L	L	L	L	L	L	L
	L	H	×	×	×	×	×	×	×	×	L	×	H	L	L	L	L	L	L	L	L	H
	L	H	×	×	×	×	×	×	×	×	H	×	H	L	L	L	L	L	L	L	L	H
	H	L	×	×	×	×	×	×	×	×	L	×	H	L	L	L	L	L	L	L	L	L
	H	L	×	×	×	×	×	×	×	×	H	×	H	L	L	L	L	L	L	L	L	H
	H	H	×	×	×	×	×	×	×	×	L	×	H	L	L	L	L	L	L	L	L	H
	H	H	×	×	×	×	×	×	×	×	H	×	H	L	L	L	L	L	L	L	L	H

H: HIGH voltage level
L: LOW voltage level
X: Don't care
⎍: Positive transition edge

Typical Application — 16bit Up/Down Counter



Block Diagram