FINAL

Am27C512

512 Kilobit (65,536 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — 55 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance available**
- **100% Flashrite programming**
  - — Typical programming time of 8 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, 32-pin TSOP, and PLCC packages**

GENERAL DESCRIPTION

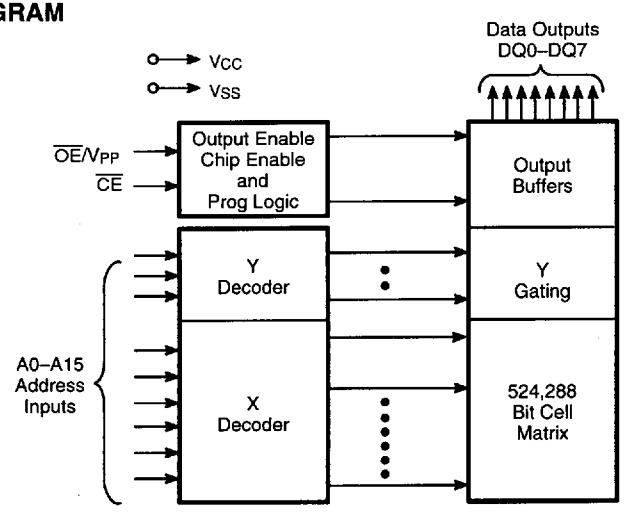
The Am27C512 is a 512 K-bit ultraviolet erasable programmable read-only memory. It is organized as 64K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages as well as plastic one time programmable (OTP) PDIP, TSOP, and PLCC packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C512 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in a typical programming time of 8 seconds.

BLOCK DIAGRAM



08140H-1

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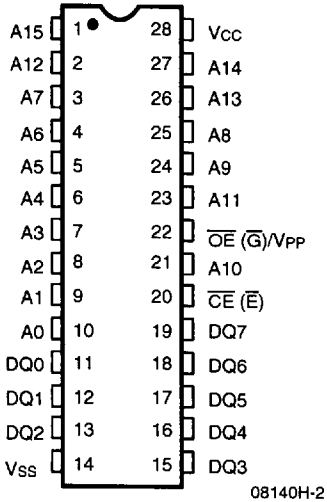
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C512						
Ordering Part No: V_{CC} ± 5%	-55						-255
V_{CC} ± 10%		-70	-90	-120	-150	-200	
Max Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	55	40	40	50	50	75	75

CONNECTION DIAGRAMS

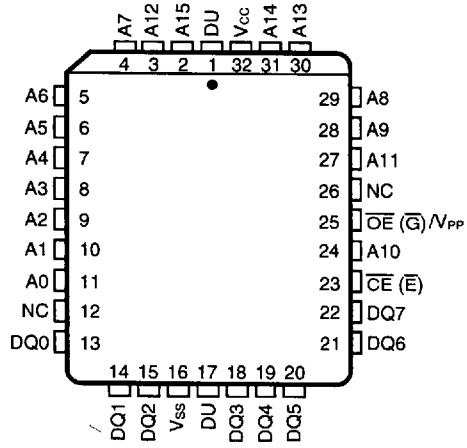
Top View

DIP



08140H-2

PLCC

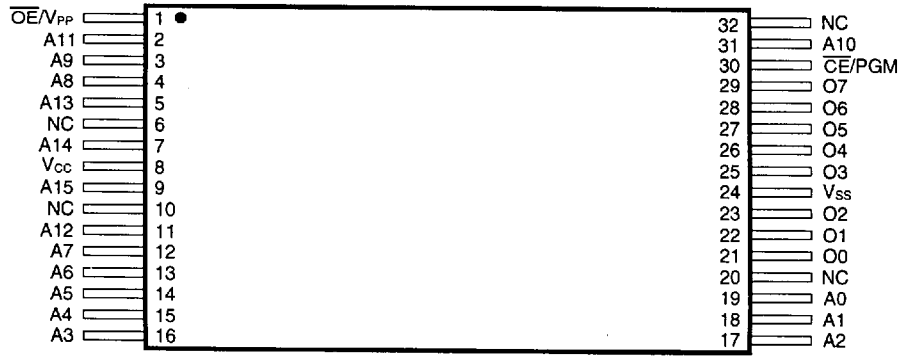


08140H-3

Notes:

1. JEDEC nomenclature is in parentheses.

TSOP*



08140H-4

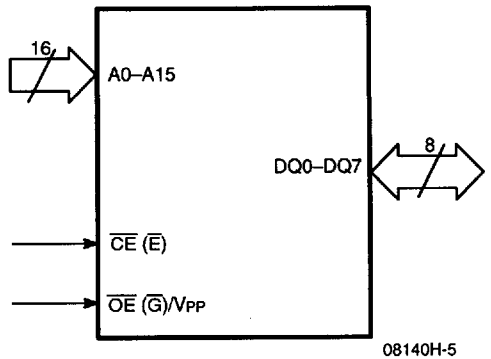
**Contact local AMD sales office for package availability.*

Standard Pinout

PIN DESIGNATIONS

A0–A15	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0–DQ7	=	Data Inputs/Outputs
DU	=	No External Connection (Do Not Use)
NC	=	No Internal Connection
$\overline{OE}$ ($\overline{G}$)/V_{PP}	=	Output Enable Input/ Program Voltage Input
V_{CC}	=	V_{CC} Supply Voltage
V_{SS}	=	Ground

LOGIC SYMBOL

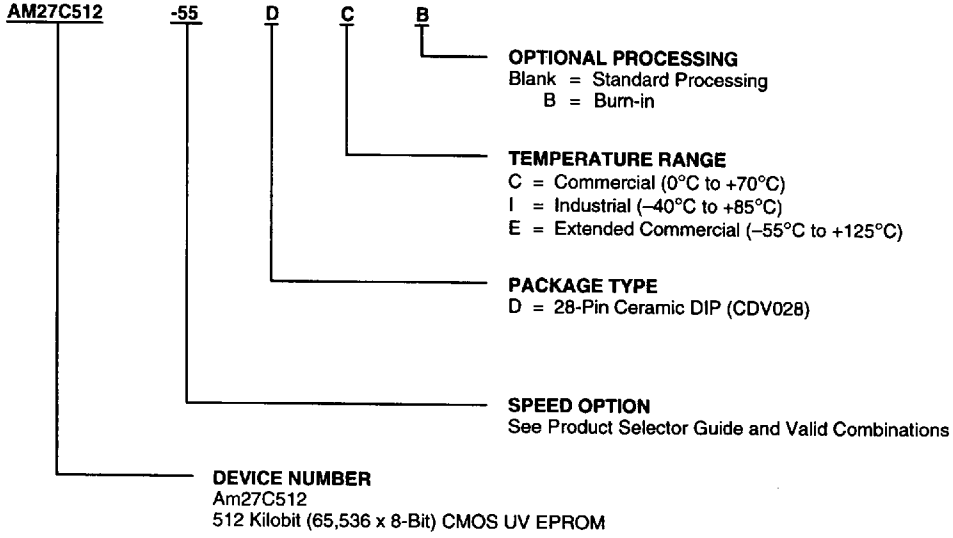


08140H-5

ORDERING INFORMATION

UV EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C512-55	DC
AM27C512-70	DC, DCB
AM27C512-90	
AM27C512-120	
AM27C512-150	DC, DCB, DI, DIB
AM27C512-200	DE, DEB
AM27C512-250	
AM27C512-255	DC, DCB, DI, DIB

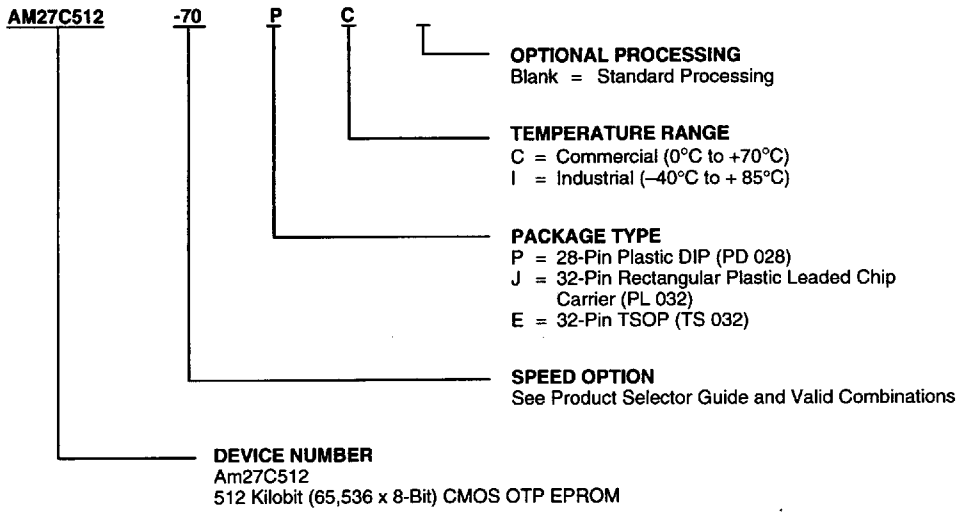
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27C512-70	PC, JC, EC PI, JI, EI
AM27C512-90	
AM27C512-120	
AM27C512-150	
AM27C512-200	
AM27C512-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Erasing the Am27C512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C512 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C512. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C512 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C512 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C512

Upon delivery or after each erasure the Am27C512 has all 524,288 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C512 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the $\overline{OE}/V_{PP}$ and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C512. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C512 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C512 may be common. A TTL low-level program pulse applied to an Am27C512 $\overline{CE}$ input and $\overline{OE}/V_{PP}$ = 12.75 V ± 0.25 V, will program that Am27C512. A high-level $\overline{CE}$ input inhibits the other Am27C512 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{CE}$ at V_{IL} and $\overline{OE}/V_{PP}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C512.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the Am27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27C512, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The Am27C512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}/V_{PP}$	A0	A9	Outputs
Read		V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	Hi-Z
Program		V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	91H

Notes:

1. *$V_H = 12.0 \pm 0.5$ V*
2. *X = Either V_{IH} or V_{IL}*
3. *A1–A8 = A10–A15 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- OTP Products ..... –65°C to +125°C
- All Other Products ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Voltage with Respect To V_{SS}
- All pins except A9,
  V_{PP}, V_{CC} ..... –0.6 V to V_{CC} + 0.5 V
- A9 and V_{PP} ..... –0.6 V to +13.5 V
- V_{CC} ..... –0.6 V to +7.0 V

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During transitions, the inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *For A9 and V_{PP} the minimum DC input is –0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Ambient Temperature (T_A) ..... 0°C to +70°C

Industrial (I) Devices
- Ambient Temperature (T_A) ..... –40°C to +85°C

Extended Commercial (E) Devices
- Ambient Temperature (T_A) .... –55°C to +125°C

Supply Read Voltages
- V_{CC} for Am27C512-XX5 ..... +4.75 V to +5.25 V
- V_{CC} for Am27C512-XX0 ..... +4.50 V to +5.50 V
- V_{CC} for Am27C512-55 ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA,			30	mA
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27C512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

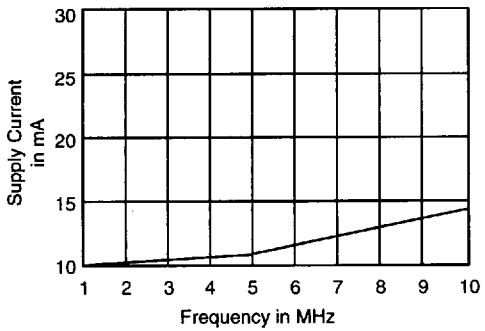


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

08140H-6

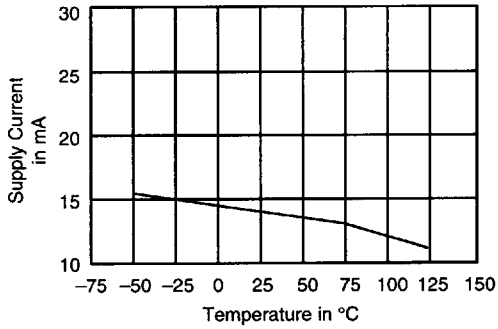


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

08140H-7

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	TS 032		CDV028		PL 032		PD 028		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	10	12	10	12	9	12	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	14	10	13	9	12	6	10	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, 4 and 5)

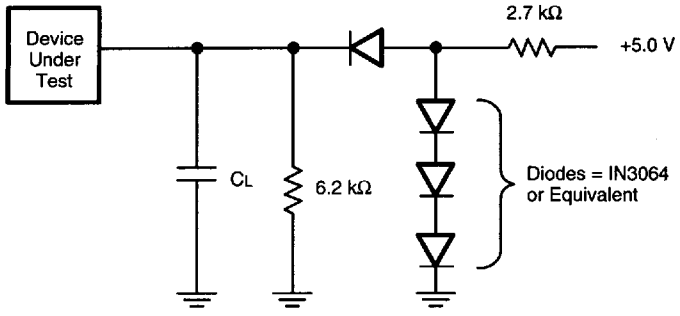
Parameter Symbols		Parameter Description	Test Conditions		Am27C512							Unit
JEDEC	Standard				-55	-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	55	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min	–	–	–	–	–	–	–	
				Max	35	40	40	50	50	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	–	–	–	–	–	–	–	
				Max	25	25	30	30	30	30	30	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	0	0	
				Max	–	–	–	–	–	–	–	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:** The Am27C512 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and C_L = 100 pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: 0.8 V and 2 V inputs and outputs

   For the Am27C512-55:
   Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs

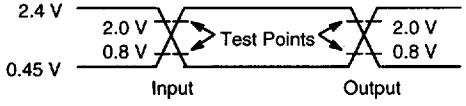
SWITCHING TEST CIRCUIT



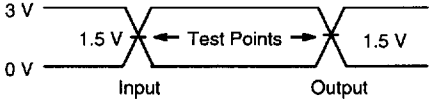
C_L = 100 pF including jig capacitance (30 pF for -55)

08140H-8

SWITCHING TEST WAVEFORM



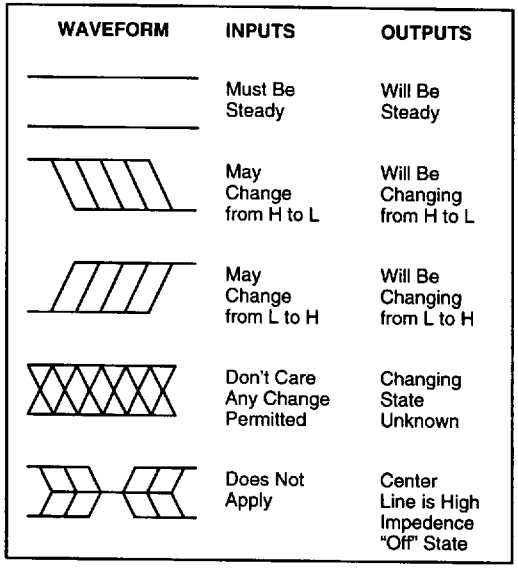
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08140H-9

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55 device.

KEY TO SWITCHING WAVEFORMS



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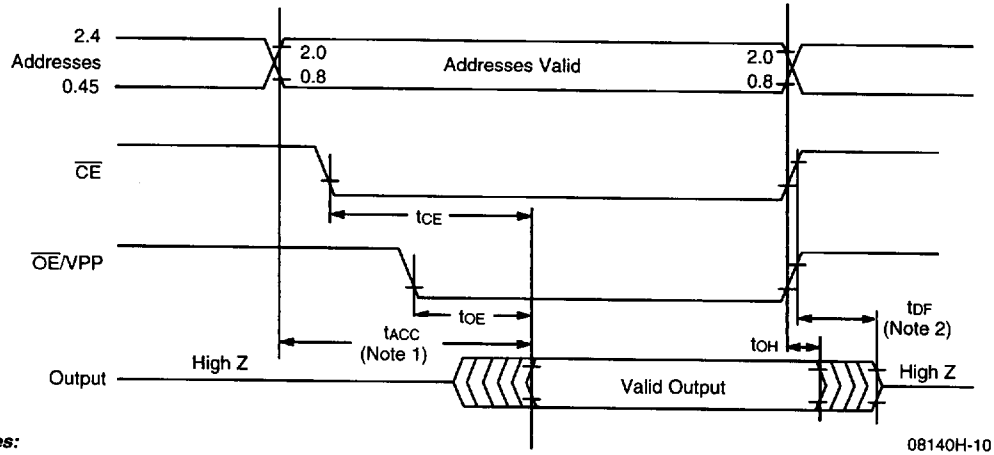
SWITCHING WAVEFORMS



08140H-10

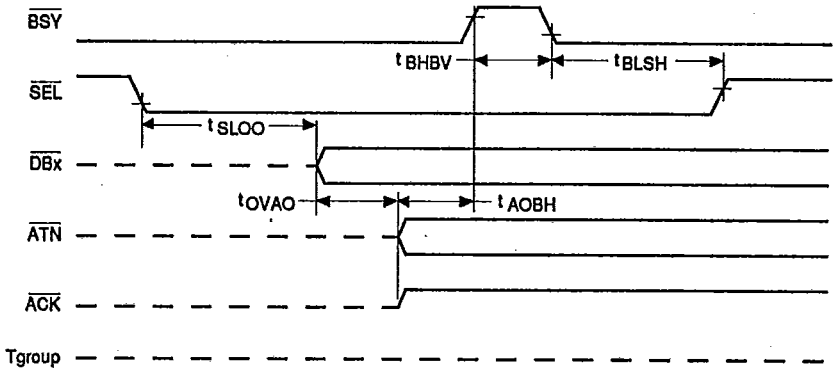
Notes:

1. *$\overline{OE}$/V_{PP} may be delayed up to t_{ACC}–t_{OE} after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.*

T-52-33-27

SELECTING A TARGET (AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SLOO}	$\overline{SEL}$ Out Low to "OR-ED" ID Out	1.2		us
t_{OVAO}	"OR-ED" ID Out Valid to $\overline{ACK}$, $\overline{ATN}$ Out	100		ns
t_{AOBH}	$\overline{ACK}$, $\overline{ATN}$ Out Valid to $\overline{BSY}$ Out High	100		ns
t_{BHBV}	$\overline{BSY}$ Out High to $\overline{BSY}$ In Low Valid	400		ns
t_{BLSH}	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns



NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

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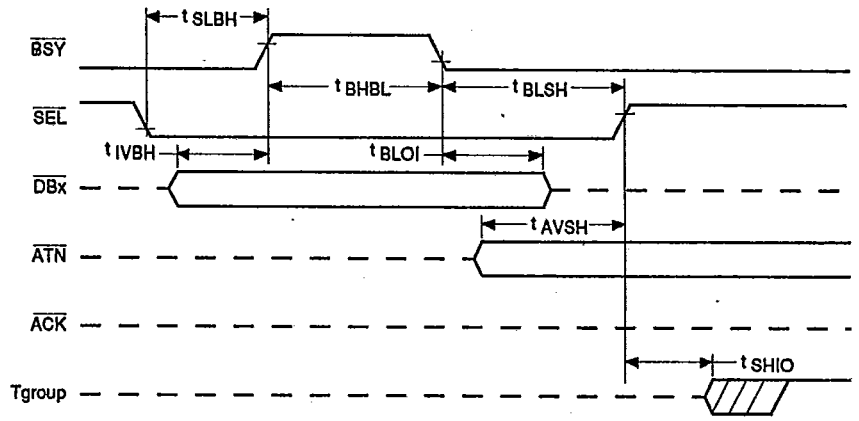
RESPONSE TO SELECTION (AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SLBH}	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
t_{IVBH}	"OR-ED" ID Valid In to $\overline{BSY}$ In High	0		ns
t_{BHBL}	$\overline{SEL}$ Low , ID Valid , $\overline{BSY}$ High to $\overline{BSY}$ Low	0.4	200	us
t_{BLOI}	$\overline{BSY}$ Out Low to "OR-ED" ID Invalid In	0		ns
t_{BLSH}	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
t_{AVSH}	$\overline{ATN}$ Valid In to $\overline{SEL}$ In High	0		ns
t_{SHIO}	$\overline{SEL}$ In High to Tgroup Out	100		ns



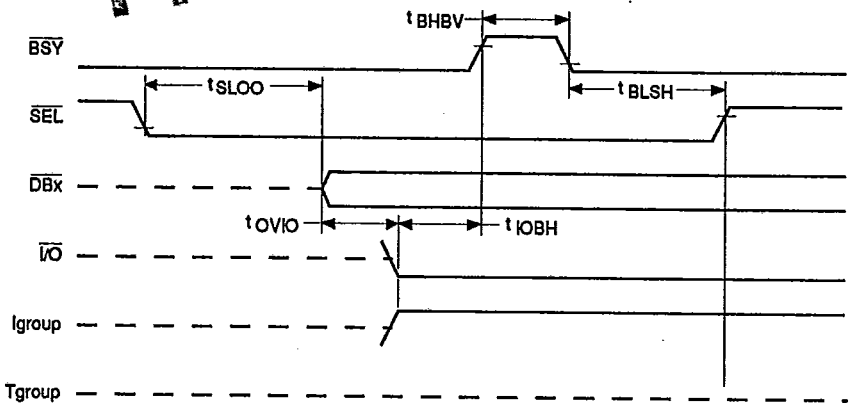
NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

11653-028A

T-52-33-27

RESELECTING AN INITIATOR (AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SLOO}	$\overline{SEL}$ Out Low to "OR-ED" ID Out	2		µs
t_{OVIO}	"OR-ED" ID Out Valid to I/O & Tgroup Out Valid	100		ns
t_{IOBH}	I/O & Tgroup Out Valid to $\overline{BSY}$ Out High	100		ns
t_{BHBV}	$\overline{BSY}$ Out High to $\overline{BSY}$ In Low Valid	400		ns
t_{BLSH}	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns

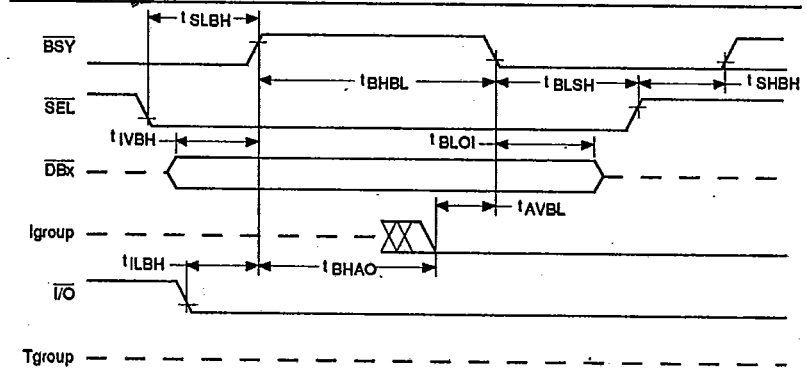


NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

11853-029A

RESPONSE TO RESELECTION (AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SLBH}	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
t_{IVBH}	"OR-ED" ID Valid In to $\overline{BSY}$ In High	0		ns
t_{ILBH}	$\overline{I/O}$ In Low to $\overline{BSY}$ In High	0		ns
t_{BHAO}	$\overline{SEL}$ Low , ID Valid , $\overline{BSY}$ High to Igroup Out	100		ns
t_{AVBL}	Igroup Valid Out to $\overline{BSY}$ Out Low	100		ns
t_{BHBL}	$\overline{BSY}$ In High to $\overline{BSY}$ Out Low	0.4	200	µs
t_{BLOI}	$\overline{BSY}$ Out Low to "OR-ED" ID Invalid In	0		ns
t_{BLSH}	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
t_{SHBH}	$\overline{SEL}$ In High to $\overline{BSY}$ Out High	0		ns



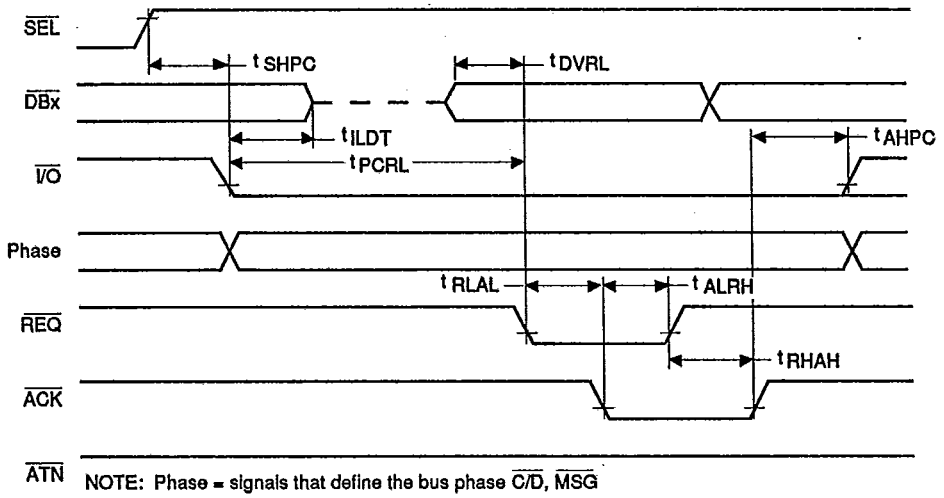
Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$
*** $\overline{BSY}$ will still be driven by the reselecting target.

11853-030A

T-52-33-27

RECEIVE ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change In	0		ns
t_{ILDT}	$\overline{I/O}$ In Low to Data Bus TRISTATE	0	125	ns
t_{PCRL}	Phase Change In to $\overline{REQ}$ In Low	400		ns
t_{DVRL}	Data Valid In to $\overline{REQ}$ In Low	0		ns
t_{RLAL}	$\overline{REQ}$ In Low to $\overline{ACK}$ Out Low	0	175	ns
t_{ALDI}	$\overline{ACK}$ Out Low to Data Invalid In	0		ns
t_{ALRH}	$\overline{ACK}$ Out Low to $\overline{REQ}$ In High	0		ns
t_{RHAH}	$\overline{REQ}$ In High to $\overline{ACK}$ Out High	0	175	ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change In	0		ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

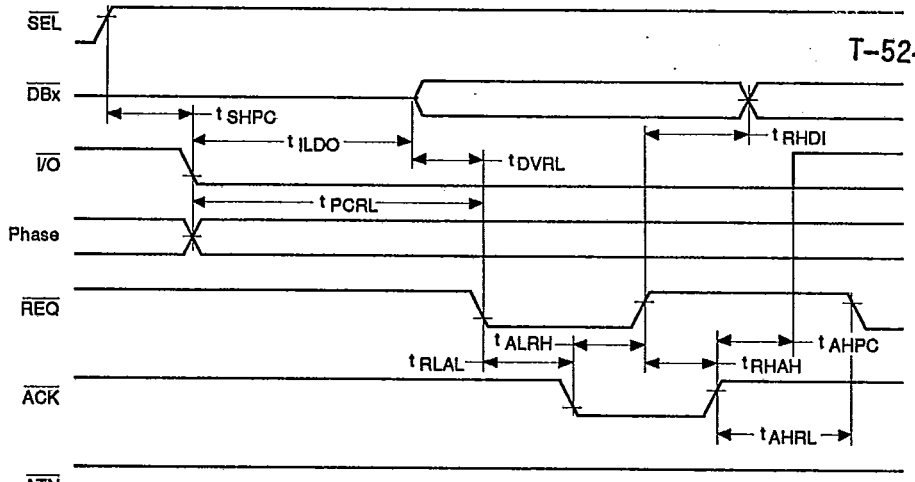
11853-031A

4

SEND ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change Out	100		ns
t_{ILDO}	$\overline{I/O}$ Out Low to Data Out	800		ns
t_{DVRL}	Data Out Valid to $\overline{REQ}$ Out Low	55		ns
t_{PCRL}	Phase Change Out to $\overline{REQ}$ Out Low	500		ns
t_{RLAL}	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
t_{ALRH}	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
t_{ALDI}	$\overline{ACK}$ In Low to Data Out Invalid	0		ns
t_{RHAH}	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	100		ns
t_{AHRL}	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns

T-52-33-27

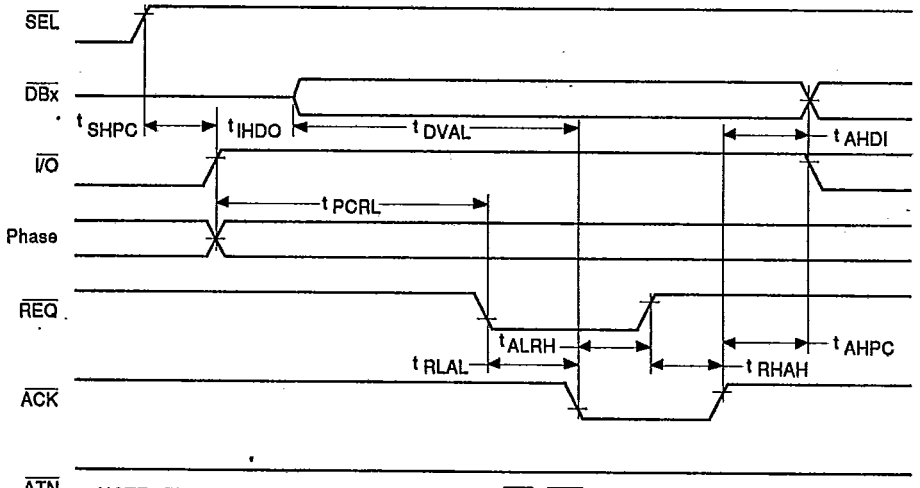


NOTE: Phase = signals that define the bus phase C/D, MSG

11853-032A

SEND ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	SEL In High to Phase Change In	0		ns
t_{IHDO}	I/O In High to Data Out	0		ns
t_{PCRL}	Phase Change In to REQ In Low	400		ns
t_{RLAL}	REQ In Low to ACK Out Low	0	175	ns
t_{DVAL}	Data Out Valid to ACK Out Low	55		ns
t_{ALRH}	ACK Out Low to REQ In High	0		ns
t_{RHAH}	REQ In High to ACK Out High	0	175	ns
t_{RHDI}	REQ In High to Data Out Invalid	0		ns
t_{AHPC}	ACK Out High to Phase Change In	0		ns



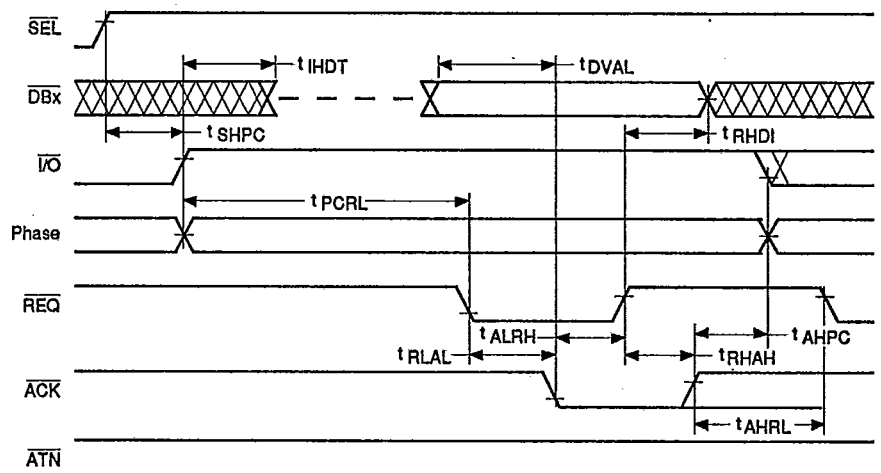
NOTE: Phase = signals that define the bus phase C/D, MSG

11853-033A

T-52-33-27

RECEIVE ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change Out	100		ns
t_{IHDT}	$\overline{I/O}$ Out High to Data Bus TRISTATE	0		ns
t_{PCRL}	Phase Change to $\overline{REQ}$ Out Low	500		ns
t_{RLAL}	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
t_{DVAL}	Data In Valid to $\overline{ACK}$ In Low	0		ns
t_{ALRH}	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
t_{RHDI}	$\overline{REQ}$ Out High to Data In Invalid	0		ns
t_{RHAH}	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	0		ns
t_{AHRL}	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns



NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-034A

4

RECEIVE SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{DVRL}	Data Valid In to $\overline{REQ}$ In Low	0		ns
t_{RLDI}	$\overline{REQ}$ In Low to DATA Invalid	45		ns
t_{RLRH}	$\overline{REQ}$ In Low to $\overline{REQ}$ In High	50		ns
t_{RHRL}	$\overline{REQ}$ In High to $\overline{REQ}$ In Low	50		ns
t_{ALAH}	$\overline{ACK}$ Out Low to $\overline{ACK}$ Out High	Tcyc-10		ns
t_{AHAL}	$\overline{ACK}$ Out High to $\overline{ACK}$ Out Low	Tcyc-25		ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change	0		ns

Parameters t_{SHPC}, t_{ILDT}, and t_{PCRL} are also applicable and are identical to those in Receive Asynchronous Information Transfer In (Acting as an Initiator), top of page 37.