TECHNICAL SPECIFICATIONS

ATA 20 SERIES FLASH CARDS

7P008ATA2003C25 8MB
7P016ATA2003C25 16MB
7P032ATA2003C25 32MB
7P048ATA2003C25 48MB
7P064ATA2003C25 64MB
7P080ATA2003C25 80MB
7P096ATA2003C25 96MB
7P112ATA2003C25 112MB
7P128ATA2003C25 128MB
7P160ATA2003C25 160MB

Description

Models 7P008ATA20, 7P016ATA20, 7P032ATA20, 7P048ATA20, 7P064ATA20, 7P080ATA20, 7P096ATA20, 7P112ATA20, 7P128ATA20 and 7P160ATA20 are Flash ATA cards. They comply with the PC card ATA standard and are suitable for usage as a data storage memory medium for PCs or other electronic equipment. These cards are built with Hitachi 64 Mb Flash memory devices HN29W6411. The cards are suitable for the ISA (Industry Standard Architecture) bus interface standard. The read/write unit is 1 sector (512 bytes) sequential access.

Features

- PC card ATA standard specification
  - 68 pin two piece connector and type I (3.3 mm) or type II (5 mm) stainless steel housing
- 3.3 V/5 V single power supply operation
- ISA standard and Read/Write unit is 512 bytes (sector) sequential access
  - Sector Read/Write transfer rate: 8MB/sec burst
  - High reliability based on internal ECC (Error Correcting Code) function
- Maximum card density is 160MB
  - Cards are built with Hitachi 64 Mb Flash memory devices (HN29W6411A)
- 3 variations of mode access
  - Memory card mode
  - I/O card mode
  - True-IDE mode
- Internal self-diagnostic program operates at V_{CC} power on
- High reliability based on wear leveling function
- Data write endurance is 300,000 cycles (with approximately 500 kB DOS file)
- Data reliability is 1 error in 10^{14} bits read.
- Industrial temperature range version: -40°C to +85°C
- Auto Sleep Function

Card Line Up

Card type	Card density	Capacity (3)	Total sectors/ card (2)	Sectors / track	Number of heads	Number of cylinder
7P008ATA2003C25	8MB	8,060,928 Byte	15,744	32	2	246
7P016ATA2003C25	16MB	16,121,856 Byte	31,488	32	4	246
7P032ATA2003C25	32MB	32,243,712 Byte	62,976	32	4	492
7P048ATA2003C25	48MB	48,365,568 Byte	94,464	32	4	738
7P064ATA2003C25	64MB	64,487,424 Byte	125,952	32	4	984
7P080ATA2003C25	80MB	80,609,280 Byte	157,440	32	8	615
7P096ATA2003C25	96MB	96,731,136 Byte	188,928	32	8	738
7P112ATA2003C25	112MB	112,852,992 Byte	220,416	32	8	861
7P128ATA2003C25	128MB	128,974,848 Byte	251,904	32	8	984
7P160ATA2003C25	160MB	161,218,560 Byte	314,880	32	16	615

Notes: 1. Total tracks = number of head × number of cylinder.
2. Total sectors/card = sectors/track × number of head × number of cylinder.
3. It is the logical address capacity including the area which is used for file system.

Card Pin Assignment

	Memory card mode		I/O card mode		True IDE mode	
Pin NO.	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE1	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	—	—	—	—	—	—
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	—	—	—	—	—	—
14	—	—	—	—	—	—
15	-WE	I	-WE	I	-WE	I
16	RDY/-BSY	O	-IREQ	O	INTRQ	O
17	VCC	—	VCC	—	VCC	—
18	—	—	—	—	—	—
19	—	—	—	—	—	—
20	—	—	—	—	—	—
21	—	—	—	—	—	—
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	-IOIS16	O	-IOIS16	O
34	GND	—	GND	—	GND	—
35	GND	—	GND	—	GND	—

	Memory card mode		I/O card mode		True IDE mode	
Pin NO.	Signal name	I/O	Signal name	I/O	Signal name	I/O
36	-CD1	O	-CD1	O	-CD1	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I/O	D15	I/O	D15	I/O
42	-CE2	I	-CE2	I	-CE2	I
43	-VS1	O	-VS1	O	-VS1	O
44	-IORD	I	-IORD	I	-IORD	I
45	-IOWR	I	-IOWR	I	-IOWR	I
46	—	—	—	—	—	—
47	—	—	—	—	—	—
48	—	—	—	—	—	—
49	—	—	—	—	—	—
50	—	—	—	—	—	—
51	VCC	—	VCC	—	VCC	—
52	—	—	—	—	—	—
53	—	—	—	—	—	—
54	—	—	—	—	—	—
55	—	—	—	—	—	—
56	-CSEL	I	-CSEL	I	-CSEL	I
57	-VS2	O	-VS2	O	-VS2	O
58	RESET	I	RESET	I	-RESET	I
59	-WAIT	O	-WAIT	O	IORDY	O
60	-INPACK	O	-INPACK	O	-INPACK	O
61	-REG	I	-REG	I	-REG	I
62	BVD2	I/O	-SPKR	I/O	-DASP	I/O
63	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	I/O	D10	I/O	D10	I/O
67	-CD2	O	-CD2	O	-CD2	O
68	GND	—	GND	—	GND	—

Card Pin Explanation

Address bus (A0 to A10: input): Address bus is A0 to A10. A0 is invalid in word mode. A10 is MSB and A0 is LSB. In True IDE Mode only HA [2 : 0] are used for selecting the one of eight registers in the Task File, the remaining address lines should be grounded.

Data bus (D0 to D15: input/output): Data bus is D0 to D15. D0 is the LSB of the Even Byte of the Word. D8 is the LSB of the Odd Byte of the Word.

Card enable (-CE1, -CE2: input): -CE1 and -CE2 are low active card select signals. Even addresses are controlled by -CE1 and odd addresses are by -CE2. In True IDE Mode -CE2 is used for select the Alternate Status Register and the Device Control Register while -CE1 is the chip select for the other task file registers.

Output enable, ATA select (-OE, -ASTEL: input): -OE is used for the control of data read in Attribute area or Common memory area. To enable True IDE Mode this input should be grounded by the host.

Write enable (-WE: input): -WE is used for the control of data write in Attribute memory area or Common memory area. In True IDE Mode this input signal is not used and should be connected to VCC.

I/O read (-IORD: input): -IORD is used for control of read data in the Task File area. This card does not respond to -IORD until I/O card interface setting up.

I/O write (-IOWR: input): -IOWR is used for control of data write in the Task File area. This card does not respond to -IOWR until I/O card interface setting up.

Ready/Busy, Interrupt request (RDY/-BSY, -IREQ, INTRQ: output): In the I/O card mode, this signal is -IREQ pin. The signal of low level indicates that the card is requesting software service to the host, and high level indicates that the card is not requesting. In memory card mode, the signal is RDY/-BSY pin. RDY/-BSY pin turns low level during the card internal initialization operation at V_{CC} applied or reset applied, so the next access to the card should be after the signal turns high level. In True IDE Mode signal is the active high Interrupt Request to the host.

Card detection (-CD1, -CD2: output): -CD1 and -CD2 are the card detection signals. -CD1 and -CD2 are connected to ground in this card, so the host can detect if the card is inserted or not.

Write protect, 16 bit I/O port (WP, -IOIS16: output): In memory card mode, WP is held low because this card does not have a write protect switch. In the I/O card mode, -IOIS16 is asserted when Task File registers are accessed in 16-bit mode. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Attribute memory area selection (-REG: input): -REG should be high level during common memory area accessing, and low level during Attribute area accessing. The attribute memory area is located only in an even address, so D0 to D7 are valid and D8 to D15 are invalid in the word access mode. Odd addresses are invalid in the byte access mode. In True IDE Mode this input signal is not used and should be connected to VCC.

Battery voltage detection, Digital audio output, Disk active/slave present (BVD2, -SPKR, -DASP: input/output): In memory card mode, BVD2 outputs the battery voltage status in the card. This card has no battery, so this output is high level constantly. In the I/O card mode, -SPKR is held High because this card does not have digital audio output. In True IDE Mode -DASP is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.

Reset (RESET, -RESET: input): By assertion of the RESET signal, all registers of this card are cleared and the RDY/-BSY signal turns to high level. In True IDE Mode -RESET is the active low hardware reset from the host.

Wait (-WAIT, IORDY: output): This signal outputs low level for the purpose of delaying memory access cycle or I/O access cycle. In True IDE Mode this output signal may be used as IORDY. As for this controller, this output is high impedance state constantly.

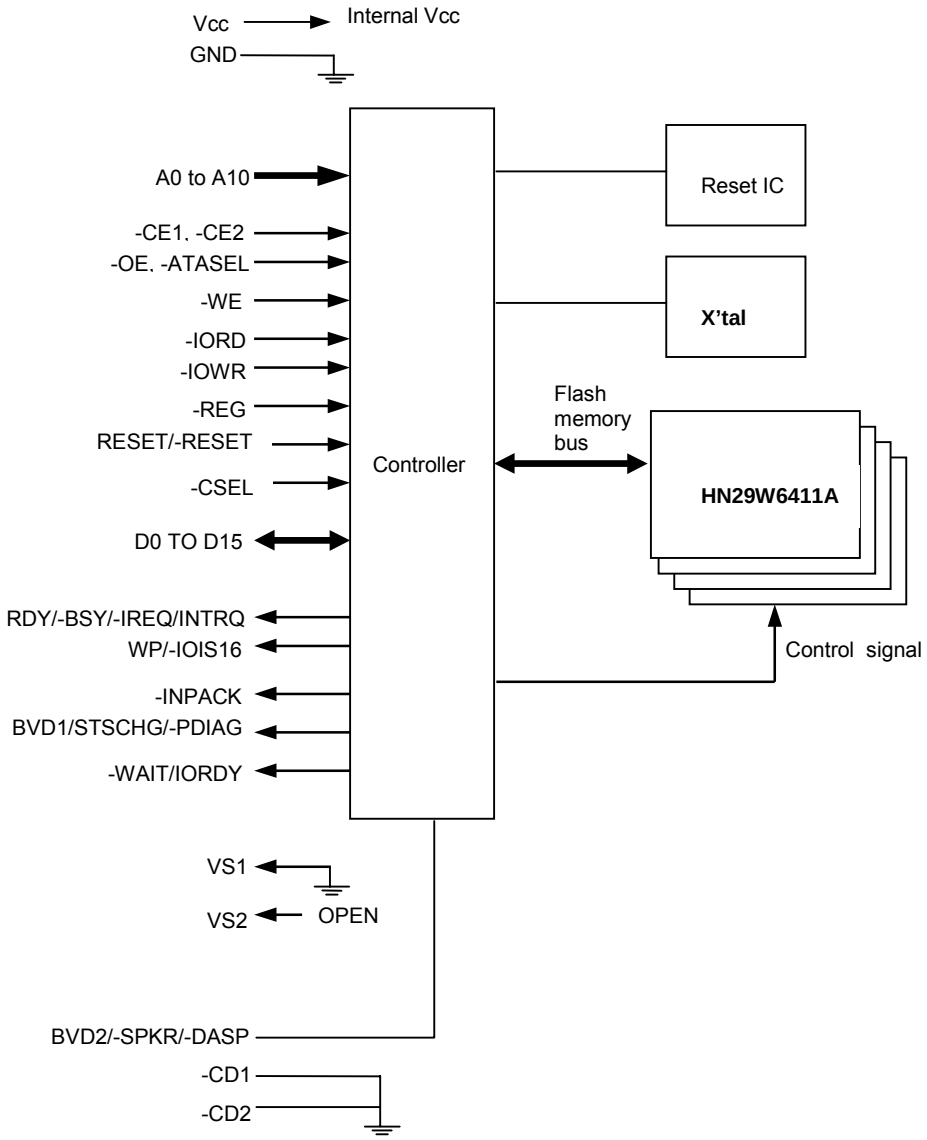
Input acknowledge (-INPACK: output): This signal is not used in the memory card mode. This signal is asserted by this card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used for the input data buffer control. In True IDE Mode this output signal is not used and should be kept open at the host side.

Battery voltage detection, Status change, Pass diagnostic (BVD1, -STSCHG, -PDIAG: input/output): In the memory card mode, BVD1 outputs the battery voltage status in the card. This card has no battery, so this output is high level constantly. In the I/O card mode, -STSCHG is used for changing the status of the Configuration status register in the Attribute area, while the card is set I/O card interface. In True IDE Mode, -PDIAG is the Pass Diagnostic signal in the Master/Slave handshake protocol.

V_{CC} voltage sense (-VS1, -VS2: output): These signals are intended to notify the socket of the PC Card's CIS V_{CC} requirement. -VS1 is held low and -VS2 is nonconnected in this card.

Card select (-CSEL: input): This signal is not used in the memory card mode and I/O card mode. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Card Block Diagram



Note: -CE1, -CE2, -OE, -WE, -IORD, -IOWR, -REG, RESET, -CSEL pins are pulled up in the card.
-PDIAG PIN IS Schmitt trigger type input output buffer.

Card Function Explanation

Register Construction

- Attribute region
  - — Configuration register
    - Configuration Option register
    - Configuration and Status register
    - Pin Replacement register
    - Socket and Copy register
  - — CIS (Card Information Structure)

- Task File region
  - — Data register
  - — Error register
  - — Feature register
  - — Sector Count register
  - — Sector Number register
  - — Cylinder Low register
  - — Cylinder High register
  - — Drive Head register
  - — Status register
  - — Alternate Status register
  - — Command register
  - — Device Control register
  - — Drive Address register

Host Access Specifications

1. Attribute Access Specifications

When the CIS-ROM region or the Configuration register region is accessed, read and write operations are executed under the condition of -REG = "L" as follows. That region can be accessed by Byte/Word/Odd-byte modes which are defined by the PC card standard specifications.

Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access (16-bit)	L	L	L	×	L	H	invalid	even byte
Odd byte access (8-bit)	L	L	H	×	L	H	invalid	High-Z

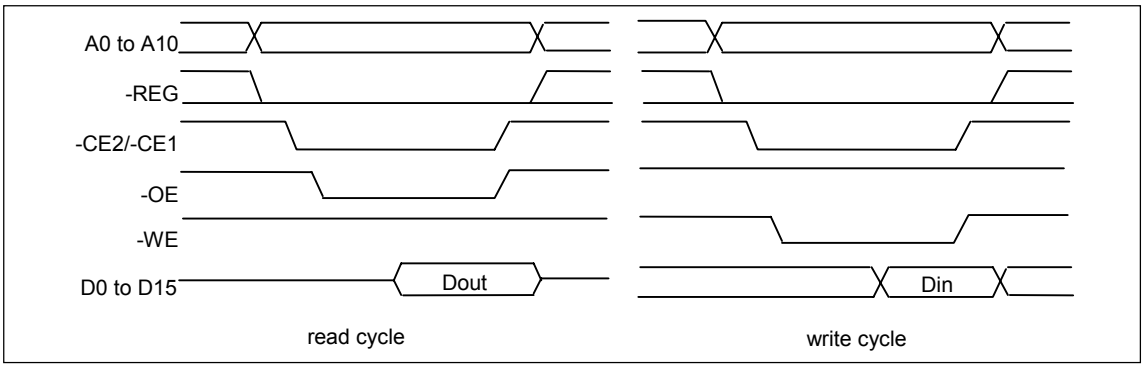
Note: ×: L or H

Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	Don't care	even byte
	L	H	L	H	H	L	Don't care	Don't care
Word access (16-bit)	L	L	L	×	H	L	Don't care	even byte
Odd byte access (8-bit)	L	L	H	×	H	L	Don't care	Don't care

Note: ×: L or H

Attribute Access Timing Example



2. Task File Register Access Specifications

There are two cases of Task File register mapping, one is the mapped I/O address area, the other is the mapped Memory address area. Each case of Task File register read and write operations is executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte mode which is defined by the PC card standard specifications.

(1) I/O address map

Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access (8-bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16-bit)	L	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access (8-bit)	L	L	H	×	L	H	H	H	odd byte	High-Z

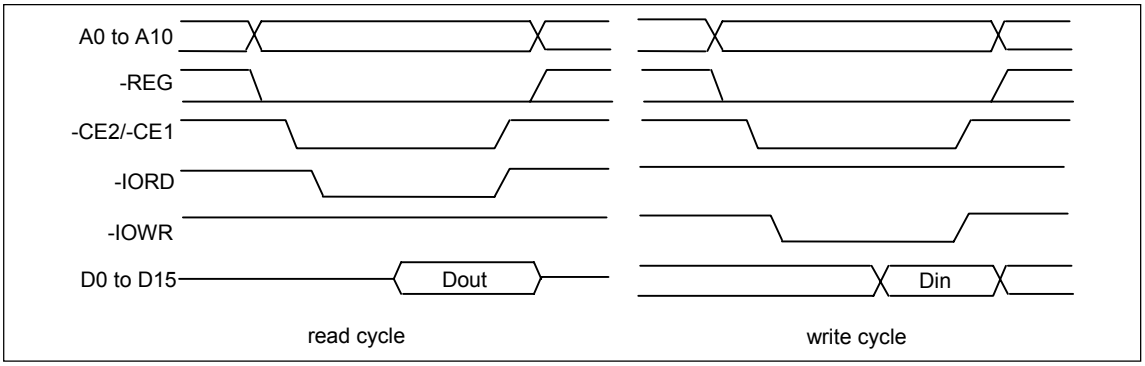
Note: ×: L or H

Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access (8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16-bit)	L	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access (8-bit)	L	L	H	×	H	L	H	H	odd byte	Don't care

Note: ×: L or H

Task File Register Access Timing Example (1)



(2) Memory address map

Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access (8-bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access (16-bit)	H	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access (8-bit)	H	L	H	×	L	H	H	H	odd byte	High-Z

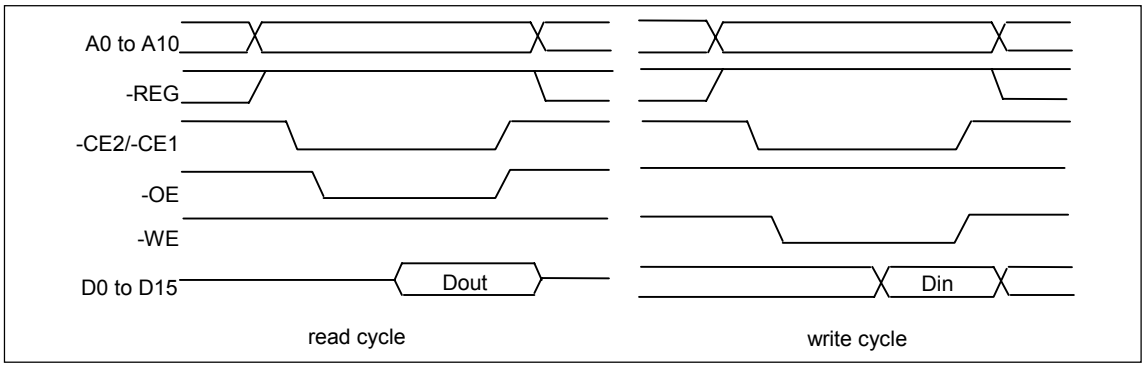
Note: ×: L or H

Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access (8-bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access (16-bit)	H	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access (8-bit)	H	L	H	×	H	L	H	H	odd byte	Don't care

Note: ×: L or H

Task File Register Access Timing Example (2)



3. True IDE Mode

The card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the -OE input signal is asserted low by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode no Memory or Attribute Registers are accessible to the host. The card permits 8 bit access if the user issues a Set Feature Command to put the device in the 8 bit Mode.

True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	High-Z	High-Z
Standby mode	H	H	×	×	×	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
All status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

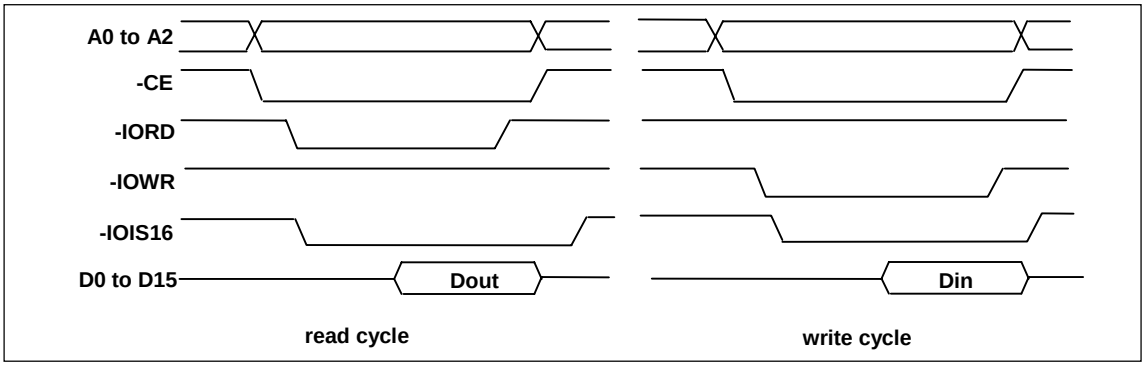
Note: ×: L or H

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	don't care	don't care
Standby mode	H	H	×	×	×	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: ×: L or H

True IDE Mode I/O Access Timing Example



Configuration Register Specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card.

1. Configuration Option Register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing the soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevlREQ	INDEX					

Note: initial value: 00H

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to "1", places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit is set to "0", places the card in the reset state of Hard Reset (This bit is set to "0" by Hard Reset) . Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so the next access to the card should be the same sequence as the power on sequence.
LevlREQ (HOST->)	R/W	This bit sets to "0" when pulse mode interrupt is selected, and "1" when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bit is used to select the operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is "000000" for the purpose of Memory card interface recognition.

INDEX bit assignment

INDEX bit								
5	4	3	2	1	0	Card mode	Task File register address	Mapping mode
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
0	0	0	0	0	1	I/O card	xx0H to xxFH	contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	secondary I/O mapped

2. Configuration and Status Register (Address 202H)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value: 00H

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that the CRDY/-BSY bit on the Pin Replacement register is set to "1". When CHGED bit is set to "1", the -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by the CHGED bit. If this bit is set to "0", the -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with on 8 bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters the sleep state (Power Down mode). When this bit is reset to "0", the card transfers to the idle state (active mode). RRDY/-BSY bit on the Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether the I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero.

3. Pin Replacement Register (Address 204H)

This register is used for providing the signal state of the -IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

Note: initial value: 0CH

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-BSY bit masking.

4. Socket and Copy Register (Address 206H)

This register is used for identification of the card from the other cards. The host can read and write this register. This register should be set by the host before this card's Configuration Option register set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

Note: initial value: 00H

Name	R/W	Function
DRV# (HOST->)	R/W	This field is used for the configuration of the plural cards.

CIS Information

CIS information is defined as follows. By reading the attribute address from "0000 H", the card CIS information can be confirmed.

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
000H	01H	CISTPL DEVICE								Device info tuple	Tuple code
002H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
004H	DFH	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 1: No WP Device speed = 7: ext speed	Device type, WPS, speed
006H	4AH	EXT	Speed mantissa				Speed exponent			400 ns if no wait	Extended speed
008H	01H	1x					2k units			2k byte of address space	Device size
00AH	FFH	List end marker								End of device	END marker
00CH	1CH	CISTPL DEVICE OC								Other conditions device info tuple	Tuple code
00EH	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
010H	02H	EXT	Reserved				V_{CC}		MWAIT	3 V, wait is not used	Other conditions info field
012H	D9H	Device type				WPS	Device speed			Device type = DH: I/O device WPS = 1: No WP Device speed = 1: 250 ns	Device type, WPS, speed
014H	01H	1x					2k units			2k byte of address space	Device size
016H	FFH	List end marker								End of device	END marker
018H	18H	CISTPL JEDEC C								JEDEC ID common memory	Tuple code
01AH	02H	TPL_LINK								Link length is 2 bytes	Link to next tuple
01CH	DFH	PCMCIA's manufacturer's JEDEC ID code								Manufacturer's ID code	JEDEC ID of PC Card ATA
01EH	01H	PCMCIA JEDEC device code								2nd byte of JEDEC ID	
020H	20H	CISTPL MANFID								Manufacturer's ID code	Tuple code
022H	04H	TPL_LINK								Link length is 4 bytes	Link to next tuple
024H	07H	Low byte of PCMCIA manufacturer's code								HITACHI JEDEC manufacturer's ID	Low byte of manufacturer's ID code
026H	00H	High byte of PCMCIA manufacturer's code								Code of 0 because other byte is JEDEC 1 byte manufac ID	High byte of manufacturer's ID code
028H	00H	Low byte of product code								HITACHI code for PC CARD ATA	Low byte of product code
02AH	00H	High byte of product code									High byte of product code

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
02CH	15H	CISTPL_VER_1	Level 1 version/product info	Tuple code
02EH	15H	TPL_LINK	Link length is 15h bytes	Link to next tuple
030H	04H	TPPLV1_MAJOR	PCMCIA2.0/JEIDA4.1	Major version
032H	01H	TPPLV1_MINOR	PCMCIA2.0/JEIDA4.1	Minor version
034H	48H		‘ H ’	Info string 1
036H	49H		‘ I ’	
038H	54H		‘ T ’	
03AH	41H		‘ A ’	
03CH	43H		‘ C ’	
03EH	48H		‘ H ’	
040H	49H		‘ I ’	
042H	00H		Null terminator	
044H	46H		‘ F ’	Info string 2
046H	4CH		‘ L ’	
048H	41H		‘ A ’	
04AH	53H		‘ S ’	
04CH	48H		‘ H ’	
04EH	00H		Null terminator	
050H	34H		‘ 4 ’	Vender specific strings
052H	2EH		‘ . ’	
054H	30H		‘ 0 ’	
056H	00H		Null terminator	
058H	FFH	List end marker	End of device	END marker
05AH	21H	CISTPL FUNCID	Function ID tuple	Tuple code
05CH	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
05EH	04H	TPLFID_FUNCTION = 04H	Disk function, may be silicon, may be removable	PC card function code
060H	01H	Reserved	R	P

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
062H	22H	CISTPL FUNCE	Function extension tuple	Tuple code
064H	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
066H	01H	Disk function extension tuple type	Disk interface type	Extension tuple type for disk
068H	01H	Disk interface type	PC card ATA interface	Interface type
06AH	22H	CISTPL FUNCE	Function extension tuple	Tuple code
06CH	03H	TPL_LINK	Link length is 3 bytes	Link to next tuple
06EH	02H	Disk function extension tuple type	Single drive	Extension tuple type for disk
070H	0CH	Reserved D U S V	No V_{PP}, silicon, single drive V = 0: No V_{PP} required S = 1: Silicon U = 1: Unique serial # D = 0: Single drive on card	Basic ATA option parameters byte 1
072H	0FH	R I E N P3 P2 P1 P0	P0: Sleep mode supported P1: Standby mode supported P2: Idle mode supported P3: Drive auto power control N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS16# data reg only R: Reserved	Basic ATA option parameters byte 2
074H	1AH	CISTPL CONF	Configuration tuple	Tuple code
076H	05H	TPL LINK	Link length is 5 bytes	Link to next tuple
078H	01H	RFS RMS RAS	RFS: Reserved RMS: TPCC_RMSK size - 1 = 0 RAS: TPCC_RADR size - 1 = 1 1 byte register mask 2 byte config base address	Size of fields byte TPCC_SZ
07AH	03H	TPCC_LAST	Entry with config index of 03H is final entry in table	Last entry of config registers
07CH	00H	TPCC RADR (LSB)	Configuration registers are located at 200 H in REG space	Location of config registers
07EH	02H	TPCC RADR (MSB)		
080H	0FH	Reserved S P C I	I: Configuration Index C: Config. and Status P: Pin Replacement S: Socket and Copy	Configuration registers present mask TPCC_RMSK

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
082H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
084H	08H	TPL_LINK								Link length is 8 bytes	Link to next tuple
086H	C0H	I	D	Configuration index						Memory mapped I/O configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
088H	C0H	W	R	P	B	Interface type				W = 1: Wait used R = 1: Ready active P = 0: WP used B = 0: BVD1 and BVD2 not used IF type = 0: Memory interface	Interface description field TPCE_IF
08AH	A1H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 01: Memory space info single 2-byte length IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
08CH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
08EH	55H	X	Mantissa				Exponent			Nominal voltage = 5 V	V_{CC} nominal value
090H	08H	Length in 256 bytes pages (LSB)								Length of memory space is 2 kB	Memory space description structures (TPCE MS)
092H	00H	Length in 256 bytes pages (MSB)									
094H	20H	X	R	P	R O	A	T			X = 0: No more misc fields R: Reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
096H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
098H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
09AH	00H	I	D	Configuration index						Memory mapped I/O configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 0	Configuration table index byte TPCE_INDX
09CH	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
09EH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0A0H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0A2H	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0A4H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0A6H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0A8H	0AH	TPL_LINK								Link length is 10 bytes	Link to next tuple
0AAH	C1H	I	D	Configuration INDEX						Contiguous I/O mapped ATA registers configuration I = 1: Interface byte follows D = 1: Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0ACH	41H	W	R	P	B	interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0AEH	99H	M	MS		IR	IO	T	P		M = 1: Misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0B0H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0B2H	55H	X	Mantissa			Exponent				Nominal voltage = 5 V	V_{CC} nominal value
0B4H	64H	R	S	E	IO AddrLine					S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLine: 4 lines decoded	I/O space description field TPCE_IO
0B6H	F0H	S	P	L	M	V	B	I	N	S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 1: Bit mask of IRQs present V = 0: No vender unique IRQ B = 0: No bus error IRQ I = 0: No IO check IRQ N = 0: No NMI	Interrupt request description structure TPCE_IR

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0B8H	FFH	IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1	IRQ0	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
0BAH	FFH	IRQ 15	IRQ 14	IRQ 13	IRQ 12	IRQ 11	IRQ 10	IRQ 9	IRQ8	Recommended routing to any “normal, maskable” IRQ.	Mask extension byte 2 TPCE_IR
0BCH	20H	X	R	P	RO	A	T			X = 0: No more misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0BEH	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0C0H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0C2H	01H	I	D	Configuration index						Contiguous I/O mapped ATA registers configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 1	Configuration table index byte TPCE_INDX
0C4H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0C6H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0C8H	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0CAH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0CCH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0CEH	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0D0H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
0D2H	C2H	I	D	Configuration INDEX						ATA primary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry follows Configuration index = 2	Configuration table index byte TPCE_INDX
0D4H	41H	W	R	P	B	interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
0D6H	99H	M	MS		IR	IO	T	P		M = 1: misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0D8H	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0DAH	55H	X	Mantissa			Exponent				Nominal voltage = 5 V	V_{CC} nominal value
0DCH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
0DEH	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0E0H	F0H									1st I/O base address (LSB)	1st I/O range address
0E2H	01H									1st I/O base address (MSB)	
0E4H	07H									1st I/O length - 1	1st I/O range length
0E6H	F6H									2nd I/O base address (LSB)	2nd I/O range address
0E8H	03H									2nd I/O base address (MSB)	
0EAH	01H									2nd I/O length - 1	2nd I/O range length
0ECH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level is IRQ14	Interrupt request description structure TPCE_IR
0EEH	20H	X	R	P	RO	A	T			X = 0: No more misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0F0H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
0F2H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
0F4H	02H	I	D	Configuration index						ATA primary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 2	Configuration table index byte TPCE_INDX
0F6H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
0F8H	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
0FAH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
0FCH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
0FEH	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
100H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
102H	0FH	TPL_LINK								Link length is 15 bytes	Link to next tuple
104H	C3H	I	D	Configuration INDEX						ATA secondary I/O mapped configuration I = 1: Interface byte follows D = 1: default entry Configuration index = 3	Configuration table index byte TPCE_INDX
106H	41H	W	R	P	B	interface type				W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface	Interface description field TPCE_IF
108H	99H	M	MS		IR	IO	T	P		M = 1: misc info present MS = 00: No memory space info IR = 1: Interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
10AH	01H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down Current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
10CH	55H	X	Mantissa			Exponent				Nominal voltage = 5 V	V_{CC} nominal value
10EH	EAH	R	S	E	IO AddrLine					R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
110H	61H	LS		AS		N range				LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address range - 1	I/O range format description

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
112H	70H									1st I/O base address (LSB)	1st I/O range address
114H	01H									1st I/O base address (MSB)	
116H	07H									1st I/O length - 1	1st I/O range length
118H	76H									2nd I/O base address (LSB)	2nd I/O range address
11AH	03H									2nd I/O base address (MSB)	
11CH	01H									2nd I/O length - 1	2nd I/O range length
11EH	EEH	S	P	L	M	IRQ level				S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present IRQ level isIRQ14	Interrupt request description structure TPCE_IR
120H	20H	X	R	P	RO	A	T			X = 0: No more misc fields R: reserved P = 1: Power down supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
122H	1BH	CISTPL_CFTABLE ENTRY								Configuration table entry tuple	Tuple code
124H	06H	TPL_LINK								Link length is 6 bytes	Link to next tuple
126H	03H	I	D	Configuration index						ATA secondary I/O mapped configuration I = 0: No Interface byte D = 0: No Default entry Configuration index = 3	Configuration table index byte TPCE_INDX
128H	01H	M	MS			IR	IO	T	P	M = 0: No Misc info MS = 00: No Memory space info IR = 0: No interrupt info present IO = 0: No I/O port info present T = 0: No timing info present P = 1: V_{CC} only info	Feature selection byte TPCE_FS
12AH	21H	R	DI	PI	AI	SI	HV	LV	NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{CC}
12CH	B5H	X	Mantissa				Exponent			Nominal voltage = 3.0 V	V_{CC} nominal value
12EH	1EH	X	Mantissa				Exponent			+0.3 V	Extension byte
130H	4DH	X	Mantissa				Exponent			Max average current over 10 msec is 45 mA	Max. average current
132H	14H	CISTPL_NO_LINK								No link control tuple	Tuple code
134H	00H									Link is 0 bytes	Link to next tuple
136H	FFH	CISTPL_END								End of list tuple	Tuple code

Task File Register Specification

These registers are used for reading and writing the storage data in this card. These registers are mapped four types by the configuration of INDEX in the Configuration Option register. The decoded addresses are shown as follows.

Memory Map (INDEX = 0)

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE = L	-WE = L
1	0	×	0	0	0	0	0H	Data register	Data register
1	0	×	0	0	0	1	1H	Error register	Feature register
1	0	×	0	0	1	0	2H	Sector count register	Sector count register
1	0	×	0	0	1	1	3H	Sector number register	Sector number register
1	0	×	0	1	0	0	4H	Cylinder low register	Cylinder low register
1	0	×	0	1	0	1	5H	Cylinder high register	Cylinder high register
1	0	×	0	1	1	0	6H	Drive head register	Drive head register
1	0	×	0	1	1	1	7H	Status register	Command register
1	0	×	1	0	0	0	8H	Dup. even data register	Dup. even data register
1	0	×	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
1	0	×	1	1	0	1	DH	Dup. error register	Dup. feature register
1	0	×	1	1	1	0	EH	Alt. status register	Device control register
1	0	×	1	1	1	1	FH	Drive address register	Reserved
1	1	×	×	×	×	0	8H	Even data register	Even data register
1	1	×	×	×	×	1	9H	Odd data register	Odd data register

Contiguous I/O Map (INDEX = 1)

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD = L	-IOWR = L
0	×	0	0	0	0	0H	Data register	Data register
0	×	0	0	0	1	1H	Error register	Feature register
0	×	0	0	1	0	2H	Sector count register	Sector count register
0	×	0	0	1	1	3H	Sector number register	Sector number register
0	×	0	1	0	0	4H	Cylinder low register	Cylinder low register
0	×	0	1	0	1	5H	Cylinder high register	Cylinder high register
0	×	0	1	1	0	6H	Drive head register	Drive head register
0	×	0	1	1	1	7H	Status register	Command register
0	×	1	0	0	0	8H	Dup. even data register	Dup. even data register
0	×	1	0	0	1	9H	Dup. odd data register	Dup. odd data register
0	×	1	1	0	1	DH	Dup. error register	Dup. feature register
0	×	1	1	1	0	EH	Alt. status register	Device control register
0	×	1	1	1	1	FH	Drive address register	Reserved

Primary I/O Map (INDEX = 2)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	-IOWR = L
0	×	1FH	0	0	0	0	Data register	Data register
0	×	1FH	0	0	0	1	Error register	Feature register
0	×	1FH	0	0	1	0	Sector count register	Sector count register
0	×	1FH	0	0	1	1	Sector number register	Sector number register
0	×	1FH	0	1	0	0	Cylinder low register	Cylinder low register
0	×	1FH	0	1	0	1	Cylinder high register	Cylinder high register
0	×	1FH	0	1	1	0	Drive head register	Drive head register
0	×	1FH	0	1	1	1	Status register	Command register
0	×	3FH	0	1	1	0	Alt. status register	Device control register
0	×	3FH	0	1	1	1	Drive address register	Reserved

Secondary I/O Map (INDEX = 3)

-REG	A10	A9 to A4	A3	A2	A1	A0	-IORD = L	-IOWR = L
0	×	17H	0	0	0	0	Data register	Data register
0	×	17H	0	0	0	1	Error register	Feature register
0	×	17H	0	0	1	0	Sector count register	Sector count register
0	×	17H	0	0	1	1	Sector number register	Sector number register
0	×	17H	0	1	0	0	Cylinder low register	Cylinder low register
0	×	17H	0	1	0	1	Cylinder high register	Cylinder high register
0	×	17H	0	1	1	0	Drive head register	Drive head register
0	×	17H	0	1	1	1	Status register	Command register
0	×	37H	0	1	1	0	Alt. status register	Device control register
0	×	37H	0	1	1	1	Drive address register	Reserved

True IDE Mode I/O Map

-CE2	-CE1	A2	A1	A0	-IORD = L	-IOWR = L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

1. Data register: This register is a 16 bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

2. Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	“0”	IDNF	“0”	ABRT	“0”	AMNF

bit	Name	Function
7	BBK (Bad block detected)	This bit is set when a Bad Block is detected in requested ID field.
6	UNC (Data ECC error)	This bit is set when an uncorrectable error occurs when reading the card.
4	IDNF (I D Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (ABoRTed command)	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, Invalid command, etc.)
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

3. Feature register: This register is a write only register and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

4. Sector count register: This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. In this card, the plural sector transfer is available across the Track or Cylinder. If the value of this register is zero, a count of 256 sectors is specified. In the plural sector transfer, if not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request. This register's initial value is "01H".

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

5. Sector number register: This register contains the starting sector number which is started by following a sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

6. Cylinder low register: This register contains the low 8 bits of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

7. Cylinder high register: This register contains the high 8 bits of the starting cylinder address which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

8. Drive head register: This register is used for selecting the Drive of Master/Slave organization and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head number			

bit	Name	Function
7	1	This bit is set to "1".
6	LBA	LBA is a flag to select either Cylinder / Head / Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00 : Sector Number Register D7-D0. LBA15-LBA08 : Cylinder Low Register D7-D0. LBA23-LBA16 : Cylinder High Register D7-D0. LBA27-LBA24 : Drive / Head Register bits HS3-HS0.
5	1	This bit is set to "1".
4	DRV (DRiVe select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using the DRV# of the Socket and Copy register.
3 to 0	Head number	This bit is used for selecting the Head number for the following command. Bit 3 is MSB.

9. Status register: This register is a read only register, and it indicates the card status of command execution. Other bits are invalid when BSY bit is "1". When this register is read, -IREQ is negated. When the host writes the command code to Command register, bits 0, 4 and 6 are cleared and bit 7 is set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF (Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC (Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ (Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR (CORRected data	This bit is set when a correctable data error has occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

10. Alternate status register: This register is the same as the Status register physically, so the bit assignment refers to a previous item of Status register. But this register is different from the Status register that -IREQ is not negated when data is read.

11. Command register: This register is a write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card, is Ready state.

		Used parameter						
Command	**Command code**	**FR**	**SC**	**SN**	**CY**	**DR**	**HD**	**LBA**
Check power mode	E5H or 98H	N	N	N	N	Y	N	N
Execute drive diagnostic	90H	N	N	N	N	Y	N	N
Erase sector	C0H	N	Y	Y	Y	Y	Y	Y
Format track	50H	N	Y	N	Y	Y	Y	Y
Identify Drive	ECH	N	N	N	N	Y	N	N
Idle	E3H or 97H	N	Y	N	N	Y	N	N
Idle immediate	E1H or 95H	N	N	N	N	Y	N	N
Initialize drive parameters	91H	N	Y	N	N	Y	Y	N
Read buffer	E4H	N	N	N	N	Y	N	N
Read multiple	C4H	N	Y	Y	Y	Y	Y	Y
Read long sector	22H or 23H	N	N	Y	Y	Y	Y	Y
Read sector	20H or 21H	N	Y	Y	Y	Y	Y	Y
Read verify sector	40H or 41H	N	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	N	N	N	N	Y	N	N
Request sense	03H	N	N	N	N	Y	N	N
Seek	7XH	N	N	Y	Y	Y	Y	Y
Set features	EFH	Y	N	N	N	Y	N	N
Set multiple mode	C6H	N	Y	N	N	Y	N	N
Set sleep mode	E6H or 99H	N	N	N	N	Y	N	N
Stand by	E2H or 96H	N	N	N	N	Y	N	N
Stand by immediate	E0H or 94H	N	N	N	N	Y	N	N
Translate sector	87H	N	Y	Y	Y	Y	Y	Y
Wear level	F5H	N	N	N	N	Y	Y	N
Write buffer	E8H	N	N	N	N	Y	N	N
Write long sector	32H or 33H	N	N	Y	Y	Y	Y	Y
Write multiple	C5H	N	Y	Y	Y	Y	Y	Y
Write multiple w/o erase	CDH	N	Y	Y	Y	Y	Y	Y
Write sector	30H or 31H	N	Y	Y	Y	Y	Y	Y
Write sector w/o erase	38H	N	Y	Y	Y	Y	Y	Y
Write verify	3CH	N	Y	Y	Y	Y	Y	Y

Note: FR: Feature register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder register
DR: DRV bit of Drive Head register
HD: Head Number of Drive Head register
LBA: Logical Block Address Mode Supported
Y: The register contains a valid parameter for this command.
N: The register does not contain a valid parameter for this command.

12. Device control register: This register is a write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×	×	×	×	1	SRST	nIEN	0

bit	Name	Function
7 to 4	×	don't care
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN (Interrupt ENable)	This bit is used for enabling -IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

13. Drive Address register: This register is a read only register, and it is used for confirming the drive status. This register provides for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
×	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	×	This bit is unknown
6	nWTG (WriTing Gate)	This bit is unknown
5 to 2	nHS3-0 (Head Select3-0)	These bits are the negative value of Head Select bits (bit 3 to 0) in theDrive/Head register.
1	nDS1 (Idrive Select1)	This bit is unknown
0	nDS0 (Idrive Select0)	This bit is unknown

ATA Command Specifications

This table summarizes the ATA command set with the paragraphs. The following shows the support commands and command codes which are written in the command registers.

ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H or 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	Y	—	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y	Y
5	Identify Drive	ECH	—	—	—	—	Y	—	—
6	Idle	E3H or 97H	—	Y	—	—	Y	—	—
7	Idle immediate	E1H or 95H	—	—	—	—	Y	—	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
9	Read buffer	E4H	—	—	—	—	Y	—	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
11	Read long sector	22H, 23H	—	—	Y	Y	Y	Y	Y
12	Read sector (s)	20H, 21H	—	Y	Y	Y	Y	Y	Y
13	Read verify sector (s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—	—
15	Request sense	03H	—	—	—	—	Y	—	—
16	Seek	7XH	—	—	Y	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—	—
19	Set sleep mode	E6H or 99H	—	—	—	—	Y	—	—
20	Stand by	E2H or 96H	—	—	—	—	Y	—	—
21	Stand by immediate	E0H or 94H	—	—	—	—	Y	—	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y	—
24	Write buffer	E8H	—	—	—	—	Y	—	—
25	Write long sector	32H or 33H	—	—	Y	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	—	Y	Y	Y	Y	Y	Y
29	Write sector(s) w/o erase	38H	—	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Note: FR: Feature Register
SC: Sector Count register (00H to FFH)
SN: Sector Number register (01H to 20H)
CY: Cylinder Low/High register (to)
DR: Drive bit of Drive/Head register
HD: Head No.(0 to 3) of Drive/Head register
NH: No. of Heads
Y: Set up
—: Not set up

1. Check Power Mode (code: E5H or 98H): This command checks the power mode.
2. Execute Drive Diagnostic (code: 90H): This command performs the internal diagnostic tests implemented by the Card.
3. Erase Sector(s) (code: C0H): This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command.
4. Format Track (code: 50H): This command writes the desired head and cylinder of the selected drive but the selected sector data is not exchanged. This card accepts a sector buffer of data from the host to follow the command with same protocol as the Write Sector Command.
5. Identify Drive (code: ECH): This command enables the host to receive parameter information from the Card.

Identify Drive Information

Word address	Default value	Total bytes	Data field type information
0	848AH	2	General configuration bit-significant information
1	XXXX	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	XXXX	2	Number of unformatted bytes per sector
6	XXXX	2	Default number of sectors per track
7 to 8	XXXX	4	Number of sectors per card (Word7 = MSW, Word8 = LSW)
9	0000H	2	Reserved
10 to 19	XXXX	20	Reserved
20	0002H	2	Buffer type (dual ported)
21	0002H	2	Buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23 to 46	XXXX	48	Firmware revision in ASCII etc.
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	Capabilities: DMA NOT Supported (bit 8), LBA supported (bit9)
50	0000H	2	Reserved
51	0100H	2	PIO data transfer cycle timing mode 1
52	0000H	2	DMA data transfer cycle timing mode not Supported
53 to 58	XXXX	12	Reserved
59	010XH	2	Multiple sector setting is valid
60 to 61	XXXX	4	Total number of sectors addressable in LBA Mode
62 to 255	0000H	388	Reserved

6. Idle (code: E3H or 97H): This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
7. Idle Immediate (code: E1H or 95H): This command causes the Card to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.
8. Initialize Drive Parameters (code: 91H): This command enables the host to set the number of sectors per track and the number of heads per cylinder.
9. Read Buffer (code: E4H): This command enables the host to read the current contents of the card's sector buffer.
10. Read Multiple (code: C4H): This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
11. Read Long Sector (code: 22H or 23H): This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
12. Read Sector(s) (code: 20H, 21H): This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
13. Read Verify Sector (code: 40H or 41H): This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host .
14. Recalibrate (code: 1XH): This command is effectively a NOP command to the Card and is provided for compatibility purposes.
15. Request Sense (code: 03H): This command requests an extended error code after a command ends with an error.
16. Seek (code: 7XH): This command is effectively a NOP command to the Card although it does perform a range check.
17. Set Features (code: EFH): This command is used by the host to establish or select certain features.

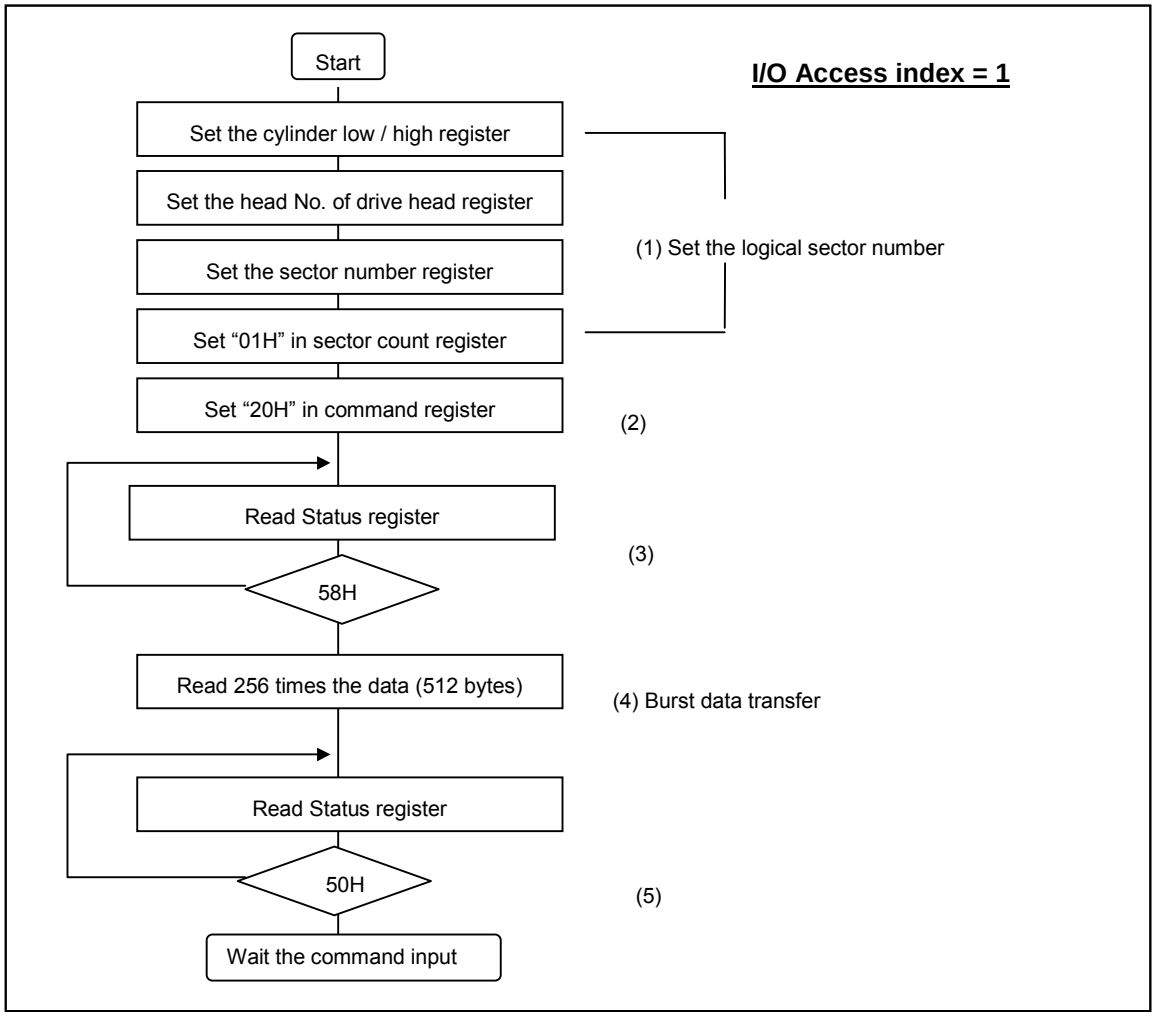
Feature	Operation
01H	Enable 8-bit data transfers.
55H	Disable Read Look Ahead.
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
81H	Enable 8-bit data transfers.
BBH	4 bytes of data apply on Read/Write Long commands.
CCH	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

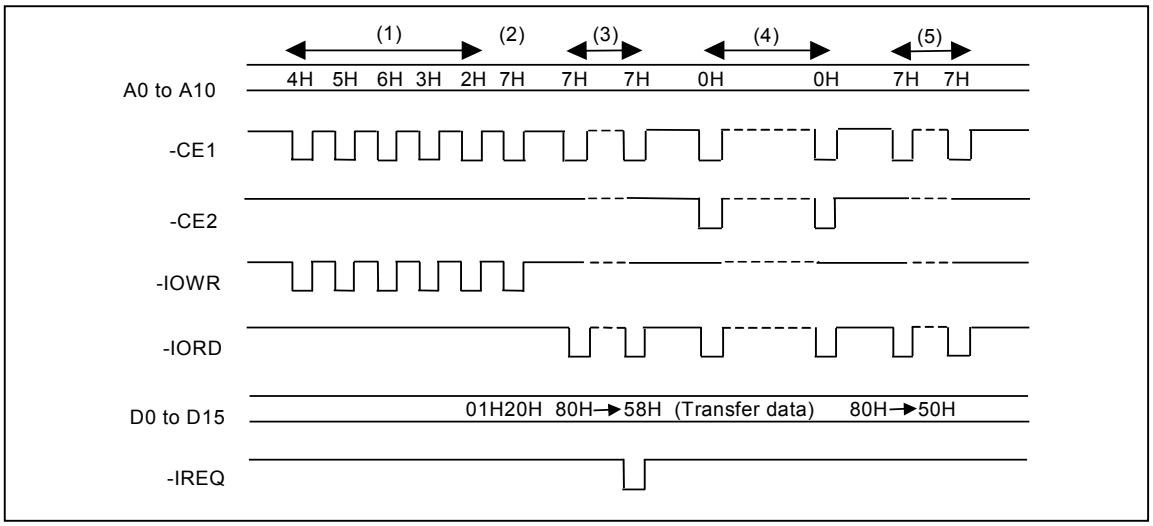
18. Set Multiple Mode (code: C6H): This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands.
19. Set Sleep Mode (code: E6H or 99H): This command causes the Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.
20. Stand By (code: E2H or 96H): This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

21. Stand By Immediate (code: E0H or 94H): This command causes the Card to set BSY, enter the Sleep mode(which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
22. Translate Sector (code: 87H): This command allows the host a method of determining the exact number of times a user sector has been erased and programmed.
23. Wear Level (code: F5H): This command is effectively a NOP command and is only implemented for backward compatibility.
24. Write Buffer (code: E8H): This command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired.
25. Write Long Sector (code: 32H or 33H): This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
26. Write Multiple (code: C5H): This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
27. Write Multiple without Erase (code: CDH): This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed.
28. Write Sector(s) (code: 30H or 31H): This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
29. Write Sector(s) without Erase (code: 38H): This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed.
30. Write Verify (code: 3CH): This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

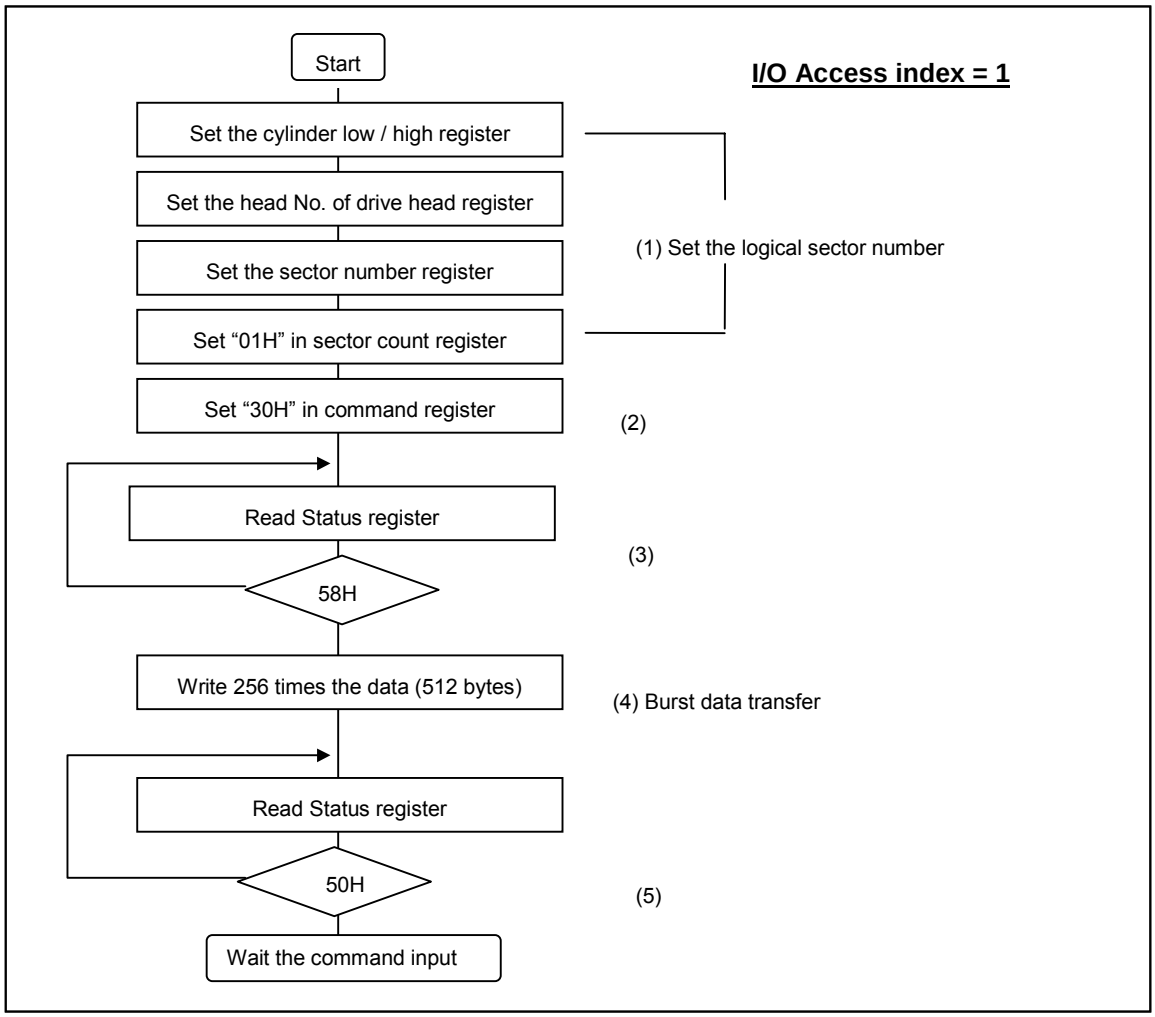
Sector Transfer Protocol

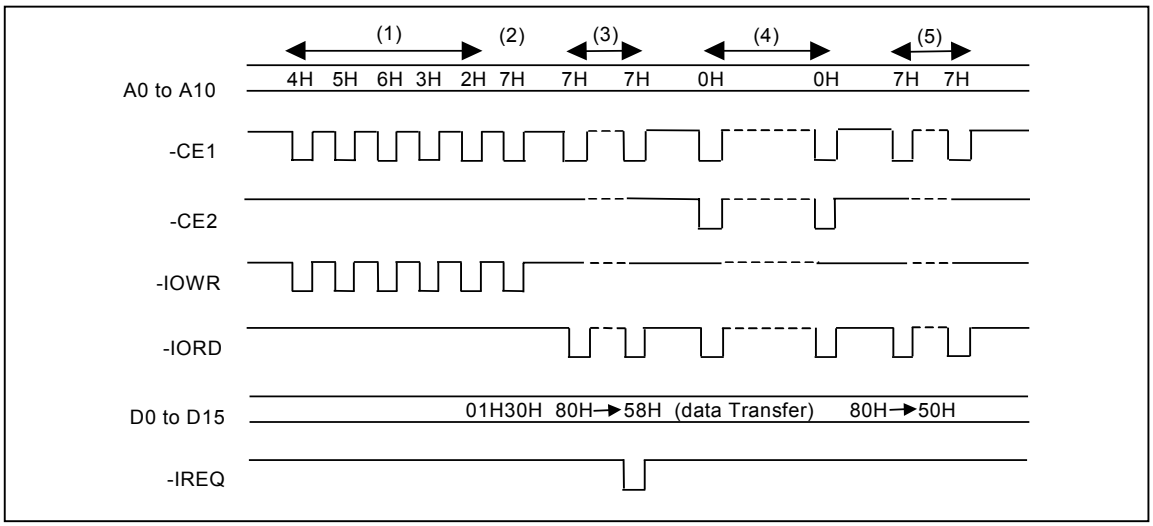
1. Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.





2. Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.





Absolute Maximum Ratings

Parameter		Symbol	Value	Unit	Note
All input/output voltages		Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
V_{CC} voltage		V_{CC}	–0.3 to +6.5	V	
Operating temperature range	Commercial	Topr	0 to +60	°C	
	Industrial		-40 to +85		
Storage temperature range	Commercial	Tstg	–20 to +65	°C	
	Industrial		-40 to +85		

Note: 1. Vin, Vout min = –2.0 V for pulse width ≤ 20 ns.

Recommended DC Operating Conditions

Voltage reference to GND, Commercial Ta =0 to 65C , industrial Ta=-40 to +85C

Parameter		Symbol	Min	Typ	Max	Unit	Note
Operating	Commercial	Ta	0	25	+60	°C	
temperature	Industrial		-40		+85		
V_{CC} voltage		V_{CC}	4.5	5.0	5.5	V	
			3.15	3.3	3.45	V	

Capacitance (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	35	pF	Vin = 0 V
Output capacitance	Cout	—	—	35	pF	Vout = 0 V

System Performance

Item	Performance
Start up times (Reset to ready)	100 ms (max)
Start up times (Sleep to idle)	2 ms (max)
Data transfer rate to/from host	8 MB/s burst
Controller overhead (Command to DRQ)	2 ms (max)
Data transfer cycle end to ready (Sector write)	1.2 ms (typ)

DC Characteristics-1

(Commercial Ta = 0 to +60°C, V_{CC} = 5.0 V ± 10%)
(Industrial Ta = -40 to +85°C, V_{CC} = 5.0 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input leakage current	I_{LI}	—	—	± 1	µA	Vin = GND to V_{CC}	1
Input voltage (CMOS)	V_{IL}	—	—	0.8	V		
	V_{IH}	4.0	—	—	V		
Input voltage (schmitt trigger)	V_{IL}	—	2.0	—	V		
	V_{IH}	—	2.8	—	V		
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	V_{CC} – 0.8	—	—	V	I_{OH} = –8 mA	

Note: 1. Except pulled up input pin.

DC Characteristics-2

(Ta = 0 to +60°C, V_{CC} = 3.3 V ± 5%)
(Ta = -40 to +85°C, V_{CC} = 3.3 V ± 5%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input leakage current	I_{LI}	—	—	± 1	µA	Vin = GND to V_{CC}	1
Input voltage (CMOS)	V_{IL}	—	—	0.6	V		
	V_{IH}	2.4	—	—	V		
Input voltage (schmitt trigger)	V_{IL}	—	1.0	—	V		
	V_{IH}	—	1.8	—	V		
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	V_{CC} – 0.8	—	—	V	I_{OH} = –8 mA	

Note: 1. Except pulled up input pin.

DC Characteristics-3 (Ta = 0 to +60°C, V_{CC} = 5.0 V ± 10%)

(Industrial Ta = -40 to +85°C, V_{CC} = 5.0 V ± 10%)

		8MB/16MB 32MB/48MB		64MB/80MB 96MB		112MB/128 MB/150MB			
Parameter	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**	**Test conditions**
Sleep/standby current	I_{SP1}	0.5	1.0	0.7	1.5	1.0	2.0	mA	CMOS level (control signal = V_{CC} – 0.2 V in Memory Card Mode and I/O Card Mode)
Sector read current	I_{CCR} (DC)	40	75	40	75	40	75	mA	CMOS level (control signal = V_{CC} – 0.2 V) during sector read transfer
	I_{CCR} (Peak)	80	120	80	120	80	120		
Sector write current	I_{CCW} (DC)	45	75	45	75	45	75	mA	CMOS level (control signal = V_{CC} – 0.2 V) during sector write transfer
	I_{CCW} (Peak)	80	120	80	120	80	120		

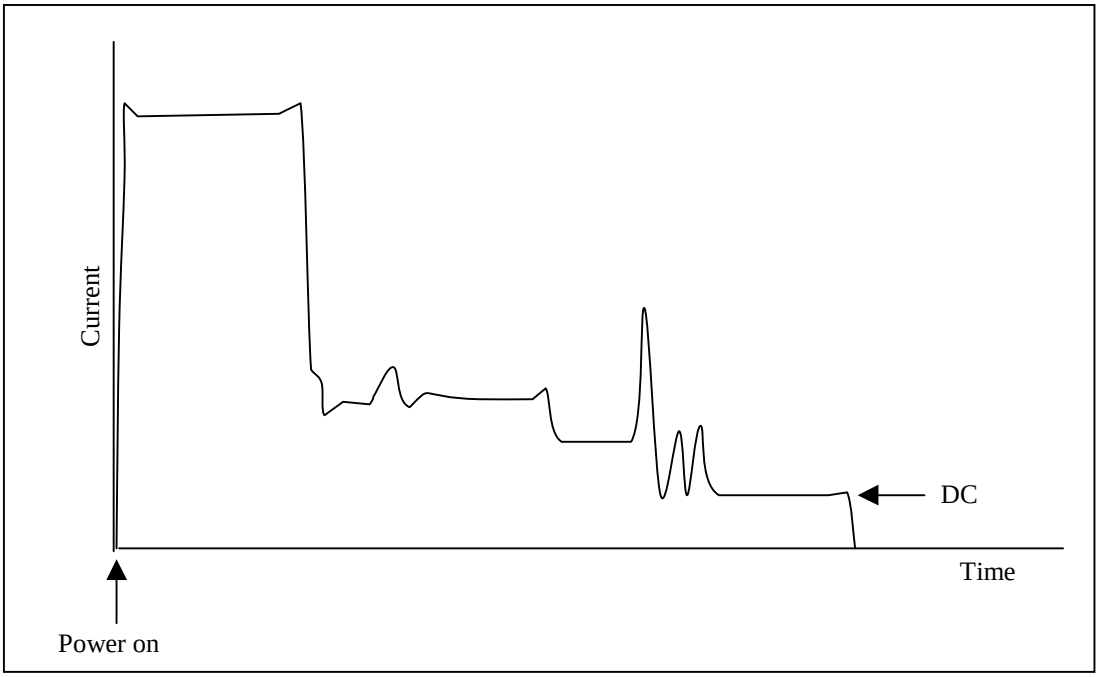
DC Characteristics-4 (Ta = 0 to +60°C, V_{CC} = 3.3 V ± 5%)

(Ta = -40 to +85°C, V_{CC} = 3.3 V ± 5%)

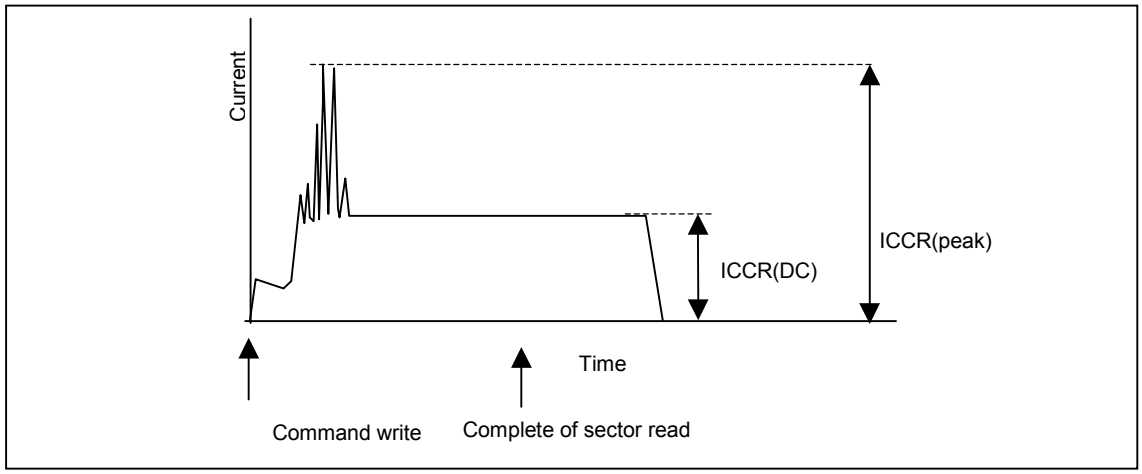
		8MB/16MB 32MB/48MB		64MB/80MB 96MB		112MB/128 MB/160MB			
Parameter	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**	**Test conditions**
Sleep/standby current	I_{SP1}	0.3	0.6	0.4	0.8	0.5	1.0	mA	CMOS level (control signal = V_{CC} – 0.2 V in Memory Card Mode and I/O Card Mode)
Sector read current	I_{CCR} (DC)	25	50	25	50	25	50	mA	CMOS level (control signal = V_{CC} – 0.2 V) during sector read transfer
	I_{CCR} (Peak)	50	80	50	80	50	80		
Sector write current	I_{CCW} (DC)	25	50	25	50	25	50	mA	CMOS level (control signal = V_{CC} – 0.2 V) during sector write transfer
	I_{CCW} (Peak)	50	80	50	80	50	80		

DC Current Waveform (Example of sector read or write: V_{CC} = 5 V, Ta = 25°C)

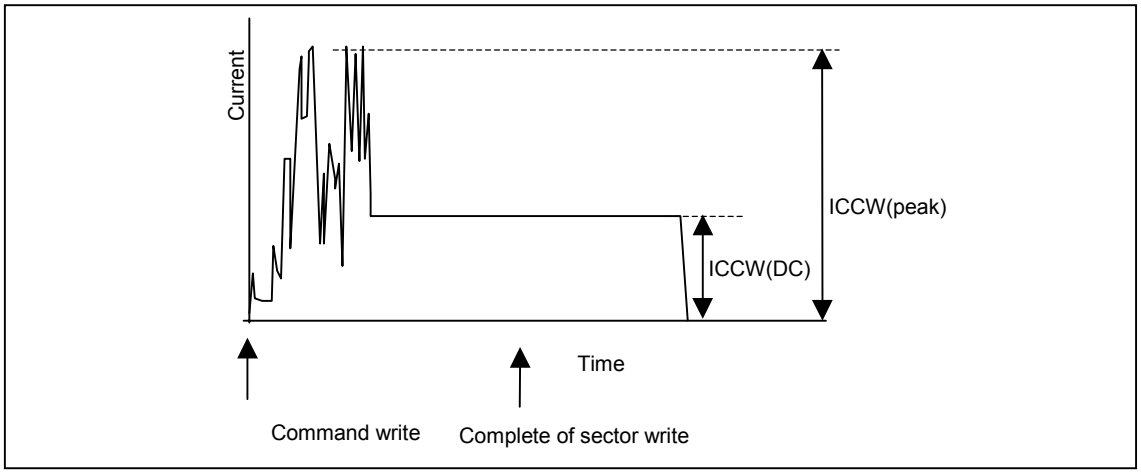
Power on Operation (Reference only)



Sector Read



Sector Write

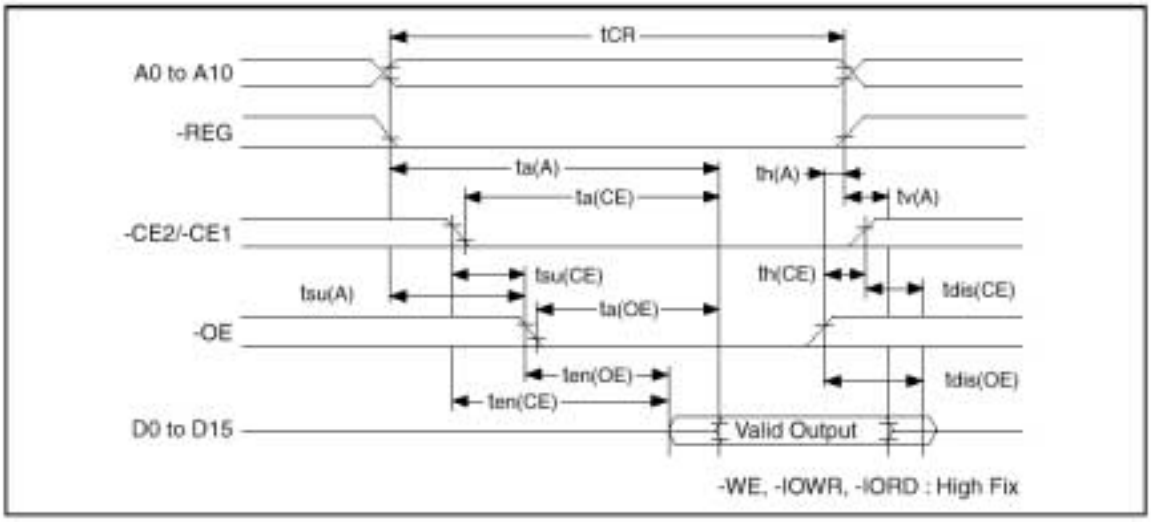


AC Characteristics (Commercial Ta=0 to +60°C, V_{CC} = 5 V ± 10%, V_{CC} = 3.3 V ±5%)
(Industrial Ta= -40 to +85°C, V_{CC} = 5.0 V ± 10%, **V_{CC} = 3.3 V ±5%**)

Attribute Memory Read AC Characteristics

		250 ns			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Read cycle time	tCR	250	—	—	ns
Address access time	ta(A)	—	—	250	ns
-CE access time	ta(CE)	—	—	250	ns
-OE access time	ta(OE)	—	—	125	ns
Output disable time (-CE)	tdis(CE)	—	—	100	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Output enable time (-CE)	ten(CE)	5	—	—	ns
Output enable time (-OE)	ten(OE)	5	—	—	ns
Data valid time (A)	tv(A)	0	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Address hold time	th(A)	20	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

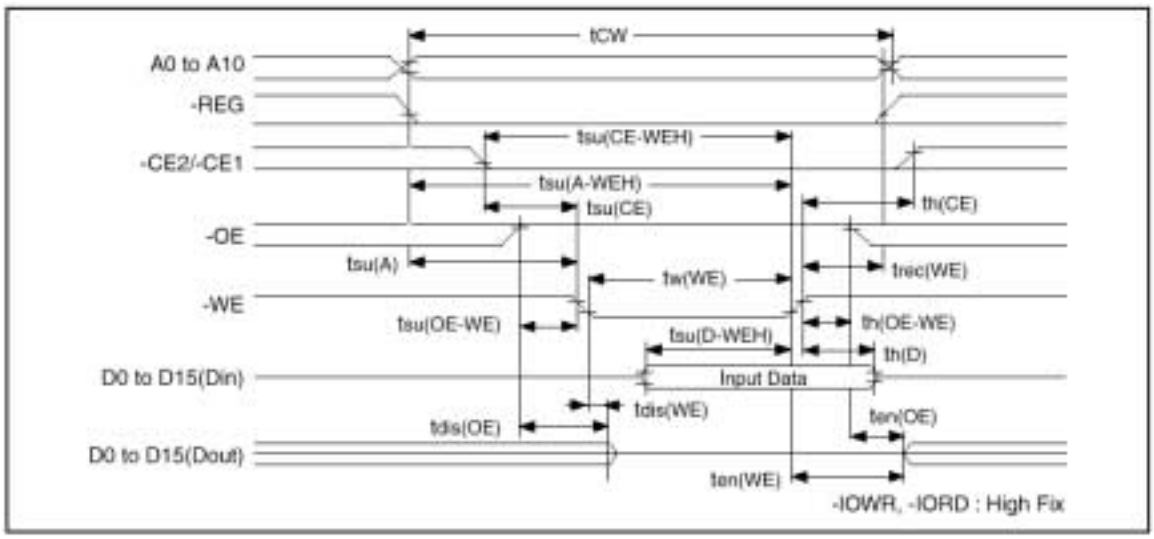
Attribute Memory Read Timing



Attribute Memory Write AC Characteristics

		250 ns			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Write cycle time	tCW	250	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Address setup time (-WE)	tsu(A-WEH)	180	—	—	ns
-CE setup time (-WE)	tsu(CE-WEH)	180	—	—	ns
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
Output disable time (-WE)	tdis(WE)	—	—	100	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Output enable time (-WE)	ten(WE)	5	—	—	ns
Output enable time (-OE)	ten(OE)	5	—	—	ns
Output enable setup time (-WE)	tsu(OE-WE)	10	—	—	ns
Output enable hold time (-WE)	th(OE-WE)	10	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

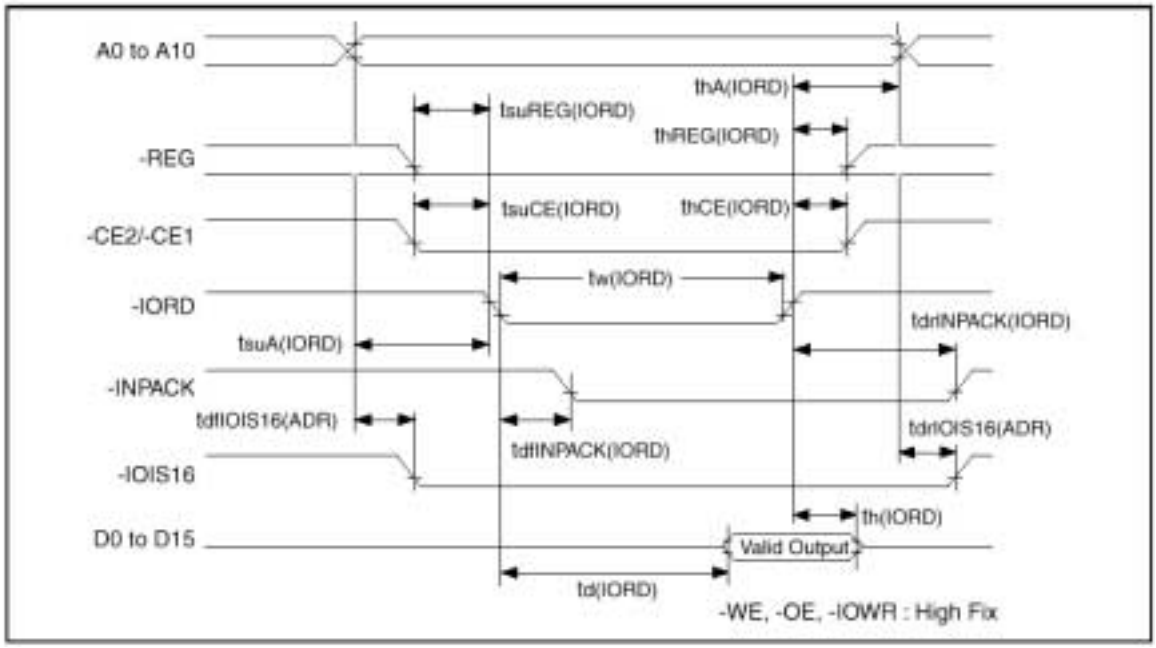
Attribute Memory Write Timing



I/O Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after -IORD	td(IORD)	—	—	100	ns
Data hold following -IORD	th(IORD)	0	—	—	ns
-IORD pulse width	tw(IORD)	165	—	—	ns
Address setup before -IORD	tsuA(IORD)	70	—	—	ns
Address hold following -IORD	thA(IORD)	20	—	—	ns
-CE setup before -IORD	tsuCE(IORD)	5	—	—	ns
-CE hold following -IORD	thCE(IORD)	20	—	—	ns
-REG setup before -IORD	tsuREG(IORD)	5	—	—	ns
-REG hold following -IORD	thREG(IORD)	0	—	—	ns
-INPACK delay falling from -IORD	tdfINPCAK(IORD)	0	—	45	ns
-INPACK delay rising from -IORD	tdrINPACK(IORD)	—	—	45	ns
-IOIS16 delay falling from address	tdfIOIS16(IORD)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(IORD)	—	—	35	ns

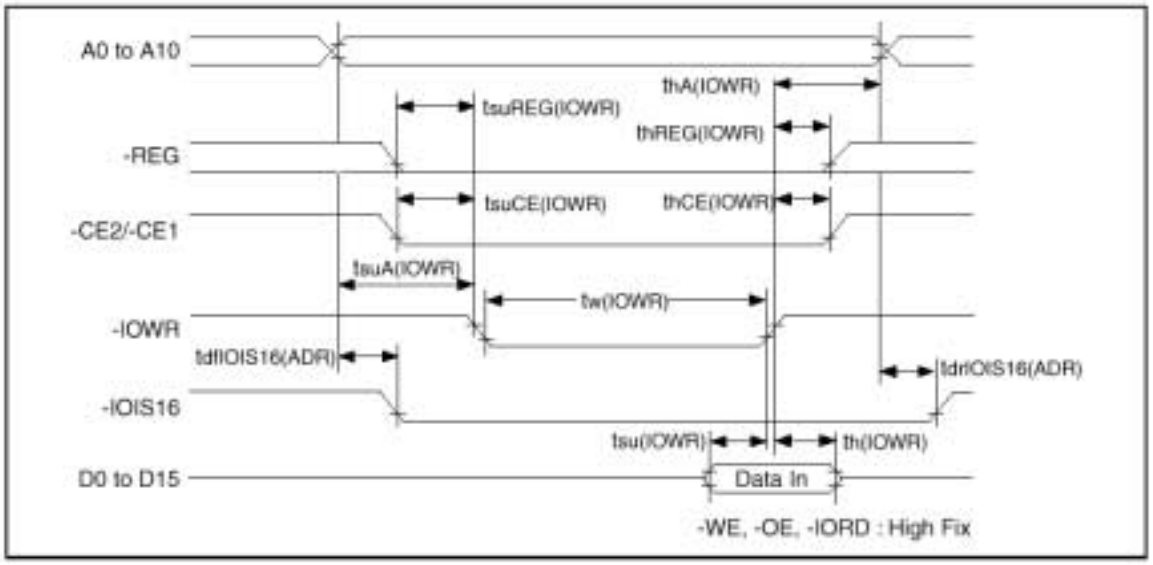
I/O Access Read Timing



I/O Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before -IOWR	tsu(IOWR)	60	—	—	ns
Data hold following -IOWR	th(IOWR)	30	—	—	ns
-IOWR pulse width	tw(IOWR)	165	—	—	ns
Address setup before -IOWR	tsuA(IOWR)	70	—	—	ns
Address hold following -IOWR	thA(IOWR)	20	—	—	ns
-CE setup before -IOWR	tsuCE(IOWR)	5	—	—	ns
-CE hold following -IOWR	thCE(IOWR)	20	—	—	ns
-REG setup before -IOWR	tsuREG(IOWR)	5	—	—	ns
-REG hold following -IOWR	thREG(IOWR)	0	—	—	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

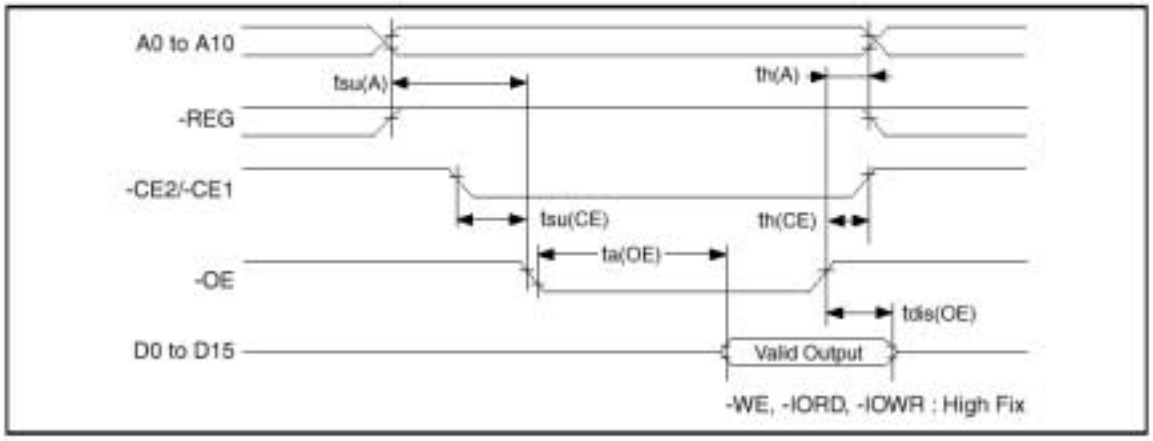
I/O Access Write Timing



Common Memory Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
-OE access time	ta(OE)	—	—	125	ns
Output disable time (-OE)	tdis(OE)	—	—	100	ns
Address setup time	tsu(A)	30	—	—	ns
Address hold time	th(A)	20	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
-CE hold time	th(CE)	20	—	—	ns

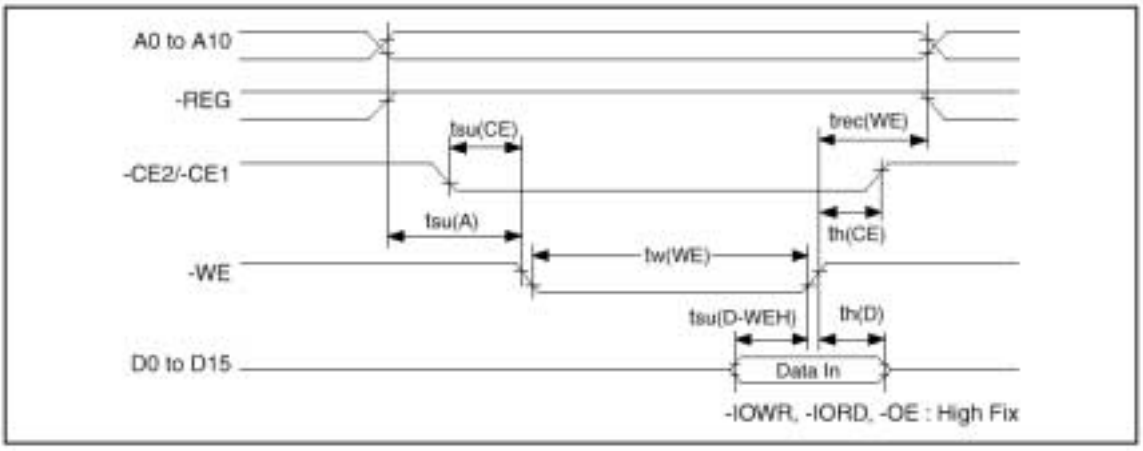
Common Access Read Timing



Common Memory Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
-CE hold following -WE	th(CE)	20	—	—	ns

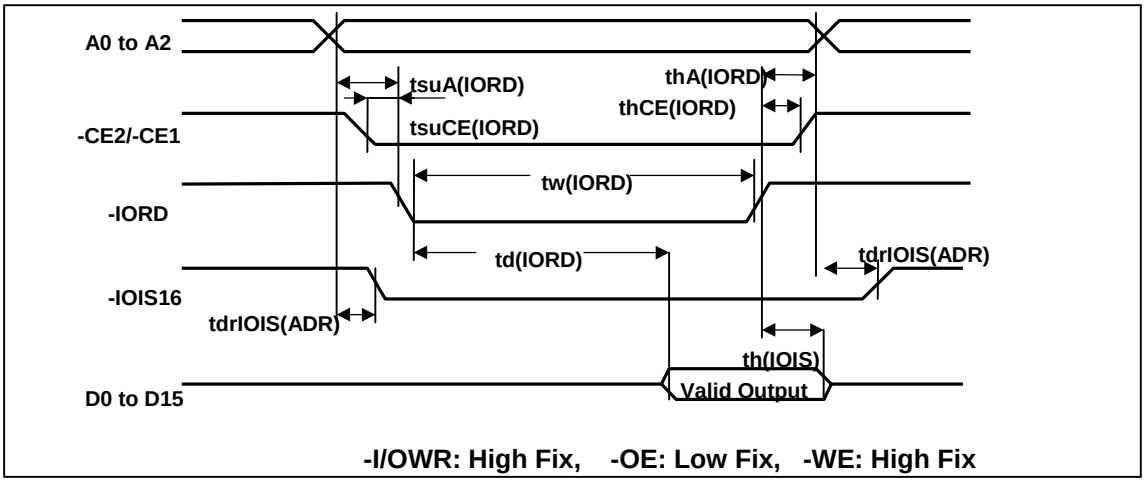
Common Access Write Timing



True IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after IORD	td(IORD)	—	—	100	ns
Data hold follwing IORD	th(IORD)	0	—	—	ns
IORD width time	tw(IORD)	165	—	—	ns
Address setup before IORD	tsuA(IORD)	70	—	—	ns
Address hold following IORD	thA(IORD)	20	—	—	ns
CE setup before IORD	tsuCE(IORD)	5	—	—	ns
CE hold following IORD	thCE(IORD)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdfIOIS16(ADR)	—	—	35	ns

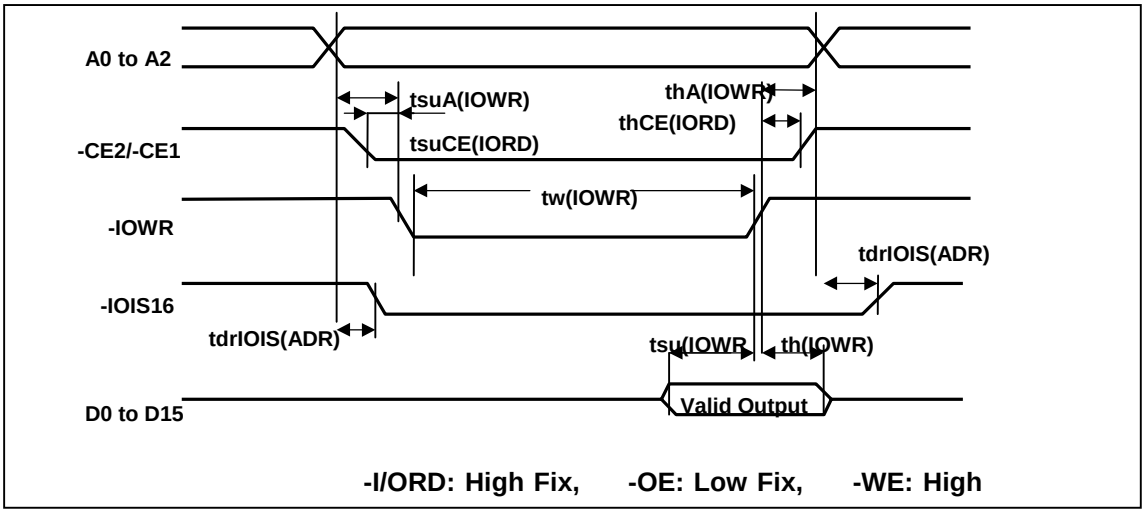
True IDE Mode Access Read Timing



True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	60	—	—	ns
data hold following IOWR	th(IOWR)	30	—	—	ns
IORD width time	tw(IOWR)	165	—	—	ns
address setup before IOWR	tsuA(IOWR)	70	—	—	ns
address hold following IOWR	thA(IOWR)	20	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	5	—	—	ns
CE hold following IOWR	thCE(IOWR)	20	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tdfIOIS16(ADR)	—	—	35	ns

True IDE Mode Access Write Timing

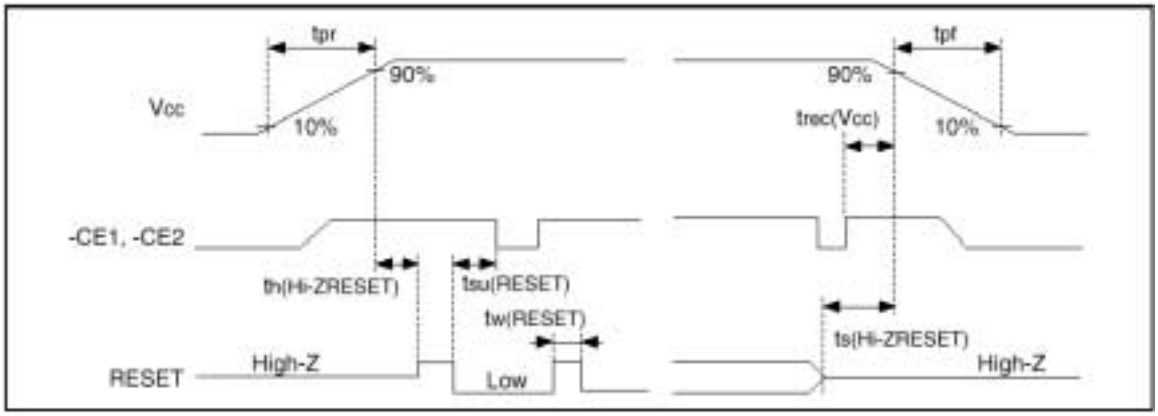


Reset Characteristics (only Memory Card Mode or I/O Card Mode)

Hard Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	µs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	µs	
	th(Hi-ZRESET)	1	—	—	ms	
	ts(Hi-ZRESET)	0	—	—	ms	

Hard Reset Timing

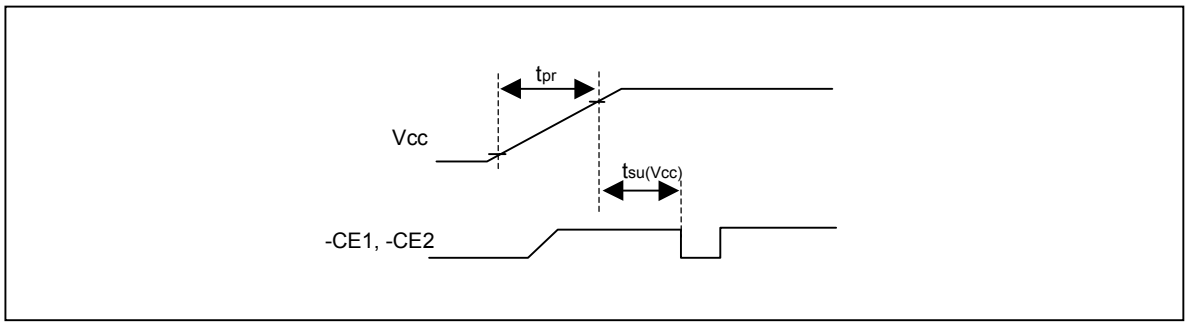


Power on Reset Characteristics

All card status are reset automatically when V_{CC} voltage goes over about 2.3 V.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
-CE setup time	tsu(VCC)	100	—	—	ms	
VCC rising up time	tpr	0.1	—	100	ms	

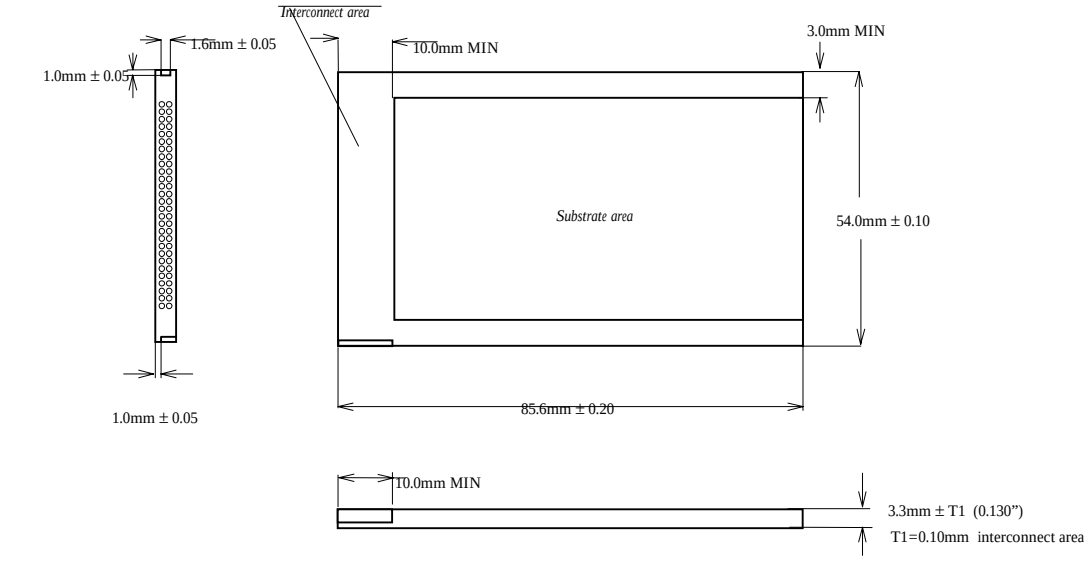
Power on Reset Timing

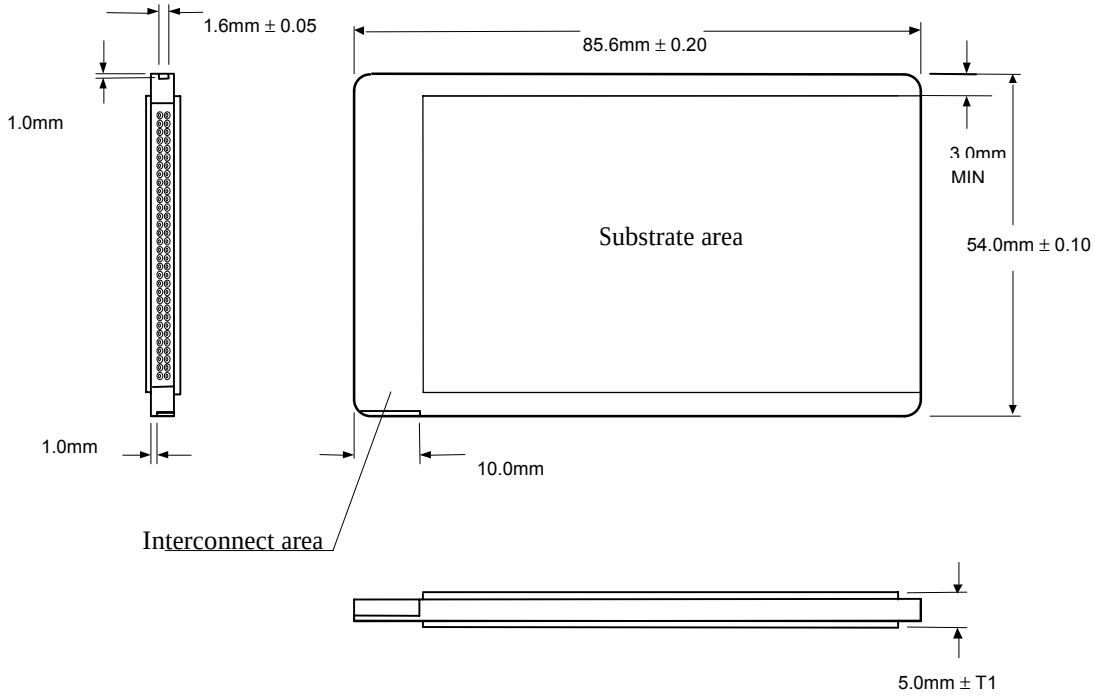


Attention for Card Use

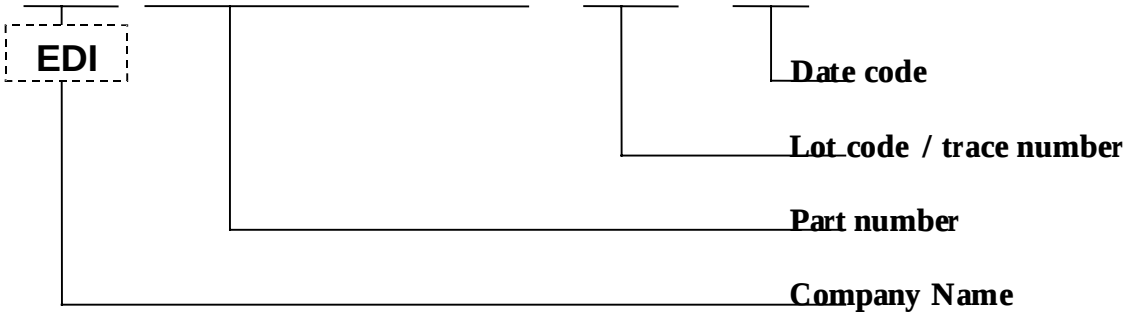
- In the reset or power off, all register information is cleared.
- All card status are cleared automatically when Vcc voltage turns below about 2.5V.
- After the card hard reset, soft reset, or power on reset, the card cannot access during +READY pin is "low" level.
- Please notice that the card insertion/removal should be executed after card internal operations are completed (status register bit 7 turns from "1" to "0").
- Unused pins of data bus (D0 to D15) signals should not be opened.
- V_{CC} should not be supplied to the card until it is completely inserted. After confirmation that the –CD1 and –CD2 pins are inserted V_{CC} can be supplied to the card. Only use drives that will wait until the card is completely inserted to supply V_{CC}.
- -OE must be kept at the V_{CC} level during power on reset in Memory Card Mode. –OE must be kept constantly at the GND level in True IDE Mode.

Physical Outline





PRODUCT MARKING



Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with WED prefix.

PART NUMBERING

7 P 016 ATA2000 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0C to +70C
I	Industrial	-40C to +85C

Packaging option

00	Standard, type 1

Card family and version

- see Card Family and Version Info. for details (next page)

Card capacity

016	16MB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Ordering Information

7P XXX **ATA** YY SS T ZZ

Where

XXX (unformatted capacity):

008	8MB
016	16MB
032	32MB
048	48MB
064	64MB
080	80MB
96	96MB
112	112MB
128	128MB
160	160MB

YY:	20	Standard, 3V/5V: (Controller type = HN)

SS:	00	WEDC Flash ATA logo	Type I
	01	Blank Housing	Type I
	02	Blank Housing	Type I Recessed
	03	WEDC Flash ATA logo	Type II
	04	Blank Housing	Type II
	05	Blank Housing	Type II Recessed

T:	C	Commercial Temperature Range
	I	Industrial Temperature Range

ZZ:	25	250ns

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	June 16, 1998	Initial issue		W. Brys
0.1	January 25, 1999	Card Line up table Card pin explanation changes for WAIT and INPACK New Block Diag and Note CIS changes: reformat CIS and changes in addresses: 004H, 010H, 012H, 050H, 05AH, 070H, 072H, 07AH, 080H, 088H, ATA Command specifications - 5. Identify Drive Information (table) (page 40) Change of data field type information: *word address 1* Change of total bytes: *word address 7 to 8* Change of total default value: *word address 51* DC Characteristics-3 (5 V) Change of test conditions: *CMOS level between* to *CMOS level during* I_{SP1} typ: 0.5 mA to 0.5/0.7/1.0 mA I_{SP1} max: TBD to 1.0/1.5/2.0 mA I_{CCR} (DC) typ: 50 mA to 40/40/40 mA I_{CCR}, I_{CCW} (DC) max: TBD to 75/75/75 mA I_{CCW} (DC) typ: 0.5 mA to 45/45/45 mA I_{CCR}, I_{CCW} (Peak) typ: 100 mA to 80 mA I_{CCR}, I_{CCW} (Peak) max: TBD to 120 mA DC Characteristics-4 (3.3 V) Change of test conditions: *CMOS level between* to *CMOS level during* I_{SP1} typ: 0.3 mA to 0.3/0.4/0.5 mA I_{SP1} max: TBD to 0.6/0.8/1.0 mA I_{CCR}, I_{CCW} (DC) typ: 30 mA to 25/25/25 mA I_{CCR}, I_{CCW} (DC) max: TBD to 50/50/50 mA I_{CCR}, I_{CCW} (Peak) typ: 60 mA to 50/50/50 mA I_{CCR}, I_{CCW} (Peak) max: TBD to 80/80/80 mA Power On Reset Characteristics tsu(RESET), tsu(VCC) min: 250 ms to 100 ms	W. Brys	W. Wrotek
0.2	April 9, 1999	Page 1: add “industrial temp range”	W. Brys	W. Wrotek
0.3	May 14, 1999	Add industrial temp range to the specification Company name change	W. Brys	W. Wrotek
0.4	August 27, 1999	Page 1: Added the 112MB and 128MB capacities and their part numbers to the list of ATA20 series cards. In the Features section, type I housing was added to the specifications to reflect the choice between type I and type II housing. In the Features section, the part number for the Hitachi memory component was changed from HN29W6411 to HN29W6411A, to reflect the new memory component used for these cards. In the features section, the data write endurance was changed from 100,000 cycles to 300,000. This change is resulting from the change in memory	M. Garrett	W. Brys

components.

Page 2: Two rows were added to the Card Line Up to show the values for the new 112MB and 128MB capacities.

Page 17: In the CIS information, at address 050H, the value was changed from 033H from 034H (from 3 to 4 in decimal), to reflect the new revision of the card.

Page 43: "Wait the Command Input" was added to the bottom bubble of the Sector read flow chart. This was previously missing from the chart.

The Sector read timing diagram was converted from a picture to a Microsoft Word Object to decrease file size.

Page 44: The Sector write timing diagram was converted from a picture to a Microsoft Word Object to decrease file size.

Page 45: The data transfer cycle end to ready (Sector write) value was changed from 2ms to 1.2ms (typ.). This change is resulting from the change in memory components.

Page 47: The capacity headings on both the DC Characteristics-3 and DC Characteristics-4 tables changed from 8MB/15MB/30MB/45MB, 60MB/75MB/90MB, and 150MB to 8MB/16MB/32MB/48MB, 64MB/80MB/96MB, and 112MB/128MB/160MB. This change reflects the addition of the 112MB and 128MB capacities, and the change of designations for the other cards, which were labeled with the old capacity values, though the capacities were actually what they are labeled now.

The Test conditions for the Sleep/standby current, for both the DC Charcteristics-3 and DC Characteristics-4 tables have the phrase "in Memory Card Mode and I/O Card Mode" appended to them.

The Sector write current values for each capacity column in the DC Characteristics-3 table were changed from 50/100,TBD/TBD to 45/80,75/120 in mA (DC/Peak for Typ and Max respectively).

Page 48: New waveform (MS Word object) added for Power on Operation, in the DC Current Waveform section.

Page 49: The old waveforms (MS Word objects) for Sector Read Current and Sector Write Current, in the DC Current Waveform section, were replaced with updated waveforms for each.

		Page 57: In the Hard Reset Characteristics table, The minimum value for Reset setup time changed from 250ms to 100ms. Page 59: Under “Attention for Card Use”, the information following the final two bullets was added. Page 60: The Mechanical Drawing for a Type I housing was added to the Physical Outline section, since the cards are now available in a Type I housing. Page 61: Under Ordering Information, The digits needed to order the new 112MB and 128MB capacity cards were added. Under Ordering Information, The digits needed to order cards in a Type I housing were added, since this option was not available before.	
0.5	June 2, 2000	Added Page 61 & 62	M. Garrett

File: F:\Marcom\Data Sheets-New\Data Sheets – Commercial\ATA20 Dsht Rev 5.doc