REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Joseph A. Kerby

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
95-04-14

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, ADVANCED BIPOLAR CMOS, 36-BIT REGISTERED BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-95578
A	67268	

SHEET 1 OF 21

DESC FORM 193
JUL 94

5962-E121-95

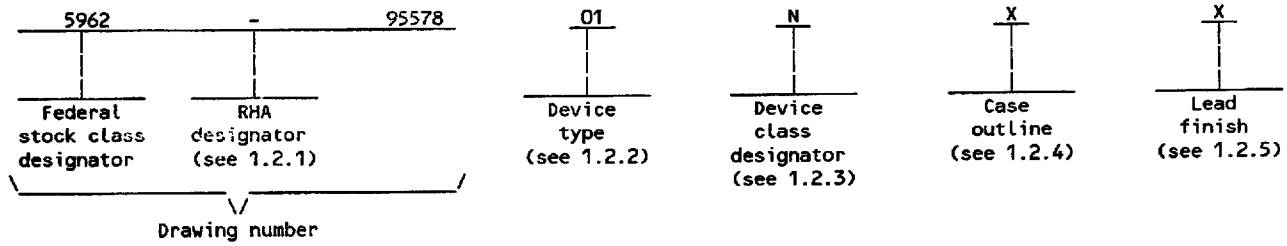
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0012205 638

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ABT32543	36-bit registered bus transceiver with three-state outputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment 1/
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Plastic thin quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference. For device class N, lead finish shall be in accordance with 1.2.5.1 herein.

1/ Any device outside the traditional performance environment; i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.5.1 Lead finish D. Lead finish D shall be designated by a single letter as follows:

Finish letter	Process
D	Palladium

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (except I/O ports) (V_{IN})	-0.5 V dc to +7.0 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to +5.5 V dc 4/
DC output current (I_{OL}) (per output)	+96 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V)	-18 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V)	-50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	11.6°C/W
Junction temperature (T_J)	+175°C
Maximum power dissipation at (at T_A = +55°C in still air) (P_D)	1.2 W 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	+0.8 V
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+48 mA
Maximum input rise or fall rate ($\Delta t/\Delta V$) (outputs enabled)	10 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C unless otherwise noted.

4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.

5/ The maximum packagae power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils.

6/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforsm shall be as specified on figure 5.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes N, Q, and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes N, Q, and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes N, Q, and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 126 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes N, Q, and V, screening shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		V_{CC}	Group A subgroups 3/	Limits 4/ Min	Limits 4/ Max	Unit
High level output voltage 3006	V_{OH}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V	I_{OH} = -3.0 mA	4.5 V	1, 2, 3	2.5		V
				5.0 V	1, 2, 3	3.0		
			I_{OH} = -24.0 mA	4.5 V	1, 2, 3	2.0		
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V I_{OL} = 48 mA		4.5 V	1, 2, 3		0.55	V
Negative input clamp voltage 3022	V_{IC-}	I_{IN} = -18 mA		4.5 V	1, 2, 3		-1.2	V
Input current 3010	I_{IN} 5/	Control inputs For input under test $V_{IN} = V_{CC}$		5.5 V	1, 2, 3		+1.0	µA
		Control inputs For input under test V_{IN} = GND		5.5 V	1, 2, 3		-1.0	
		A or B ports For input under test $V_{IN} = V_{CC}$		5.5 V	1, 2, 3		+20	
		A or B ports For input under test V_{IN} = GND		5.5 V	1, 2, 3		-20	
Three-state output leakage current high 3021	I_{OZH} 6/	$\overline{mOEAB} \ge 2.0$ V, $\overline{mOEBA} \ge 2.0$ V V_{OUT} = 2.7 V		5.5 V	1, 2, 3		10	µA
Three-state output leakage current low 3020	I_{OZL} 6/	$\overline{mOEAB} \ge 2.0$ V, $\overline{mOEBA} \ge 2.0$ V V_{OUT} = 0.5 V		5.5 V	1, 2, 3		-10	µA
High-state leakage current	I_{CEX}	For output under test V_{OUT} = 5.5 V Outputs at high logic state		5.5 V	1, 2, 3		50	µA
Output current 3011	I_{OUT} 7/	V_{OUT} = 2.5 V		5.5 V	1, 2, 3	-50	-180	mA
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 8/	For input under test, V_{IN} = 3.4 V For all other inputs $V_{IN} = V_{CC}$ or GND		5.5 V	1, 2, 3		1	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups 3/	Limits 4/		Unit
					Min	Max	
Quiescent supply current, outputs high 3005	I_{CCH}	For all inputs $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ A$	5.5 V	1, 2, 3		3.0	mA
Quiescent supply current, outputs low 3005	I_{CCL}		5.5 V	1, 2, 3		20	mA
Quiescent supply current, outputs disabled 3005	I_{CCZ}		5.5 V	1, 2 ,3		2	mA
Input capacitance 3012	C_{IN}	Control inputs, $T_C = +25°C$ See 4.4.1b	2.5 V	4		3.5	pF
Input/output capacitance 3012	$C_{I/O}$	A or B ports, $T_C = +25°C$ See 4.4.1b	2.5 V	4		11.5	pF
Low level ground bounce noise	V_{OLP} 9/	$V_{IH} = 2.5\ V$ $V_{IL} = 0.5\ V$ See 4.4.1d See figure 5	5.0 V	4		620	mV
	V_{OLV} 9/		5.0 V	4		-500	
High level V_{CC} bounce noise	V_{OHP} 9/		5.0 V	4		1900	
	V_{OHV} 9/		5.0 V	4		-430	
Functional test 3014	10/	$V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$ Verify output V_O See 4.4.1c	4.5 V and 5.5 V	7,8			
Pulse duration, mLEAB or mLEBA low	t_w	$C_L = 50\ pF$ minimum, $R_L = 500\Omega$ See figure 6	4.5 V and 5.5 V	9, 10, 11	3.3		ns
Setup time, mAn or mBn before mLEAB↑ or mLEBA↑	t_{s1}		4.5 V and 5.5 V	9, 10, 11	2.6		ns
Setup time, mAn or mBn before mCEAB↑ or mCEBA↑	t_{s2}		4.5 V and 5.5 V	9, 10, 11	2.0		
Hold time, mAn or mBn after mLEAB↑ or mLEBA↑	t_{h1}		4.5 V and 5.5 V	9, 10, 11	1.1		ns
Hold time, mAn or mBn after mCEAB↑ or mCEBA↑	t_{h2}		4.5 V and 5.5 V	9, 10, 11	1.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	V_{CC}	Group A subgroups 3/	Limits 4/		Unit
					Min	Max	
Propagation delay time, mAn or mBn to mBn or mAn 3003	t_{PLH1}	C_L = 50 pF minimum, R_L = 500Ω See figure 6	4.5 V and 5.5 V	9, 10, 11	0.5	6.3	ns
	t_{PHL1}		4.5 V and 5.5 V	9, 10, 11	0.5	5.9	ns
Propagation delay time, mLEAB or mLEBA to mBn or mAn 3003	t_{PLH2}		4.5 V and 5.5 V	9, 10, 11	0.8	7.9	ns
	t_{PHL2}		4.5 V and 5.5 V	9, 10, 11	0.8	6.9	
Propagation delay time, output enable, mCEAB or mCEBA to mBn or mAn 3003	t_{PZH1}		4.5 V and 5.5 V	9, 10, 11	0.8	8.3	ns
	t_{PZL1}		4.5 V and 5.5 V	9, 10, 11	1.0	8.8	
Propagation delay time, output disable, mCEAB or mCEBA to mBn or mAn 3003	t_{PHZ1}		4.5 V and 5.5 V	9, 10, 11	0.5	7.4	ns
	t_{PLZ1}		4.5 V and 5.5 V	9, 10, 11	1.0	7.9	
Propagation delay time, output enable, mOEAB or mOEBA to mBn or mAn 3003	t_{PZH2}		4.5 V and 5.5 V	9, 10, 11	0.5	7.6	ns
	t_{PZL2}		4.5 V and 5.5 V	9, 10, 11	1.0	8.2	
Propagation delay time, output disable, mOEAB or mOEBA to mBn or mAn 3003	t_{PHZ2}		4.5 V and 5.5 V	9, 10, 11	0.5	6.7	ns
	t_{PLZ2}		4.5 V and 5.5 V	9, 10, 11	0.8	7.2	

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \geq 3.0$ V.

3/ For device class N, all limits for subgroups 1, 3, 7, 8B, 9 and 11 are guaranteed but not production tested. These limits are characterized at qualification. Production testing is performed at maximum operating temperature.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry.

6/ For I/O ports, the limit includes I_{IN} leakage current from the input circuitry.

7/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

8/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.0 mA, and the preferred method and limits are guaranteed.

9/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 50Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 5). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 5). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

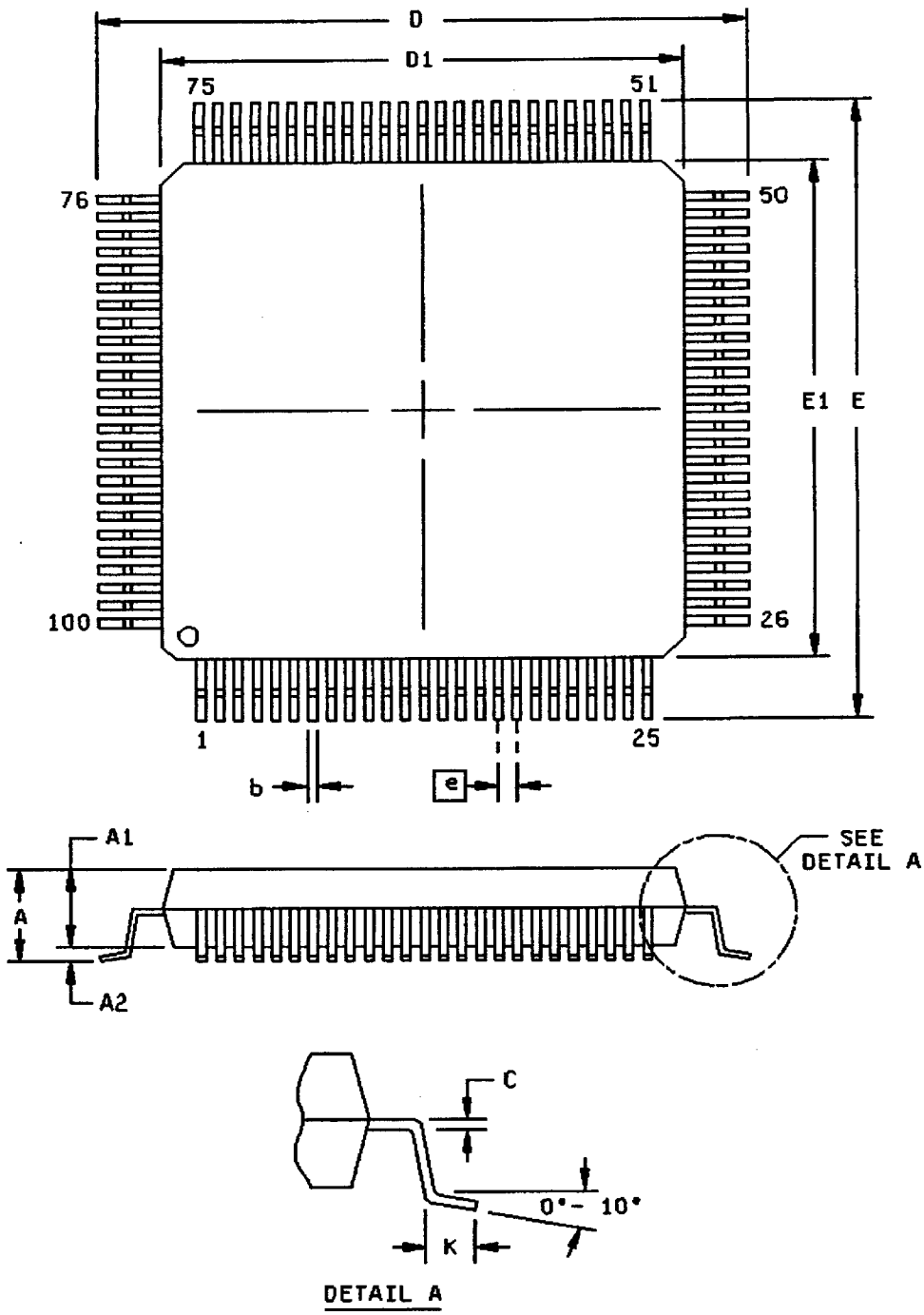


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95578
		REVISION LEVEL	SHEET 10

DESC FORM 193A
JUL 94

9004708 0012214 640

Symbol	Case outline X 1/			Notes
	Min	Nom	Max	
A	- - -	- - -	1.70	
A1	1.35	1.40	1.45	
A2	0.05	0.15	- - -	
D	16.00 BSC.			
D1	14.00 BSC.			2/ 3/
E	16.00 BSC.			
E1	14.00 BSC.			2/ 3/
N	100			
e	0.50 BSC.			
b	0.17	0.22	0.27	4/
c	- - -	0.18	- - -	5/
K	0.40	0.55	0.70	

1/ All dimensions are in millimeters.

2/ The top package body size may be smaller than the bottom package body size by as much as 0.15mm.

3/ Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

4/ Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm.

5/ These dimensions apply to the flat section of the lead.

FIGURE 1. Case outline - Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A9	51	2B10
2	1A10	52	2B9
3	GND	53	GND
4	1A11	54	2B8
5	1A12	55	2B7
6	1A13	56	2B6
7	1A14	57	2B5
8	GND	58	GND
9	1A15	59	2B4
10	1A16	60	2B3
11	1A17	61	2B2
12	1A18	62	2B1
13	V_{CC}	63	V_{CC}
14	2A1	64	1B18
15	2A2	65	1B17
16	2A3	66	1B16
17	2A4	67	1B15
18	GND	68	GND
19	2A5	69	1B14
20	2A6	70	1B13
21	2A7	71	1B12
22	2A8	72	1B11
23	GND	73	GND
24	2A9	74	1B10
25	2A10	75	1B9
26	2A11	76	1B8
27	2A12	77	1B7
28	2A13	78	1B6
29	GND	79	GND
30	2A14	80	1B5
31	2A15	81	1B4
32	2A16	82	1B3
33	2A17	83	1B2
34	2A18	84	1B1
35	$\overline{2CEBA}$	85	$\overline{1CEAB}$
36	$\overline{2OEBA}$	86	$\overline{1OEAB}$
37	2LEBA	87	1LEAB
38	V_{CC}	88	V_{CC}
39	$\overline{2LEAB}$	89	$\overline{1LEBA}$
40	$\overline{2OEAB}$	90	$\overline{1OEBA}$
41	2CEAB	91	1CEBA
42	2B18	92	1A1
43	2B17	93	1A2
44	2B16	94	1A3
45	2B15	95	1A4
46	2B14	96	1A5
47	GND	97	GND
48	2B13	98	1A6
49	2B12	99	1A7
50	2B11	100	1A8

FIGURE 2. Terminal connections.

Pin descriptions	
Terminal symbol	Description
mAn (m = 1 to 2, n = 1 to 18)	Data inputs/outputs, A ports
mBn (m = 1 to 2, n = 1 to 18)	Data inputs/outputs, B ports
$\overline{mCEAB}$/$\overline{mCEBA}$ (m = 1 to 2)	A-to-B/B-to-A chip enable inputs
$\overline{mOEAB}$/$\overline{mOEBA}$ (m = 1 to 2)	A-to-B/B-to-A output enable control inputs
$\overline{mLEAB}$/$\overline{mLEBA}$ (m = 1 to 2)	A-to-B/B-to-A latch enable inputs

FIGURE 2. Terminal connections - Continued.

(each 18-bit section)

Inputs				Outputs
$\overline{mCEAB}$	$\overline{mLEAB}$	$\overline{mOEAB}$	mAn	mBn
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0
L	L	L	L	L
L	L	L	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
B_0 = Output level before the indicated steady-state input conditions were established.

Note: mAn-to-mBn data flow is shown; mBn-to-mAn flow control is the same except that it uses $\overline{mCEBA}$, $\overline{mLEBA}$ and $\overline{mOEBA}$.

FIGURE 3. Truth table.

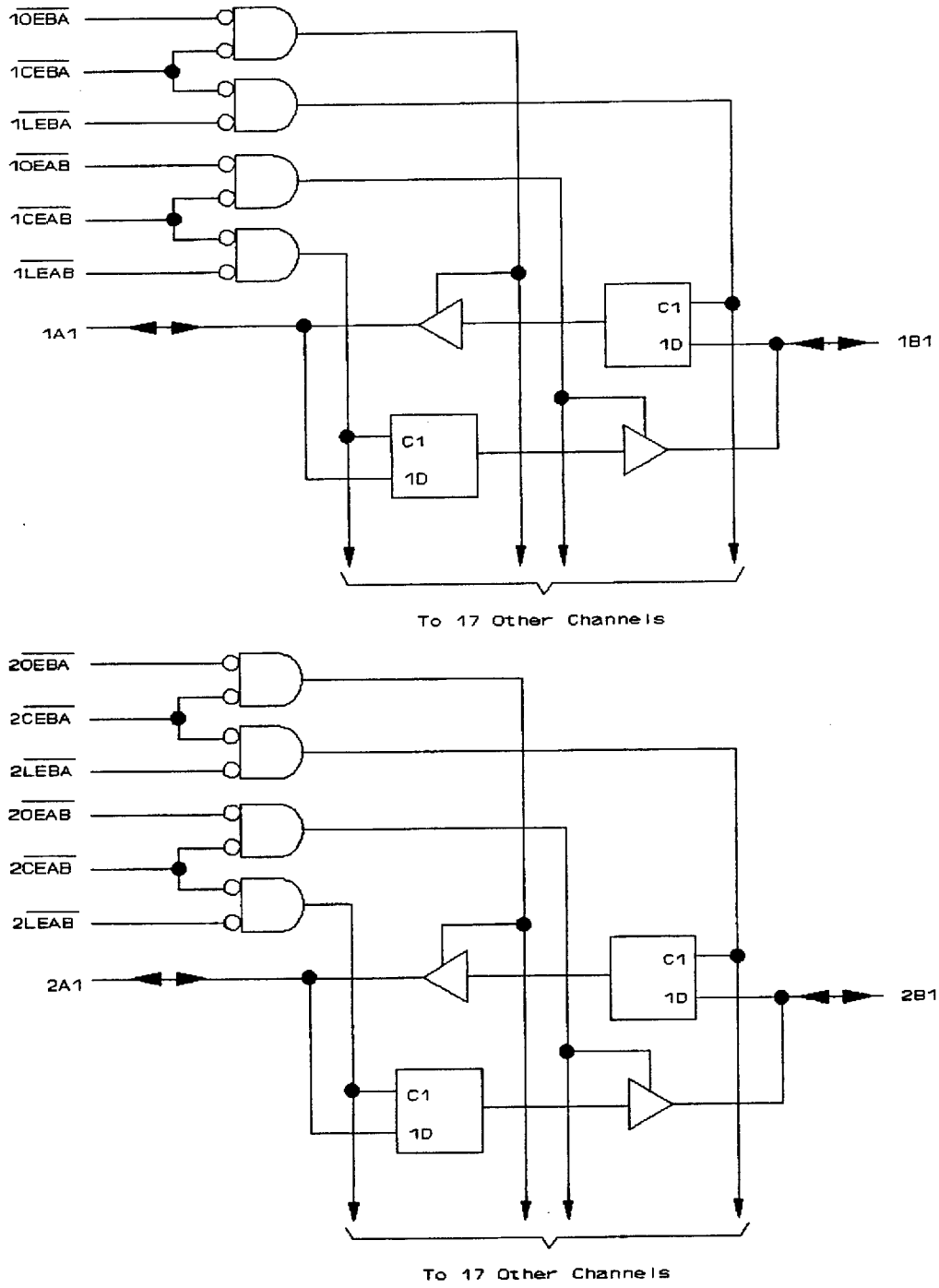
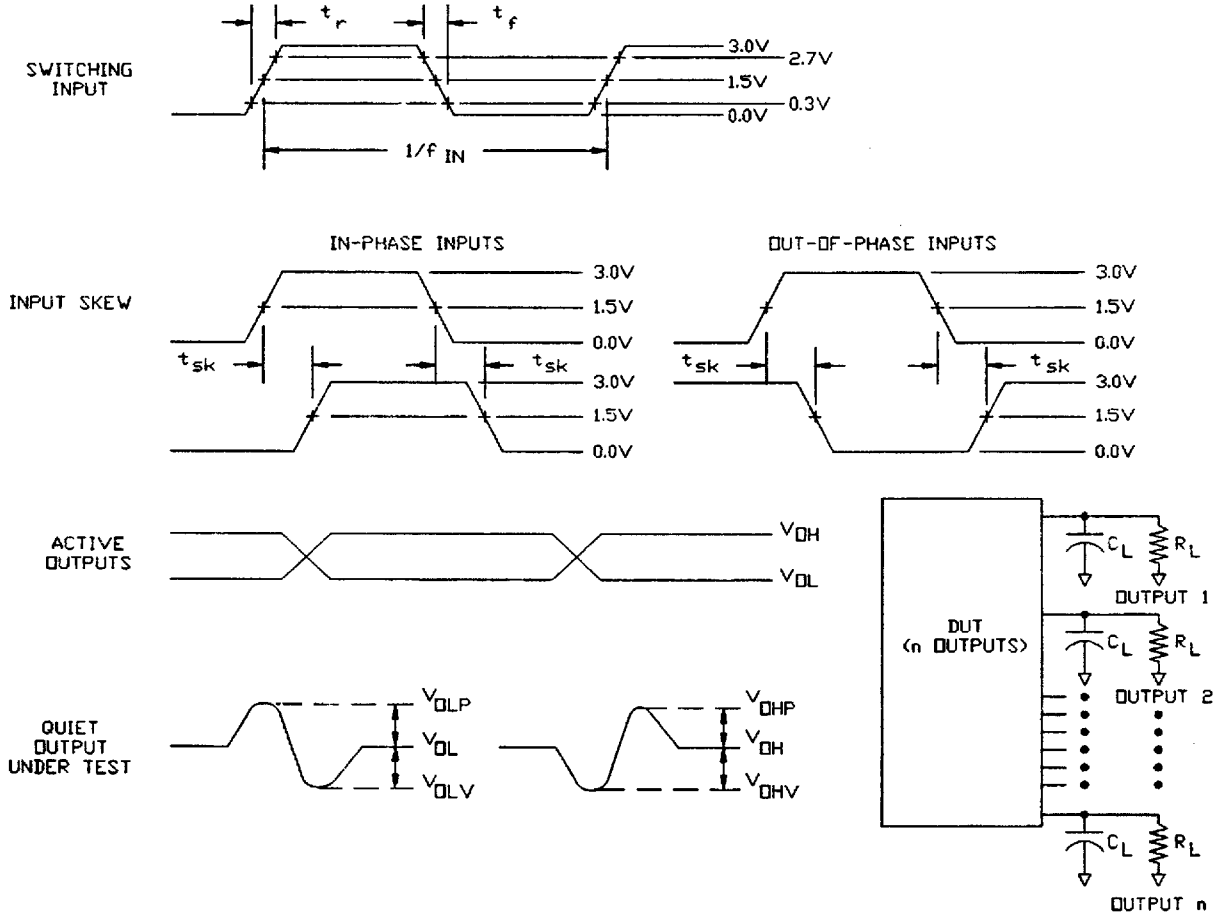


FIGURE 4. Logic diagram.

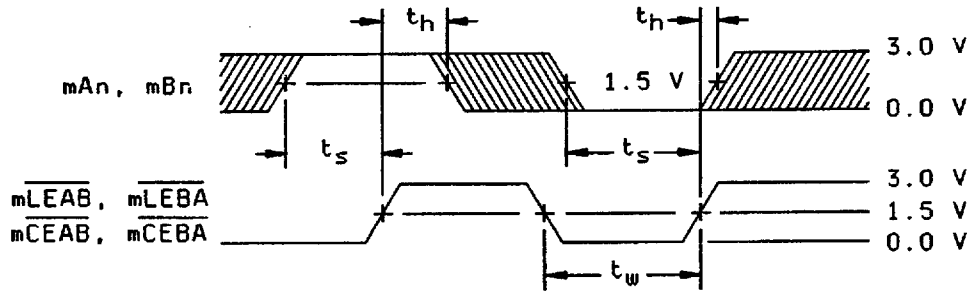


NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 5. Ground bounce load circuit and waveforms.

The shaded areas indicate when the input is permitted to change for a predictable output performance.



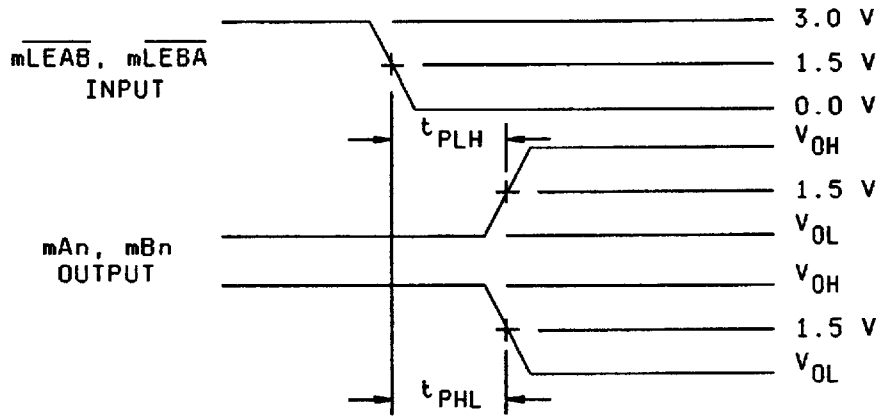
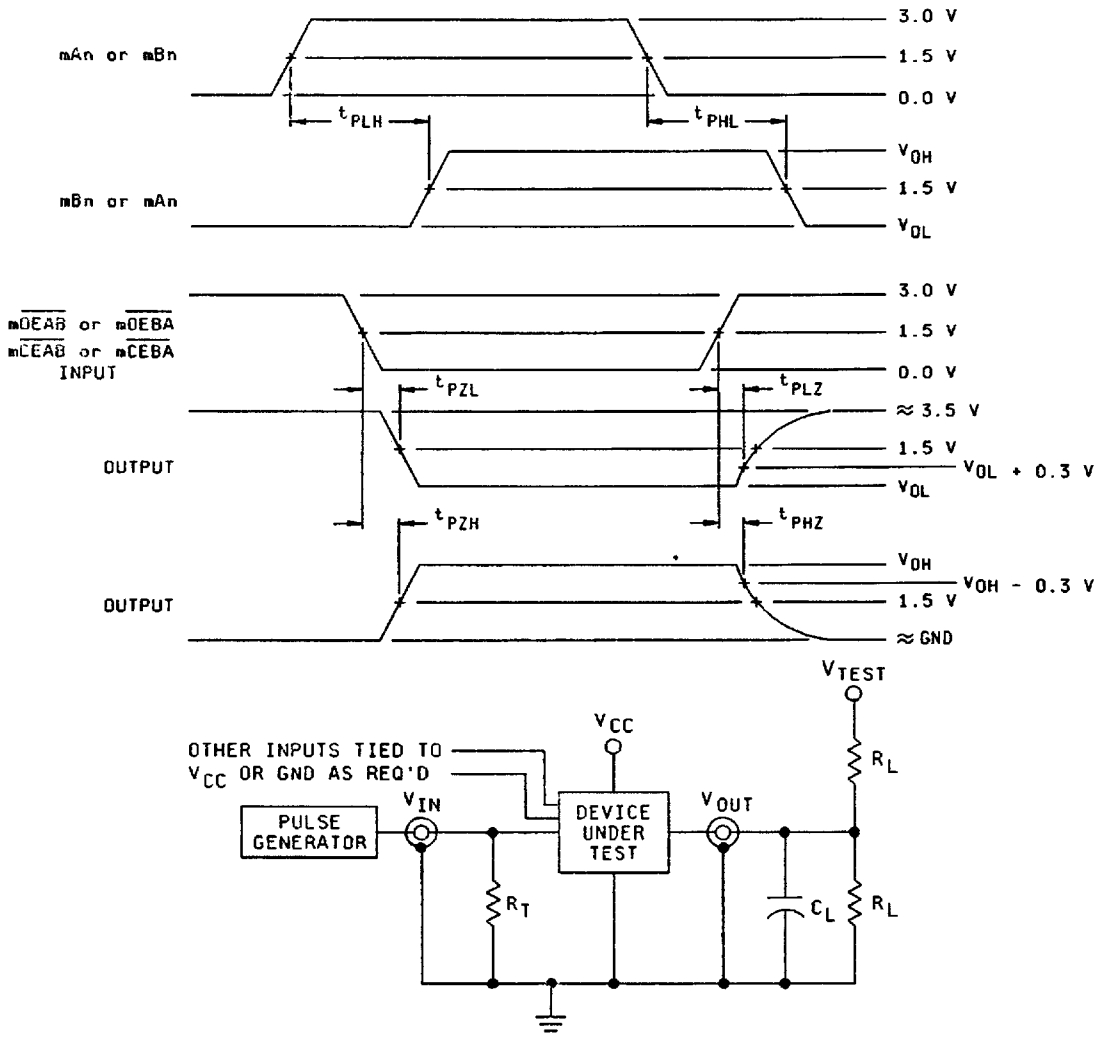


FIGURE 6. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 to 2.7 V and 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 6. Switching waveforms and test circuit - Continued.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections as specified herein and the device manufacturer's QM plan except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN} and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures. All input and output terminals shall be tested.

For C_{IN} and $C_{I/O}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN} and $C_{I/O}$ tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DESC-EC data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DESC-EC of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DESC-EC data from testing on both fixtures, that shall include all measured peak values for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the V_{OHP}, V_{OHV}, V_{OLP}, and V_{OLV} tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DESC-EC the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)		---		1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 2, 8A, 10	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	2, 8A, 10	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	---	1, 2, 3	
Group D end-point electrical parameters (see 4.4)	1, 2, 3	---	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	---	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 and the device manufacturer's QM plan for device classes N, Q, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.