2, 4, and 8MB, STmicro, 5.0V 4Mb Based, Uniform Sector FLASH Module Family

FEATURES

- 2, 4, and 8MB Density FLASH Modules
- Organized as; 512K x 32, 2 x 512K x 32, and 4 x 512K x 32
- Based on STmicro's M29F040B 5.0V FLASH Device
- Base Component DEVICE ID = E2h
- Base Component MANUFACTURERS ID = 20h
- Uniform Sector Architecture
- Sector Erase
- Sector Protection
- Embedded Erase Algorithm
- Embedded Program Algorithm (AMD Compatible)
- Data Polling and Toggle Bit for Detection
- 100,000 Program/Erase Cycles per Block
- 20 Year Data Retention

DESCRIPTION

The WED7F325ZXEBSN, WED7F2325ZXEBSN, and WED7F4325ZXEBSN are organized as 512K x 32, 2 x 512K x 32 and 4 x 512K x 32 respectively. The modules are based on 4Mb TSOP components from STmicro which are mounted onto an FR4 substrate.

The Modules are offered in Access Speeds from 70 to 150ns with an Operation Voltage Requirement of 5.0V ±10%.

PIN CONFIGURATION

PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name
1	V_{SS}	21	(Note 1)	41	A_{11}	61	DQ_9
2	V_{CC}	22	(Note 1)	42	A_{10}	62	DQ_8
3	NC	23	(Note 1)	43	A_9	63	DQ_7
4	$\overline{G}$	24	(Note 1)	44	A_8	64	DQ_6
5	$\overline{W_0}$	25	V_{SS}	45	A_7	65	DQ_5
6	$\overline{W_1}$	26	DQ_{29}	46	A_6	66	DQ_4
7	NC	27	DQ_{30}	47	A_5	67	DQ_3
8	DQ_{16}	28	DQ_{31}	48	A_4	68	DQ_2
9	DQ_{17}	29	$\overline{W_2}$	49	A_3	69	DQ_1
10	DQ_{18}	30	NC	50	A_2	70	DQ_0
11	DQ_{19}	31	NC	51	A_1	71	NC
12	DQ_{20}	32	NC	52	A_0	72	V_{CC}
13	DQ_{21}	33	NC	53	$\overline{W_3}$	73	PD_1
14	DQ_{22}	34	A_{18}	54	V_{SS}	74	PD_2
15	DQ_{23}	35	A_{17}	55	DQ_{15}	75	PD_3
16	DQ_{24}	36	A_{16}	56	DQ_{14}	76	PD_4
17	DQ_{25}	37	A_{15}	57	DQ_{13}	77	PD_5
18	DQ_{26}	38	A_{14}	58	DQ_{12}	78	PD_6
19	DQ_{27}	39	A_{13}	59	DQ_{11}	79	PD_7
20	DQ_{28}	40	A_{12}	60	DQ_{10}	80	V_{SS}

Note 1: Bank Enable

SIMM Density	Pin 24	Pin 23	Pin 22	Pin 21
512K x 32	E_0	NC	NC	NC
2 x 512K x 32	E_0	E_1	NC	NC
4 x 512K x 32	E_0	E_1	E_2	E_3

PRESENCE DETECT PINS; MODULE DENSITY

SIMM Density	Presence Select Pin			
	PD_1	PD_2	PD_3	PD_4
512K x 32	V_{SS}	V_{SS}	V_{SS}	Open
2 x 512K x 32	Open	Open	Open	V_{SS}
4 x 512K x 32	V_{SS}	Open	Open	V_{SS}

PIN NAME, DEFINITION

A_{0-19}	Address Inputs
DQ_{0-31}	Common Data Input / Output
$\overline{W_{0-3}}$	Byte Write Enables
$\overline{E_{0-3}}$	Bank Enable
$\overline{G}$	Output Enable
PD_{0-7}	Presence Detect
NC	No Connect
V_{CC}	Power 5V ±10%
V_{SS}	Ground

PIN CAPACITANCE

Parameter	Sym	Pins	2MB Value	4MB Value	8MB Value
Input Capacitance	Cin	Address	20pF	40pF	80pF
Input Capacitance	Cin	$\overline{G}$	20pF	40pF	80pF
Output Capacitance	Cio	Input / Output Data Bus	5pF	10pF	20pF
Input Capacitance	Cin	$\overline{E_{0-3}}$	20pF	20pF	20pF
Input Capacitance	Cin	$\overline{W_{0-3}}$	5pF	10pF	20pF

ORDERING INFORMATION

2MB, 512K X 32

Part Number	Density	Speed	Package
WED7F325ZXEBSN70C	2MB	70ns	366
WED7F325ZXEBSN90C	2MB	90ns	366
WED7F325ZXEBSN12C	2MB	120ns	366
WED7F325ZXEBSN15C	2MB	150ns	366

8MB, 4 X 512K X 32

Part Number	Density	Speed	Package
WED7F4325ZXEBSN90C	8MB	90ns	368
WED7F4325ZXEBSN12C	8MB	120ns	368
WED7F4325ZXEBSN15C	8MB	150ns	368

4MB, 2 X 512K X 32

Part Number	Density	Speed	Package
WED7F2325ZXEBSN70C	4MB	70ns	367
WED7F2325ZXEBSN90C	4MB	90ns	367
WED7F2325ZXEBSN12C	4MB	120ns	367
WED7F2325ZXEBSN15C	4MB	150ns	367

FIG. 1

FUNCTIONAL BLOCK DIAGRAM
2MB; 512K X 32

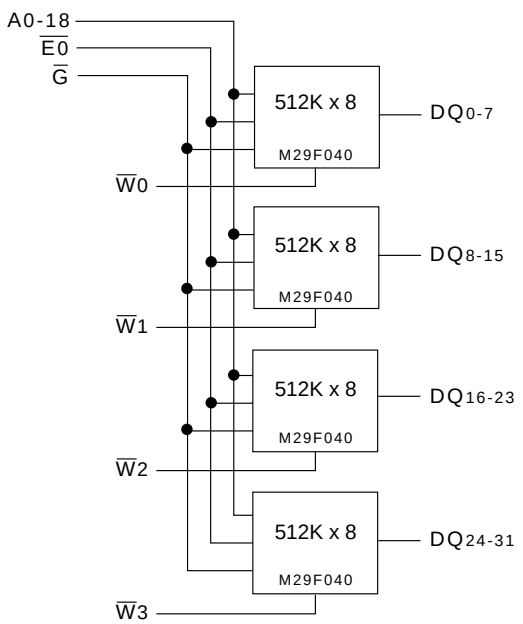

FIG. 2

FUNCTIONAL BLOCK DIAGRAM
4MB; 2 X 512K X 32

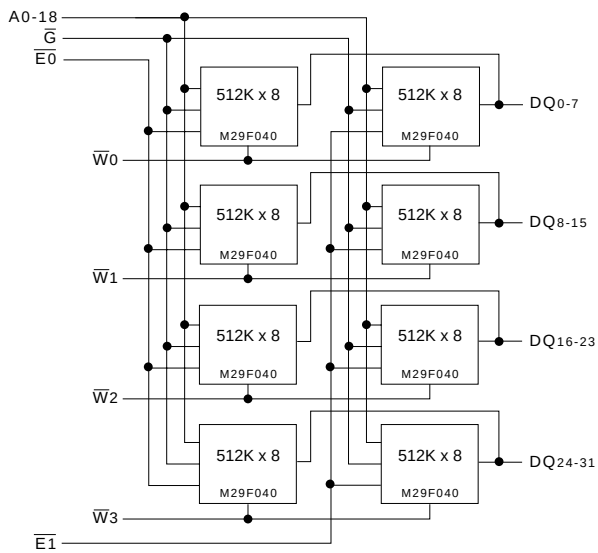

FIG. 3

FUNCTIONAL BLOCK DIAGRAM
8MB; 4 X 512K X 32

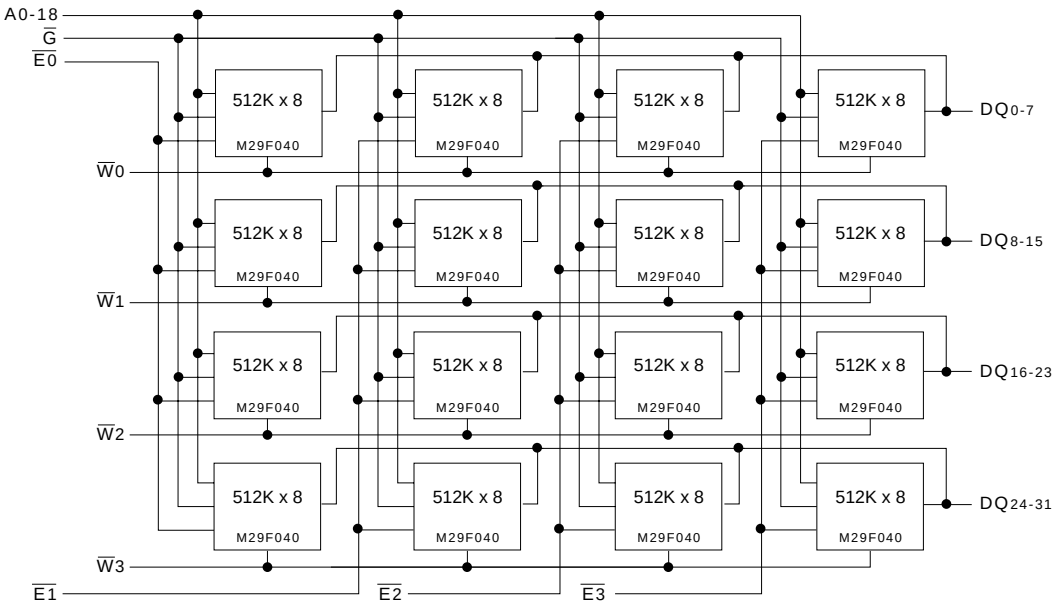

FIG. 4

MECHANICAL; PACKAGE - 366

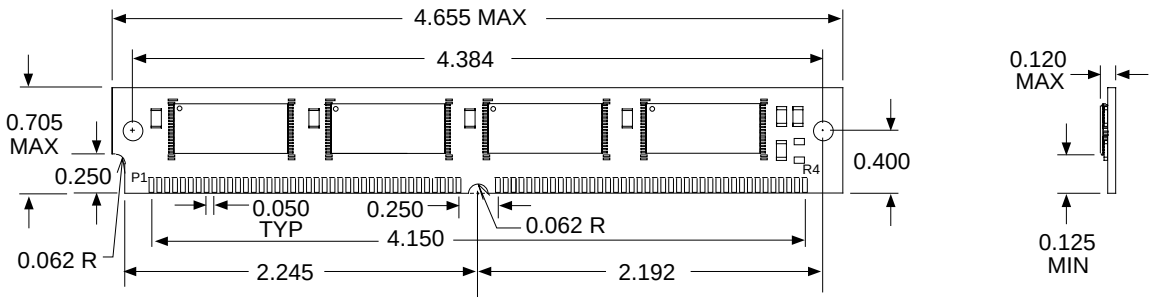

FIG. 5

MECHANICAL; PACKAGE - 367

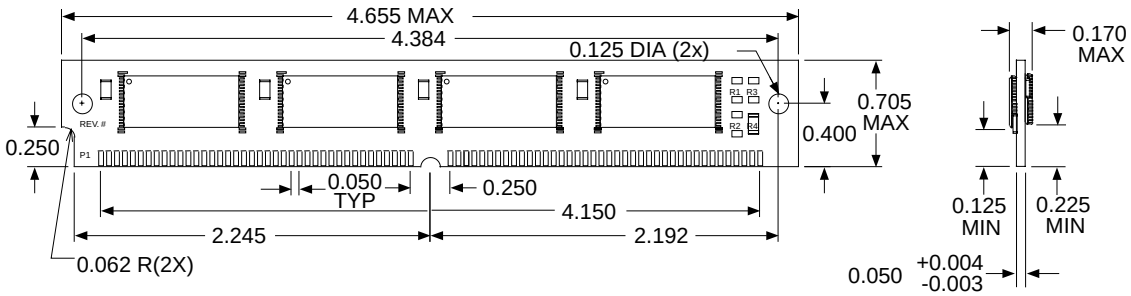

FIG. 6

MECHANICAL; PACKAGE - 368