

TOSHIBA RISC PROCESSOR
TMPR4937XB-300 (TX4937)
(64-bit RISC MICROPROCESSOR)

1. GENERAL DESCRIPTION

The TMPR4937TB, to be referred as TX4937 MIPS RISC micro-controller is a highly integrated ASSP solution based on Toshiba's TX49/H3 processor core, a 64-bit MIPS I,II,III ISA Instruction Set Architecture (ISA) compatible with additional instructions. The TX4937 is a highly integrated device with integrated peripherals such as SDRAM memory controller, PCI controller, PIO, AC-Link, UART and Timer. This class of product is targeted for applications that require a high performance and cost-effective solution such as networking and printers.

2. FEATURES

- TX49/H3 core with an integrated IEEE 754-compliant FPU for single- and double-precision operations
- 4-channel SDRAM Controller (64-bit 133MHz)
- 8-channel External Bus Controller
- 32-bit PCI Controller (32-bit 33 / 66 MHz)
- 8-channel Direct Memory Access (DMA) Controller (4-channel are for ACLC)
- 2-channel Serial I/O Port
- Parallel I/O Port (up to 16-bit)
- 3-channel Timer / Counter
- AC-Link (AC97 Interface)
- Low power dissipation (Typ. 1.5 W)

The TX4937 operates with the 1.5V core and the 3.3V I/O, while supporting a low-power (Halt) mode.

- CPU maximum operating frequency: 300 MHz
- IEEE1149.1 (JTAG) support: Debug Support Unit (Enhanced JTAG)
- **484-pin PBGA (with 64pin thermal ball)**

There are TX4927 and pin compatible nature.

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2.1 Internal Block Diagram

Figure 1 shows the TX4937 internal block diagram.

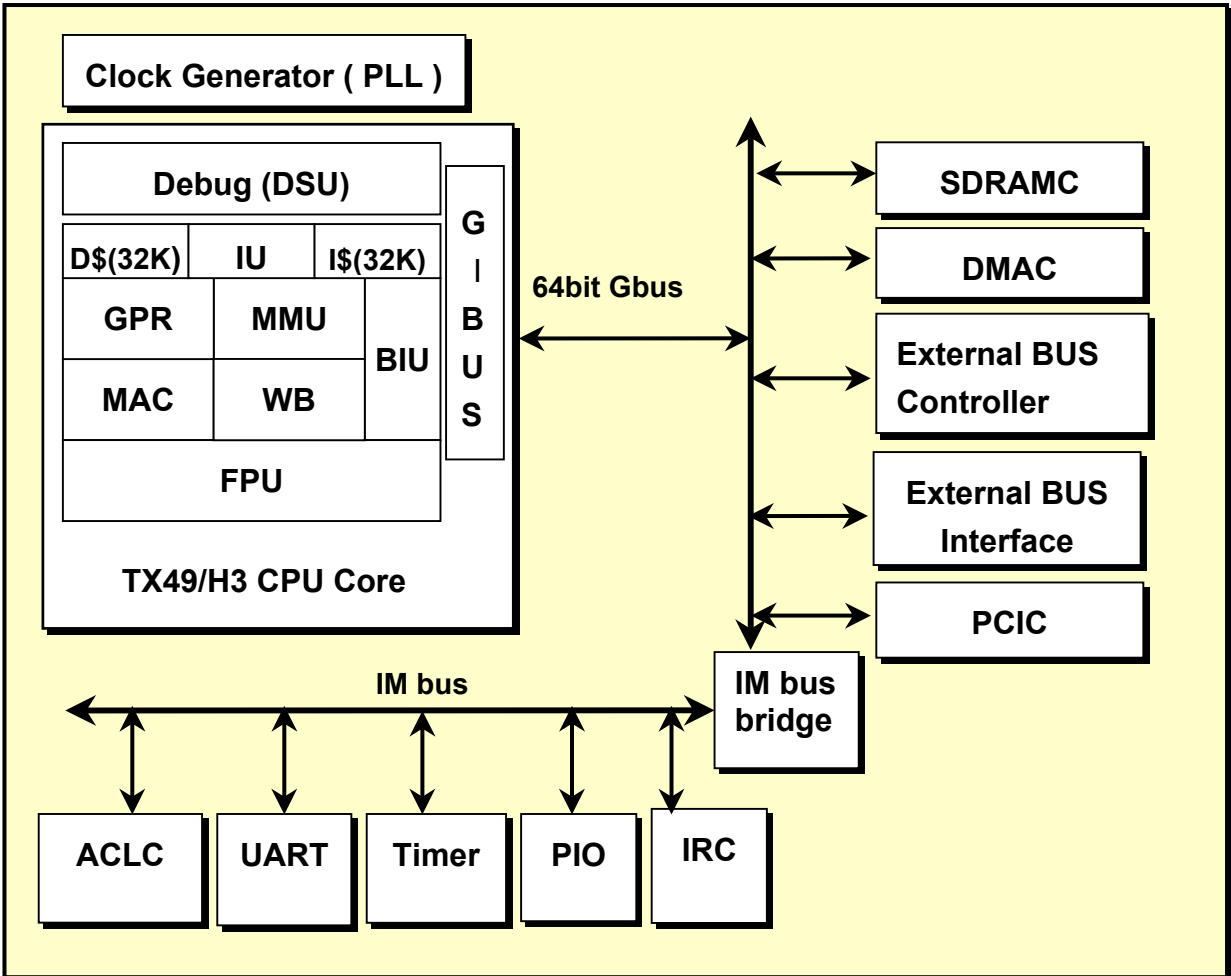


Figure 1 TX4937 Internal Block Diagram

2.2 System Block Diagram

Figure 2 shows the system block diagram with TX4937.

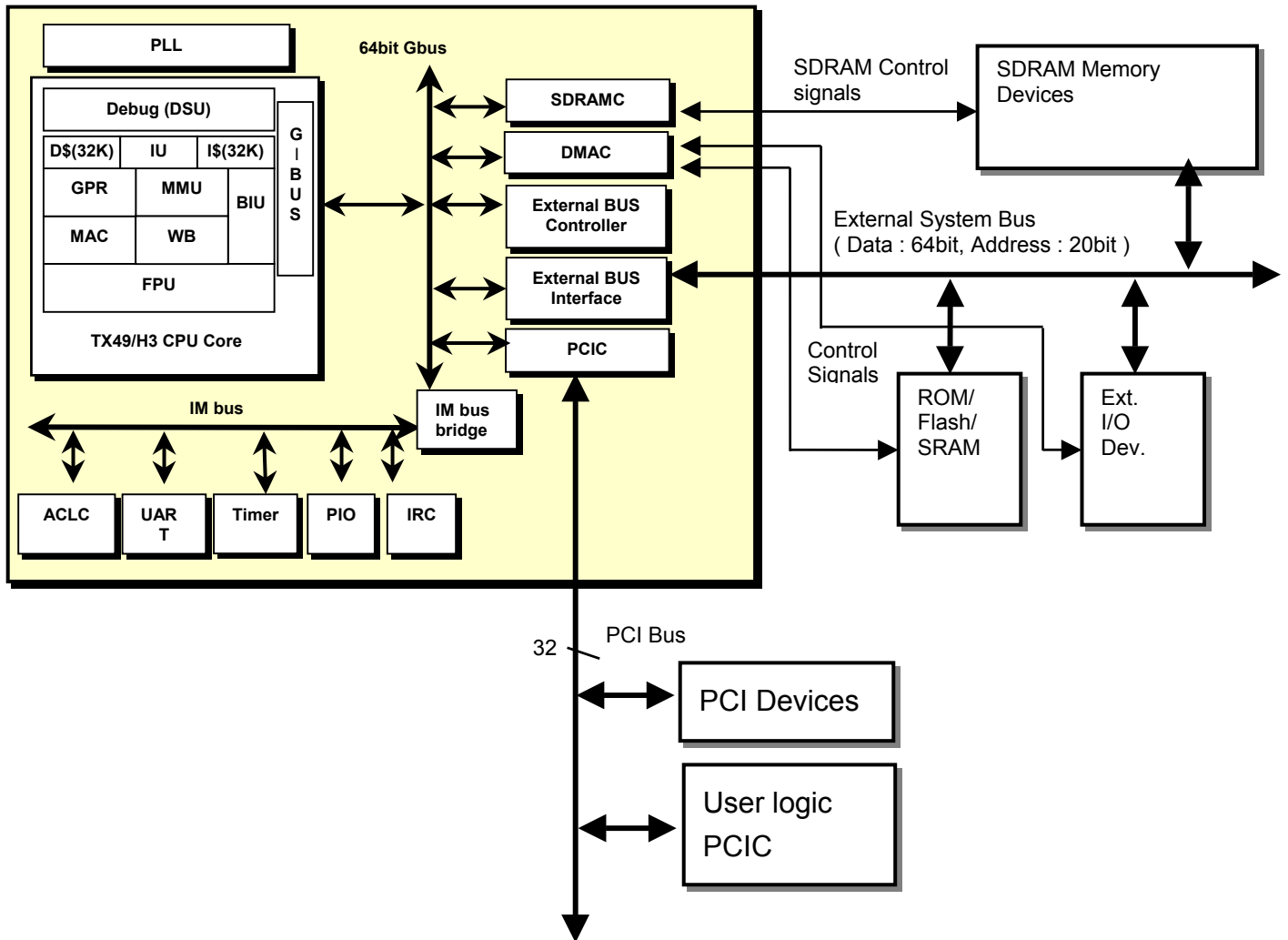


Figure 2 Typical TX4937 System Block Diagram

2.3 TX49/H3 Core Block Diagram

Figure 3 shows the internal block diagram of the TX49/H3 core

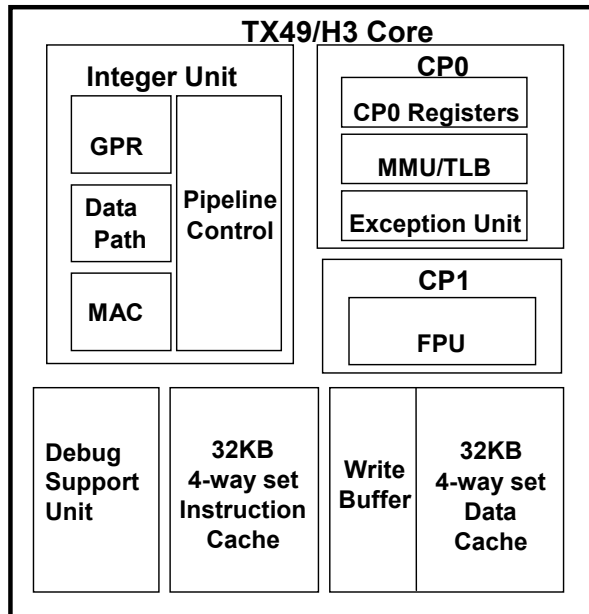


Figure 3 TX49/H3 Core Block Diagram

2.4 TX49/H3 CORE FEATURES

The TX49/H3 Core is high performance and low-power 64-bit RISC processor core developed by Toshiba.

- 64-bit operation
- 32, 64-bit integer general purpose registers
- 32-bit physical address space and 64-bit virtual address space
- Optimized 5-stage pipeline
- Instruction Set
 - MIPS I, II, III compatible ISA
 - PUF (Prefetch) and MAC (Multiply/Accumulate) instructions.
- 32k Byte Instruction Cache, and 32k Byte Data Cache
 - 4-way set associative with lock function
- MMU (Memory Management Unit): 48-entry fully associative JTLB
- The on-chip FPU supports both single- and double-precision arithmetic, as specified in IEEE Std 754.
- On-chip 4-deep write buffer
- Enhanced JTAG debug feature
 - Built-in Debug Support Unit (DSU)

2.5 TX4937 Peripheral Circuit FEATURES

■ External Bus Controller (EBUSC)

The External Bus Controller generates necessary signals to control external memory and I/O devices.

- 8 channels of chip select signals, enabling control of up to eight devices
- Supports access to ROM (including mask ROM, page mode ROM, EPROM and EEPROM), SRAM, flash ROM, **Sync Flash**, and I/O devices
- Supports 32-bit, 16-bit and 8-bit data bus sizing on a per channel basis
- Supports selection among full speed (up to 133MHz), 1/2 speed (up to 66MHz), 1/3 speed (up to 44MHz) and 1/4 speed (up to 33MHz) on a per channel basis
- Support specification of timing on a per channel basis
- The user can specify setup and hold times for address, chip enable, write enable, and output enable signals
- Supports memory sizes of 1M byte to 1G byte for devices with 32-bit data bus, 1M byte to 512M bytes for devices with 16-bit data bus, and 1M byte to 256M bytes for devices with 8-bit data bus

■ DMA Controller (DMAC)

The TX4937 contains a 4-channel DMA controller that executes DMA transfer to memory and I/O devices.

- 4-channel independently handling internal / external DMA requests
- 4-channel independently handling internal request from ACLC
- Supports DMA transfer with built-in serial I/O controller and AC-link controller based on internal DMA requests
- Supports signal address (fly-by DMA) and dual address transfers in external I/O DMA transfer mode using external DMA requests
- Supports transfer between memory and external I/O devices having 32 / 16 / 8-bit data bus
- Supports memory-to-memory copy mode, with no address boundary restrictions
- Supports burst transfer of up to 8 double words for a single read / write
- Supports memory fill mode, writing double-word data to specified memory area
- Supports chained DMA transfer

■ **SDRAM Controller (SDRAMC)**

The SDRAM Controller generates necessary control signals for the SDRAM interface. It has four channels and can handle up to 2G bytes (512 MB/channel) of memory by supporting a variety of memory configurations.

- Memory clock frequency : 66 to 133MHz
- 4 sets of independent memory channels
- Supports 16M / 64M / 128M / 256M / 512M-bit SDRAM with 2/4 bank size availability
- Supports use of Registered DIMM
- Supports ECC or parity generation / check functions
- Supports 64 / 32-bit data bus sizing on a per channel basis
- Supports specification of SDRAM timing on a per channel basis
- Supports critical word first access of TX49/H3 core
- Low power mode : selectable between self-refreshing and pre-charge power-down

■ **PCI Controller (PCIC)**

The TX4937 contains a PCI Controller that complies with PCI Local Bus Specification Revision 2.2.

- Compliance with PCI Local Bus Specification Revision 2.2
- 32-bit PCI interface featuring maximum PCI bus clock frequency of 66MHz
- Supports both target and initiator functions
- Supports change of address mapping between internal bus and PCI bus
- PCI bus arbiter enables connection of up 4 external bus masters
- Supports booting of TX4937 from memory on PCI bus
- 1 channel of DMA controller dedicated to PCI controller (PDMAC)

■ **Serial I/O Controller (UART)**

The TX4937 contains a 2-channels asynchronous serial I/O interface (full duplex UART).

- 2-channel full duplex UART
- Built-in baud rate generator
- FIFOs
- 8-bit x 8 transmitter FIFO
- 13-bit (8 data bits and 5 status bits) x 16 receiver FIFO
- Supports DMA transfer

■ **Timers / Counters Controller (TMR)**

The TX4937 contains 3-channel timer / counters.

- 3-channel 32-bit up-counter
- Supports three modes : interval timer mode, pulse generator mode, and watchdog timer mode
- 2 timer output pins
- 1 count clock input pin
- 1 external watchdog reset signal

■ **Parallel I/O Ports (PIO)**

The TX4937 contains 16-bit parallel I/O ports (including 8 bits shared with CB [7 : 0]).

- Independent selection of direction of pins and output port type (totem-pole or open-drain outputs) on a per bit basis.

■ **AC-link controller (ACLC)**

The TX4937 contains an AC-link controller, which can be operated using any audio and / or modem CODECs described in Audio CODEC'97 Revision 2.1 (AC'97).

- Supports up to two CODECs
- Supports recording and playback for right and left 16-bit PCM channels
- Supports playback for 16-bit surround, center, and LFE channels
- Supports audio recording and playback at variable rate
- Supports Line1 and GPIO slots for modem CODEC
- Supports AC-link low power mode, wakeup, and warm reset
- Supports input / output of sample data by DMA transfer

■ **Interrupt Controller (IRC)**

The TX4937 contains an interrupt controller, which receives interrupt requests sent by both the TX4937's built-in peripherals and external devices and issues interrupt requests to the TX49/H3 core. It has a 16-bit flag register to generate interrupt requests to external devices or the TX49/H3 core.

- Supports 18 internal interrupt sources from built-in peripherals and 6 external interrupt signal inputs
- 8 interrupt priority levels for each interrupt source
- Supports selection between edge- and level-triggered interrupt detection for each external interrupt
- 16-bit read / write flag register for interrupt requests, making it possible to issue interrupt request to external devices and to the TX49/H3 core (IRC interrupts)

■ **Extended EJTAG Interface**

The TX4937 contains an Extended Enhanced Joint Test Action Group (Extended EJTAG) interface, which provides two functions : JTAG boundary scan test that complies with IEEE1149.1 and real-time debugging using a debug support unit (DSU) built into the TX49/H3 core.

- IEEE 1149.1 JTAG Boundary Scan
- Real-time debugging functions using special emulation probe : execution control (execution, break, step, and register / memory access) and PC trace

3. Pins

3.1 Pin designations

| | | | | | | | | | |
|-----|-----------|-----|------------|-----|-----------|-----|-----------|-----|-----------|
| A1 | PIO[1] | B17 | PCIAD[0] | D7 | CE[0]* | E23 | PCIAD[22] | J25 | GNT[0]* |
| A2 | PIO[0] | B18 | PCIAD[3] | D8 | VddIN | E24 | PCIAD[21] | J26 | PCICLK[1] |
| A3 | SWE* | B19 | PCIAD[6] | D9 | Vss | E25 | PCIAD[20] | K1 | RESET* |
| A4 | CE[7]* | B20 | PCIAD[8] | D10 | VddIN | E26 | PCIAD[19] | K2 | TEST[0]* |
| A5 | CE[5]* | B21 | PCIAD[12] | D11 | DMAACK[0] | F1 | INT[2] | K3 | HALTDOZE |
| A6 | CE[4]* | B22 | C_BE[1] | D12 | VddIO | F2 | INT[1] | K4 | VddIN |
| A7 | DMAACK[2] | B23 | PERR* | D13 | TPC[2] | F3 | INT[0] | K5 | Vss |
| A8 | DMAACK[1] | B24 | STOP* | D14 | VddIO | F4 | NMI* | K22 | Vss |
| A9 | BWE[0]* | B25 | FRAME* | D15 | VddIN | F5 | VddIN | K23 | VddIN |
| A10 | BWE[1]* | B26 | Vss | D16 | VddIO | F22 | VddIO | K24 | GNT[1]* |
| A11 | EEPROM_DI | C1 | PIO[5] | D17 | VddIN | F23 | C_BE[3] | K25 | REQ[0]* |
| A12 | EEPROM_DO | C2 | PIO[4] | D18 | PCIAD[4] | F24 | ID_SEL | K26 | PCICLK[2] |
| A13 | Vss | C3 | VddIO | D19 | VddIO | F25 | VddIO | L1 | SYSCLK |
| A14 | EEPROM_SK | C4 | ACK* | D20 | M66EN | F26 | PCIAD[23] | L2 | TEST[4]* |
| A15 | EEPROM_CS | C5 | ACE* | D21 | VddIO | G1 | INT[5] | L3 | TEST[3]* |
| A16 | PCST[3] | C6 | CE[2]* | D22 | SERR* | G2 | INT[4] | L4 | TEST[2]* |
| A17 | PCST[0] | C7 | CE[1]* | D23 | VddIN | G3 | INT[3] | L5 | TEST[1]* |
| A18 | PCIAD[2] | C8 | DMAREQ[3] | D24 | TRDY* | G4 | RXD[0] | L22 | REQ[1]* |
| A19 | PCIAD[5] | C9 | VddIO | D25 | VddIO | G5 | VddIN | L23 | Vss |
| A20 | C_BE[0] | C10 | BWE[3]* | D26 | PCIAD[18] | G22 | PCIAD[28] | L24 | REQ[2]* |
| A21 | PCIAD[11] | C11 | TDI | E1 | TCLK | G23 | PCIAD[27] | L25 | GNT[2]* |
| A22 | PCIAD[15] | C12 | TMS | E2 | TIMER[0] | G24 | PCIAD[26] | L26 | PCICLK[3] |
| A23 | Vss | C13 | TPC[3] | E3 | TIMER[1] | G25 | PCIAD[25] | M1 | OE* |
| A24 | VddIO | C14 | PCST[7] | E4 | VddIO | G26 | PCIAD[24] | M2 | WDRST* |
| A25 | IRDY* | C15 | PCST[4] | E5 | Vss | H1 | TXD[0] | M3 | VddIO |
| A26 | C_BE[2] | C16 | PCST[1] | E6 | SDIN[1] | H2 | RTS[0]* | M4 | VddIN |
| B1 | PIO[3] | C17 | PCIAD[1] | E7 | VddIO | H3 | CTS[0]* | M5 | Vss |
| B2 | PIO[2] | C18 | VddIO | E8 | Vss | H4 | VddIO | M22 | Vss |
| B3 | BUSSPRT* | C19 | PCIAD[7] | E9 | DMADONE* | H5 | Vss | M23 | VddIO |
| B4 | CE[6]* | C20 | PCIAD[9] | E10 | Vss | H22 | Vss | M24 | REQ[3]* |
| B5 | VddIO | C21 | PCIAD[13] | E11 | DMAREQ[0] | H23 | VddIN | M25 | GNT[3]* |
| B6 | CE[3]* | C22 | PAR | E12 | Vss | H24 | PCIAD[29] | M26 | PCICLK[4] |
| B7 | DMAACK[3] | C23 | LOCK* | E13 | TPC[1] | H25 | VddIO | N1 | DATA[1] |
| B8 | DMAREQ[2] | C24 | DEVSEL* | E14 | PCST[6] | H26 | PCICLK[0] | N2 | DATA[32] |
| B9 | DMAREQ[1] | C25 | PCIAD[17] | E15 | Vss | J1 | SCLK | N3 | DATA[0] |
| B10 | BWE[2]* | C26 | PCIAD[16] | E16 | TRST* | J2 | TXD[1] | N4 | Vss |
| B11 | TCK | D1 | PIO[7] | E17 | Vss | J3 | RTS[1]* | N5 | VddIO |
| B12 | DCLK | D2 | Vss | E18 | Vss | J4 | CTS[1]* | N22 | PME* |
| B13 | TDO | D3 | PIO[6] | E19 | Vss | J5 | RXD[1] | N23 | VddIO |
| B14 | PCST[8] | D4 | VddIN | E20 | PCIAD[10] | J22 | PCIAD[31] | N24 | Vss |
| B15 | PCST[5] | D5 | BYPASSPLL* | E21 | PCIAD[14] | J23 | Vss | N25 | DATA[63] |
| B16 | PCST[2] | D6 | Vss | E22 | Vss | J24 | PCIAD[30] | N26 | PCICLK[5] |

| | | | | | | | | | |
|-----|-----------|------|----------|------|----------|------|----------|------|----------|
| P1 | DATA[2] | V3 | VddIO | AB5 | Vss | AC21 | Vss | AE11 | ADDR[9] |
| P2 | Vss | V4 | VddIO | AB6 | DQM[0] | AC22 | DATA[48] | AE12 | Vss |
| P3 | DATA[33] | V5 | DATA[7] | AB7 | VddIO | AC23 | VddIN | AE13 | ADDR[13] |
| P4 | Vss | V22 | VddIO | AB8 | Vss | AC24 | Vss | AE14 | Vss |
| P5 | VddIO | V23 | DATA[28] | AB9 | ADDR[3] | AC25 | DATA[53] | AE15 | ADDR[16] |
| P22 | VddIN | V24 | Vss | AB10 | Vss | AC26 | DATA[22] | AE16 | ADDR[19] |
| P23 | CGRESET* | V25 | DATA[60] | AB11 | ADDR[7] | AD1 | VddIO | AE17 | SDCS[2]* |
| P24 | PLL2Vcc_A | V26 | DATA[29] | AB12 | Vss | AD2 | DATA[46] | AE18 | Vss |
| P25 | PLL2Vss_A | W1 | DATA[8] | AB13 | Vss | AD3 | CB[0] | AE19 | DQM[3] |
| P26 | PCICLKIN | W2 | DATA[39] | AB14 | Vss | AD4 | Vss | AE20 | CB[6] |
| R1 | DATA[35] | W3 | Vss | AB15 | Vss | AD5 | Vss | AE21 | VddIO |
| R2 | DATA[3] | W4 | VddIN | AB16 | ADDR[17] | AD6 | DQM[4] | AE22 | DATA[49] |
| R3 | DATA[34] | W5 | Vss | AB17 | Vss | AD7 | SDCS[1]* | AE23 | Vss |
| R4 | VddIO | W22 | Vss | AB18 | SDCS[3]* | AD8 | Vss | AE24 | VddIO |
| R5 | Vss | W23 | VddIO | AB19 | Vss | AD9 | Vss | AE25 | DATA[20] |
| R22 | Vss | W24 | Vss | AB20 | DQM[7] | AD10 | ADDR[5] | AE26 | VddIO |
| R23 | VddIN | W25 | DATA[27] | AB21 | CB[3] | AD11 | Vss | AF1 | Vss |
| R24 | PLL1Vcc_A | W26 | DATA[59] | AB22 | Vss | AD12 | ADDR[10] | AF2 | DATA[47] |
| R25 | PLL1Vss_A | Y1 | DATA[10] | AB23 | VddIO | AD13 | ADDR[12] | AF3 | CB[1] |
| R26 | MASTERCLK | Y2 | DATA[41] | AB24 | Vss | AD14 | ADDR[14] | AF4 | CAS* |
| T1 | Vss | Y3 | Vss | AB25 | DATA[54] | AD15 | ADDR[15] | AF5 | Vss |
| T2 | DATA[5] | Y4 | DATA[9] | AB26 | Vss | AD16 | ADDR[18] | AF6 | DQM[5] |
| T3 | DATA[36] | Y5 | DATA[40] | AC1 | DATA[14] | AD17 | CKE | AF7 | ADDR[0] |
| T4 | VddIO | Y22 | VddIO | AC2 | Vss | AD18 | DQM[6] | AF8 | ADDR[2] |
| T5 | DATA[4] | Y23 | DATA[25] | AC3 | Vss | AD19 | Vss | AF9 | VddIO |
| T22 | DATA[30] | Y24 | DATA[57] | AC4 | VddIN | AD20 | Vss | AF10 | Vss |
| T23 | DATA[62] | Y25 | DATA[26] | AC5 | VddIO | AD21 | CB[7] | AF11 | VddIO |
| T24 | VddIO | Y26 | DATA[58] | AC6 | Vss | AD22 | DATA[17] | AF12 | ADDR[11] |
| T25 | DATA[31] | AA1 | DATA[43] | AC7 | SDCS[0]* | AD23 | Vss | AF13 | SDCLK[2] |
| T26 | Vss | AA2 | DATA[11] | AC8 | VddIO | AD24 | DATA[50] | AF14 | SDCLK[0] |
| U1 | DATA[38] | AA3 | VddIO | AC9 | VddIO | AD25 | DATA[52] | AF15 | SDCLKIN |
| U2 | DATA[6] | AA4 | Vss | AC10 | VddIN | AD26 | DATA[21] | AF16 | Vss |
| U3 | DATA[37] | AA5 | DATA[42] | AC11 | ADDR[8] | AE1 | DATA[15] | AF17 | SDCLK[3] |
| U4 | VddIN | AA22 | DATA[23] | AC12 | VddIN | AE2 | VddIO | AF18 | Vss |
| U5 | Vss | AA23 | Vss | AC13 | VddIO | AE3 | CB[4] | AF19 | SDCLK[1] |
| U22 | Vss | AA24 | DATA[55] | AC14 | VddIO | AE4 | CB[5] | AF20 | VddIO |
| U23 | VddIN | AA25 | DATA[24] | AC15 | VddIO | AE5 | WE* | AF21 | DATA[16] |
| U24 | VddIO | AA26 | DATA[56] | AC16 | VddIO | AE6 | DQM[1] | AF22 | DATA[18] |
| U25 | DATA[61] | AB1 | DATA[45] | AC17 | VddIN | AE7 | RAS* | AF23 | VddIO |
| U26 | Vss | AB2 | DATA[13] | AC18 | DQM[2] | AE8 | ADDR[1] | AF24 | DATA[19] |
| V1 | Vss | AB3 | DATA[44] | AC19 | VddIN | AE9 | ADDR[4] | AF25 | DATA[51] |
| V2 | Vss | AB4 | DATA[12] | AC20 | CB[2] | AE10 | ADDR[6] | AF26 | Vss |

Thermal Balls for radiation

| | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| K10 | VSS | L15 | VSS | N12 | VSS | P17 | VSS | T14 | VSS |
| K11 | VSS | L16 | VSS | N13 | VSS | R10 | VSS | T15 | VSS |
| K12 | VSS | L17 | VSS | N14 | VSS | R11 | VSS | T16 | VSS |
| K13 | VSS | M10 | VSS | N15 | VSS | R12 | VSS | T17 | VSS |
| K14 | VSS | M11 | VSS | N16 | VSS | R13 | VSS | U10 | VSS |
| K15 | VSS | M12 | VSS | N17 | VSS | R14 | VSS | U11 | VSS |
| K16 | VSS | M13 | VSS | P10 | VSS | R15 | VSS | U12 | VSS |
| K17 | VSS | M14 | VSS | P11 | VSS | R16 | VSS | U13 | VSS |
| L10 | VSS | M15 | VSS | P12 | VSS | R17 | VSS | U14 | VSS |
| L11 | VSS | M16 | VSS | P13 | VSS | T10 | VSS | U15 | VSS |
| L12 | VSS | M17 | VSS | P14 | VSS | T11 | VSS | U16 | VSS |
| L13 | VSS | N10 | VSS | P15 | VSS | T12 | VSS | U17 | VSS |
| L14 | VSS | N11 | VSS | P16 | VSS | T13 | VSS | | |

3.2 Pin layout

| | A | B | C | D | E | F | G | H | J | K | L | M | N | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 26 | A26 | B26 | C26 | D26 | E26 | F26 | G26 | H26 | J26 | K26 | L26 | M26 | N26 | | | |
| 25 | A25 | B25 | C25 | D25 | E25 | F25 | G25 | H25 | J25 | K25 | L25 | M25 | N25 | | | |
| 24 | A24 | B24 | C24 | D24 | E24 | F24 | G24 | H24 | J24 | K24 | L24 | M24 | N24 | | | |
| 23 | A23 | B23 | C23 | D23 | E23 | F23 | G23 | H23 | J23 | K23 | L23 | M23 | N23 | | | |
| 22 | A22 | B22 | C22 | D22 | E22 | F22 | G22 | H22 | J22 | K22 | L22 | M22 | N22 | | | |
| 21 | A21 | B21 | C21 | D21 | E21 | | | | | | | | | | | |
| 20 | A20 | B20 | C20 | D20 | E20 | | | | | | | | | | | |
| 19 | A19 | B19 | C19 | D19 | E19 | | | | | | | | | | | |
| 18 | A18 | B18 | C18 | D18 | E18 | | | | | | | | | | | |
| 17 | A17 | B17 | C17 | D17 | E17 | | | | | | | | K17 | L17 | M17 | N17 |
| 16 | A16 | B16 | C16 | D16 | E16 | | | | | | | | K16 | L16 | M16 | N16 |
| 15 | A15 | B15 | C15 | D15 | E15 | | | | | | | | K15 | L15 | M15 | N15 |
| 14 | A14 | B14 | C14 | D14 | E14 | | | | | | | | K14 | L14 | M14 | N14 |
| 13 | A13 | B13 | C13 | D13 | E13 | | | | | | | | K13 | L13 | M13 | N13 |
| 12 | A12 | B12 | C12 | D12 | E12 | | | | | | | | K12 | L12 | M12 | N12 |
| 11 | A11 | B11 | C11 | D11 | E11 | | | | | | | | K11 | L11 | M11 | N11 |
| 10 | A10 | B10 | C10 | D10 | E10 | | | | | | | | K10 | L10 | M10 | N10 |
| 9 | A9 | B9 | C9 | D9 | E9 | | | | | | | | | | | |
| 8 | A8 | B8 | C8 | D8 | E8 | | | | | | | | | | | |
| 7 | A7 | B7 | C7 | D7 | E7 | | | | | | | | | | | |
| 6 | A6 | B6 | C6 | D6 | E6 | | | | | | | | | | | |
| 5 | A5 | B5 | C5 | D5 | E5 | F5 | G5 | H5 | J5 | K5 | L5 | M5 | N5 | | | |
| 4 | A4 | B4 | C4 | D4 | E4 | F4 | G4 | H4 | J4 | K4 | L4 | M4 | N4 | | | |
| 3 | A3 | B3 | C3 | D3 | E3 | F3 | G3 | H3 | J3 | K3 | L3 | M3 | N3 | | | |
| 2 | A2 | B2 | C2 | D2 | E2 | F2 | G2 | H2 | J2 | K2 | L2 | M2 | N2 | | | |
| 1 | A1 | B1 | C1 | D1 | E1 | F1 | G1 | H1 | J1 | K1 | L1 | M1 | N1 | | | |

| | | | |
|-----|-----|-----|-----|
| K17 | L17 | M17 | N17 |
| K16 | L16 | M16 | N16 |
| K15 | L15 | M15 | N15 |
| K14 | L14 | M14 | N14 |
| K13 | L13 | M13 | N13 |
| K12 | L12 | M12 | N12 |
| K11 | L11 | M11 | N11 |
| K10 | L10 | M10 | N10 |

3.3 Pin Description

Note: In the I/O columns, "PU" indicates an I/O pin with a pull-up resistor, and the term "OD" indicates an open drain output. * denotes an active-low signal when used as a suffix to a signal name.

| Signal Name | Type | Function |
|--|-------------------|---|
| SDRAM / External Bus Interface Common Signals | | |
| ADDR[19:0] | I/O PU | <p>Addresses</p> <p>Address signals.</p> <p>For SDRAM, ADDR[19:5] are used .</p> <p>When the external bus controller uses these pins, the meaning of each bit varies with the data bus width. The ADDR signals are also used as boot configuration signals (input) during a reset.</p> <p>ADDR signals are input signals only when the RESET* signal is asserted and become output signals after the RESET* signal is de-asserted.</p> |
| DATA[63:0] | I/O PU | <p>Data Bus</p> <p>64-bit data bus.</p> <p>The DATA[15:0] signals are also used as boot configuration signals (input) during a reset.</p> |
| BUSSPRT* | O | <p>BUS Separate</p> <p>Controls the connection and separation of devices controlled by the external bus controller to or from a high-speed device, such as SDRAM.</p> <p>H: Separate devices other than SDRAM from the data bus.</p> <p>L: Connect devices other than SDRAM to the data bus.</p> <p>Separation and connection are performed using external bi-directional bus buffers (such as the 74xx245).</p> |

| Signal Name | Type | Function |
|--------------------------------|------------|--|
| SDRAM Interface Signals | | |
| SDCLK[3:0] | O | SDRAM Controller Clock Clock signals used by SDRAM. The clock frequency is the same as the G-Bus clock (GBUSCLK) frequency. When these clock signals are not used, the pins can be set to H using the SDCLK Enable field of the configuration register (CCFG.SDCLKEN[3:0]). |
| SDCLKIN | I/O | SDRAM feedback clock input Feedback clock signal for SDRAM controller input signals. Setting the SDCLKINEN bit of the pin configuration register causes the TX4937 to feed back signals internally, making SDCLKIN an output signal. |
| CKE | O | Clock Enable CKE signal for SDRAM. |
| SDCS[3:0]* | O | Synchronous Memory Device Chip Select Chip select signals for SDRAM. |
| RAS* | O | Row Address Strobe RAS signal for SDRAM. |
| CAS* | O | Column Address Strobe CAS signal for SDRAM. |
| WE* | O | Write Enable WR signal for SDRAM. |

| Signal Name | Type | Function |
|-----------------|-------------------|---|
| DQM[7:0] | O | <p>Data Mask</p> <p>During a read cycle, they control the SDRAM output buffers. The bits correspond to the following data bus signals:</p> <p>DMQ[7] : DATA[63:54], DMQ[6] : DATA[53:48] DMQ[5] : DATA[47:40], DMQ[4] : DATA[39:32] DMQ[3] : DATA[31:24], DMQ[2] : DATA[23:16] DMQ[1] : DATA[15:8], DMQ[0] : DATA[7:0]</p> |
| CB[7:0] | I/O PU | <p>ECC control or Data parity</p> <p>ECC/parity check bit signals. The bits correspond to the following data bus signals:</p> <p>CB[7] : DATA[63:54], CB[6] : DATA[53:48] CB[5] : DATA[47:40], CB[4] : DATA[39:32] CB[3] : DATA[31:24], CB[2] : DATA[23:16] CB[1] : DATA[15:8], CB[0] : DATA[7:0]</p> <p>CB[7:0] share pins with the PIO[15:8] signals for parallel I/O. The boot configuration signal on the ADDR[18] pin selects between PIO[15:8] and CB[7:0].</p> |

| Signal Name | Type | Function |
|---------------------------------------|-------------------------|---|
| External Bus Interface Signals | | |
| SYCLK | O | System Clock Clock for external I/O devices. Outputs a clock in full speed mode (at the same frequency as the G-Bus clock (GBUSCLK) frequency), half speed mode (at one half the GBUSCLK frequency), third speed mode (at one third the GBUSCLK frequency), or quarter speed mode (at one quarter the GBUSCLK frequency). The boot configuration signals on the ADDR[14:13] pins select which speed mode will be used. When this clock signal is not used, the pin can be set to H using the SYCLK Enable bit of the configuration register (CCFG.SYCLKEN). |
| ACE* | O | Address Clock Enable Latch enable signal for the high-order address bits of ADDR. |
| CE [7:0]* | O | Chip Enable Chip select signals for ROM, SRAM, and I/O devices. |
| OE* | O | Output Enable Output enable signal for ROM, SRAM, and I/O devices. |
| SWE* | O | Static RAM Write Enable Write enable signal for SRAM and I/O devices. |
| BWE[3:0]* / BE[3:0]* | O | Byte Write Enable / Byte Enable BE[3:0]* indicate valid data position on the data bus DATA[31:0] at both read and write bus operation. In 16-bit bus mode, BE[1:0]* is only used. In 8-bit bus mode, BE[0]* is only used. BWE[3:0]* indicate valid data position on the data bus DATA[31:0] at write bus operation. In 16-bit bus mode, BWE[1:0]* is only used. In 8-bit bus mode, BWE[0]* is only used. The following shows the correspondence between BE[3:0]*/BWE[3:0]* and the data bus. BE[3]* / BWE[3]* : DATA[31:24] BE[1]* / BWE[1]* : DATA[15:8] BE[2]* / BWE[2]* : DATA[23:16] BE[0]* / BWE[0]* : DATA[7:0] The function of these signals can be selected from BE[3:0]* and BWE[3:0]* by using the DATA[5] signal and the EBCCRn and BC registers in the External Bus Controller during boot-mode configuration. |
| ACK* / READY | I/O PU | Acknowledge Flow control signal. |

| Signal Name | Type | Function |
|----------------------|-------------------|---|
| DMA Interface | | |
| DMAREQ[3:0] | I PU | DMA Request DMA transfer request signals from an external I/O device. The DMAREQ[2] signal shares the pin with the ACRESET* signal. The boot configuration signal on the ADDR[9] pin selects between DMAREQ[2] and ACRESET*. |
| DMAACK[3:0] | O | DMA Acknowledge DMA transfer acknowledge signals to an external I/O device. The DMAACK[2] signal shares the pin with the SYNC signal. The boot configuration signal on the ADDR[9] pin selects between DMAACK[2] and SYNC. |
| DMADONE* | I/O PU | DMA Transfer/Chain Finished DMADONE* is either used as an output signal that reports the termination of DMA transfer or as an input signal that causes DMA transfer to terminate. |

| | | |
|----------------------|------------|---|
| PCI Interface | | |
| PCICLK[5:0] | O | PCI Clock PCI bus clock signals. When these clock signals are not used, the pins can be set to H using the PCICLK Enable field of the pin configuration register (PCFG.PCICLKEN[5:0]). |
| PCICLKIN | I/O | PCI feedback clock input PCI feedback clock input. |
| PCIAD[31:0] | I/O | PCI Address and Data Multiplexed address and data bus. |
| C_BE[3:0]* | I/O | Bus Command and Byte Enable Command and byte enable signals. |

| Signal Name | Type | Function |
|-------------|------|--|
| PAR | I/O | Parity Even parity signal for PCIAD[31:0] and C_BE[3:0]*. |
| FRAME* | I/O | Cycle Indicates that bus operation is in progress. |
| IRDY* | I/O | Initiator ready Indicates that the initiator is ready to complete data transfer. |
| TRDY* | I/O | Target ready Indicates that the initiator is ready to complete data transfer. |
| STOP* | I/O | STOP The target sends this signal to the initiator to request termination of data transfer. |
| LOCK* | I/O | PCI resource clock Indicates that the PCI bus master is locking (exclusively accessing) a specified memory target on the PCI bus. |
| ID_SEL | I | Initialization Device select Chip select signal used for configuration access. |
| DEVSEL* | I/O | Device select The target asserts this signal in response to access from the initiator. |
| REQ[3:2]* | I | Request PCI bus Signals used by the master to request bus mastership. The boot configuration signal on the DATA[2] pin determines whether the built-in PCI bus arbiter is used. In internal arbiter mode, REQ[3:2]* are PCI bus request input signals. In external arbiter mode, REQ[3:2]* are not used. Because the pins are still placed in the input state, they must be pulled up externally. |

| Signal Name | Type | Function |
|-----------------|----------|---|
| REQ[1]* / INOUT | I/O / OD | <p>Request PCI bus</p> <p>Signal used by the master to request bus mastership. The boot configuration signal on the DATA[2] pin determines whether the built-in PCI bus arbiter is used.</p> <p>In internal arbiter mode, this signal is a PCI bus request input signal. In external arbiter mode, this signal is an external interrupt output signal (INTOUT).</p> |
| REQ[0]* | I/O | <p>Request PCI bus</p> <p>Signal used by the master to request bus mastership. The boot configuration signal on the DATA[2] pin determines whether the built-in PCI bus arbiter is used.</p> <p>In internal arbiter mode, this signal is a PCI bus request input signal. In external arbiter mode, this signal is a PCI bus request output signal.</p> |
| GNT[3:0]* | I/O | <p>Grant PCI bus</p> <p>Indicates that bus mastership has been granted to the PCI bus master. The boot configuration signal on the DATA[2] pin determines whether the built-in PCI bus arbiter is used.</p> <p>In internal arbiter mode, all of GNT[3:0]* are PCI bus grant output signals. In external arbiter mode, GNT[0]* is a PCI bus grant input signal. Because GNT[3:1]* also become input signals, they must be pulled up externally.</p> |
| PERR* | I/O | <p>Data Parity Error</p> <p>Indicates a data parity error in a bus cycle other than special cycles.</p> |
| SERR* | I/OD | <p>System Error</p> <p>Indicates an address parity error, a data parity error in a special cycle, or a fatal error.</p> <p>In host mode, SERR* is an input signal. In satellite mode, SERR* is an open-drain output signal. The mode is determined by the boot configuration signal on the ADDR[19] pin.</p> |

| Signal Name | Type | Function |
|-------------|-----------|--|
| M66EN | I/O | 66MHz clock enable 1: Enable 66 MHz operating mode. 0: Disable 66 MHz operating mode. In host mode, M66EN is an input signal. In satellite mode, M66EN is an output signal. The mode is determined by the boot configuration signal on the ADDR[19] pin. |
| PME* | I / OD | Power management event PME* indicates the power management mode. In host mode, PME* is an input signal. In satellite mode, PME* is an open-drain output signal. The mode is determined by the boot configuration signal on the ADDR[19] pin. |
| EEPROM_DI | I PU | EEPROM data in This is a data input signal from a serial EEPROM for PCI configuration. |
| EEPROM_DO | O | EEPROM data out This is a data output signal to a serial EEPROM for PCI configuration. |
| EEPROM_CS | O | EEPROM chip select This is a chip select signal for a serial EEPROM for PCI configuration. |
| EEPROM_SK | O | EEPROM SK This is a clock signal for a serial EEPROM for PCI configuration. |

| Timer Interface | | |
|-----------------|---------|--|
| TIMER[1:0] | O | Timer Pulse Width Output Timer output signal. |
| TCLK | I PU | External Timer Clock Timer input clock. TMR0, TMR1 and TMR2 share this signal. |
| WDRST* | OD | Watchdog Reset Watchdog reset output signal. |

| Signal Name | Type | Function |
|----------------------|-------------|---|
| SIO Interface | | |
| CTS[1:0]* | I PU | SIO Clear to Send CTS signals. |
| RTS[1:0]* | O | SIO Request to Send RTS signals. |
| RXD[1:0] | I PU | SIO Receive Data Serial data input signal. |
| TXD[1:0] | 3state O | SIO Transmit Data Serial data output signal. |
| SCLK | I PU | External Serial Clock Input clock for SIO0 and SIO1. SIO0 and SIO1 share this signal. |

| | | |
|----------------------|-----------|--|
| PIO Interface | | |
| PIO[15:8] | I/O PU | PIO Ports Parallel I/O signals. PIO[15:8] share pins with the SDRAM ECC/parity signals (CB[7:0]). The boot configuration signal on the ADDR[18] pin selects between PIO[15:8] and CB[7:0]. |
| PIO[7:0] | I/O PU | PIO Ports Parallel I/O signals. PIO[4:2] share pins with the AC-link interface signals (SDOUT, SDIN[0], and BITCLK). The boot configuration signal on the ADDR[9] pin selects between PIO[4:2] and AC-link interface signals. |

| Signal Name | Type | Function |
|--------------------------|----------|--|
| AC-Link Interface | | |
| ACRESET* | O | AC '97 Master H/W Reset ACRESET* shares the pin with the DMAREQ[2] signal. The boot configuration signal on the ADDR[9] pin selects between ACRESET* and DMAREQ[2].PIO[15:8] and CB[7:0]. |
| SYNC | O | 48 kHz Fixed Rate Sample Sync SYNC shares the pin with the DMAACK[2] signal. The boot configuration signal on the ADDR[9] pin selects between SYNC and DMAACK[2]. |
| SDOUT | O | Serial, Time Division Multiplexed, AC '97 Output Stream SDOUT shares the pin with the PIO[4] signal. The boot configuration signal on the ADDR[9] pin selects between SDOUT and PIO[4]. |
| SDIN[1] | I | Serial, Time Division Multiplexed, AC '97 Input Stream |
| SDIN[0] | I | Serial, Time Division Multiplexed, AC '97 Input Stream SDIN[0] shares the pin with the PIO[3] signal. The boot configuration signal on the ADDR[9] pin selects between SDIN[0] and PIO[3]. |
| BITCLK | I | Serial, Time Division Multiplexed, AC '97 Input Stream BITCLK shares the pin with the PIO[2] signal. The boot configuration signal on the ADDR[9] pin selects between BITCLK and PIO[2]. |

| Interrupt Signals | | |
|--------------------------|-----------------------|---|
| NMI* | I PU | Non Mask-able Interrupt Non-Mask-able interrupt input. |
| INT[5:0] | I PU | External Interrupt Requests The external interrupt request signals. |

| Signal Name | Type | Function |
|------------------------------|-----------------|--|
| EJTAG Debug Interface | | |
| TCK | I PU | JTAG clock input Clock input signal for JTAG. TCK is used to execute JTAG instructions and input/output data. |
| TDI / DINT* | I PU | JTAG data input / Debug interrupt input When PC trace mode is not selected, this signal is a JTAG data input signal. It is used to input serial data to JTAG data/instruction registers. When PC trace mode is selected, this signal is an interrupt input signal used to cancel PC trace mode for the debug unit. |
| TDO / TPC[0] | O | JTAG data output / PC Trace output When PC trace mode is not selected, this signal is a JTAG data output signal. Data is output by means of serial scan. When PC trace mode is selected, this signal outputs the value of the noncontiguous program counter in sync with the debug clock (DCLK). |
| TPC[3:1] | O | PC Trace Output TPC[3:1] output the value of the noncontiguous program counter in sync with DCLK. |
| TMS | I PU | JTAG command TMS mainly controls state transition in the TAP controller state machine. |
| TRST* | I | Test Reset Input Asynchronous reset input for the TAP controller and debug support unit. When an EJTAG probe is not connected, this pin must be fixed to low. When connecting an EJTAG probe, prevent floating, for example, by connecting a pull-up resistor. When this signal is de-asserted, G-Bus timeout detection is disabled. |
| DCLK | O | Debug Clock A clock output for a real-time debug system. The timing of a serial monitor bus and PC trace interface signal are all defined by this debug clock DCLK. 3 divide the operation clock of the TX4937 at the time of a serial monitor bus operation. |

| Signal Name | Type | Function |
|-------------|------|--|
| PCST[8:0] | O | PC Trace Status Output PC trace status information and the mode of the serial monitor bus. |

| Clock Signals | | |
|---------------|---|--|
| MASTERCLK | I | Master Clock Input Input pin for the TX4937 operating clock. A crystal resonator cannot be connected to this pin because the pin does not contain an oscillator. |
| HALTDOZE | O | Half/Doze state output This signal is asserted (High output) when the TX4937 enters Halt or Doze mode. |
| BYPASSPLL* | I | PLL Reset This pin must be fixed to High. |
| CGRESET* | I | CG Reset CGRESET* initializes the CG |

| Reset signals | | |
|---------------|---|-------------------------------|
| RESET* | I | Reset Reset signal. |

| Test signals | | |
|--------------|---------|--|
| TEST[4:0]* | I PU | Test mode Enable Test pins. These pins must be left open or fixed to High. |

| Signal Name | Type | Function |
|---|------|---|
| Power pins and Total pin count | | |
| PLL1Vdd_A, PLL2Vdd_A, PLL1Vss_A, PLL2Vss_A | - | Power and Ground pins to internal PLL circuit. PLL1Vcc_A and PLL2Vcc_A = 1.5V, PLL1_Vss_A and PLL2_Vss_A = GND |
| VddIN | - | Internal Power Pins Power pins at 1.5V |
| VddIO | - | I/O Power Pins Power pins at 3.3V |
| Vss | - | Ground Digital ground pins. Vss = 0 V. |

4. Pin Multiplexing

A total of 13 pins of the TX4937 have multiplexed functions. Table 4.1 shows the multiplexed pins. The function of a given pin is selected in various ways, depending on the pin(s) involved. Table 4.2 and Table 4.3 show the setting by booting of TX4937.

Table 4.1 Pin Multiplexing

| Signal name | Multiplexed Function |
|-------------|-----------------------------------|
| CB[7:0] | CB[7:0] / PIO[15:8] |
| DMAREQ[2] | DMAREQ[2] / ACRESET* |
| DMAACK[2] | DMAACK[2] / SYNC |
| PIO[4:2] | PIO[4:2] / SDOUT, SDIN[0], BITCLK |

Table 4.2 Setting by ADDR[18]

| Signal name | ADDR[18]=0 (Non ECC) | | ADDR[18]=1 (ECC) | |
|-------------|----------------------|-----------|------------------|---------|
| CB[7:0] | I/O | PIO[15:8] | I/O | CB[7:0] |

Table 4.3 Setting by ADDR[9]

| Signal name | ADDR[9]=1 (ACLC) | | ADDR[9]=0 (Non ACLC) | |
|-------------|------------------|----------|----------------------|-----------|
| DMAREQ[2] | O | ACRESET* | I | DMAREQ[2] |
| DMAACK[2] | O | SYNC | O | DMAACK[2] |
| PIO[4] | O | SDOUT | I/O | PIO[4] |
| PIO[3] | I | SDIN[0] | I/O | PIO[3] |
| PIO[2] | I | BITCLK | I/O | PIO[2] |

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATING (*1)

| PARAMETER | SYMBOL | RATING | UNIT |
|-------------------------------|------------------------|----------------------------------|------|
| Supply voltage (for I/O) | V _{ddIO} Max | -0.3 to 3.9 | V |
| Supply voltage (for internal) | V _{CCInt} Max | -0.3 to 3.0 | V |
| Input voltage (*2) | V _{IN} | -0.3 to V _{ddIO} + 0.3V | V |
| Storage Temperature | T _{STG} | -40 to +125 | °C |
| Power | P _D | T.B.D. | W |

Note) (*1) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended condition. If these conditions are exceeded, reliability of LSI may be adversely affected.

(*2) The maximum rated V_{ddIO}Max voltage must not be exceeded even at V_{ddIO} + 0.3 volts.

5.2 RECOMMENDED OPERATING CONDITIONS (*3)

| PARAMETER | SYMBOL | CONDITION | MIN. | MAX. | UNIT |
|----------------------------|----------------|-------------------|------|------|------|
| Supply Voltage | I/O | V _{ddIO} | 3.1 | 3.5 | V |
| | Internal | V _{ddIN} | 1.4 | 1.6 | V |
| Operating Case Temperature | T _c | | 0 | 70 | °C |

(*3) Functional operation should be restricted to the recommended operating conditions. Those are the limits under which proper device operation is guaranteed. Therefore, the end product must be designed within the recommended voltage and temperature ranges indicated.

5.3 DC CHARACTERISTICS

DC Characteristics except for PCI interface

(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, Vss = 0V)

| PARAMETER | SYM | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|--------------------|---|------|--------|-----------|------|
| Low-level input voltage | V _{IL1} | (*1) | -0.3 | | 0.8 | V |
| High-level input voltage | V _{IH1} | (*1) | 2.0 | | VddIO+0.3 | V |
| Low-level output current | I _{OL1} | (*2) V _{OL} = 0.4V | 8 | | - | mA |
| | I _{OL2} | (*3) V _{OL} = 0.4V | 4 | | - | mA |
| Low-level output current | I _{OL3} | (*4) V _{OL} = 0.4V | 16 | | - | mA |
| | I _{OL4} | (*5) V _{OL} = 0.4V | 8 | | - | mA |
| High-level output current | I _{OH1} | (*2) V _{OH} = 2.4V | - | | -8 | mA |
| | I _{OH2} | (*3) V _{OH} = 2.4V | - | | -4 | mA |
| High-level output current | I _{OH3} | (*4) V _{OH} = 2.4V | - | | -16 | mA |
| | I _{OH4} | (*5) V _{OH} = 2.4V | - | | -8 | mA |
| Low-level input leakage current | I _{IL1} | (*6) V _{IN} = V _{SS} | -10 | | 10 | μA |
| | I _{IL2} | (*7) V _{IN} = V _{SS} | -200 | | -10 | μA |
| High-level input leakage current | I _{IH1} | (*8) V _{IN} = V _{CCIO} | -10 | | 10 | μA |
| | I _{IH2} | (*9) V _{IN} = V _{CCIO} | 10 | | 200 | μA |
| Hi-z output leakage current | I _{OZ} | (*10) | -10 | | 10 | μA |
| Operating current (for internal) | I _{CCInt} | VddIO = 3.3V, VddIN = 1.6V, PClock = 300MHz | | T.B.D. | T.B.D. | mA |
| Operating current (for I/O) | I _{CCIO} | VddIO = 3.5V, VddIN = 1.5V, MASTERCLK=133MHz Load=25pF | | T.B.D. | T.B.D. | mA |

(*1) All input and input-mode bidirectional pins except PCI interface signals

(*2) ACE*, ACK*, BUSSPRT*, BWE[3:0]*, CE[7:0]*, DMAACK[3:0], DMADONE*, EEPROM_CS, EEPROM_DO, EEPROM_SK, HALTDOZE, PIO[7:0], RTS[1:0], SWE*, SYSCLK, TIMER[1:0], TXD[1:0]

(*3) DCLK, PCST[8:0], TDO, TPC[3:1]

(*4) Applies to ADDR[19:0], CAS*, CB[7:0], CE, DATA[63:0], DQM[7:0], OE*, RAS*, SDCLK[3:0], SDCLKIN, SDCS[3:0]* and WE when an output buffer drive strength of 16 mA is used.

(*5) Drive 8mA: ADDR[19:0], CAS*, CB[7:0], CE, DATA[63:0], DQM[7:0], OE*, RAS*, SDCLK[3:0], SDCLKIN, SDCS[3:0]*, WE

(*6) EEPROM_DI, CGRESET*, RESET*, TRST*, BYPASSPLL*, MASTERCLK, DMADONE*, PIO[7:0], SDCLKIN

(*7) CTS[1:0]*, DMAREQ[3:0], RXD[1:0], SCLK, TCLK, INT[5:0], TCK, TDI, TEST[4:0]*, TMS, ACK*, CB[7:0], DATA[63:0], ADDR[19:0], NMI*, **PIO[7:0]**

(*8) (*6), (*7) Signals except for TRST*

(*9) TRST*

(*10) TXD[1:0]

DC Characteristics except for PCI interface

(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, Vss = 0V)

| PARAMETER | SYM | CONDITIONS | MIN. | MAX. | UNIT |
|-----------------------------|--------------------|--------------------------------|-------------|-------------|------|
| Low-level input voltage | V _{ILPCI} | (*1) | -0.5 | 0.9 | V |
| High-level input voltage | V _{IHPCI} | (*1) | 1.8 | VddIO+0.3 | V |
| High-level output voltage | V _{OHPCI} | (*2) I _{OUT} = -500uA | VddIO × 0.9 | - | V |
| Low-level output voltage | V _{OLPCI} | (*2) I _{OUT} = 1500uA | - | VddIO × 0.1 | V |
| Input leakage current | I _{IHPCI} | 0 < V _{IN} < VddIO | -10 | 10 | μA |
| | I _{ILPCI} | | -10 | 10 | μA |
| Hi-z output leakage current | I _{OZPCI} | (*3) | -10 | 10 | μA |

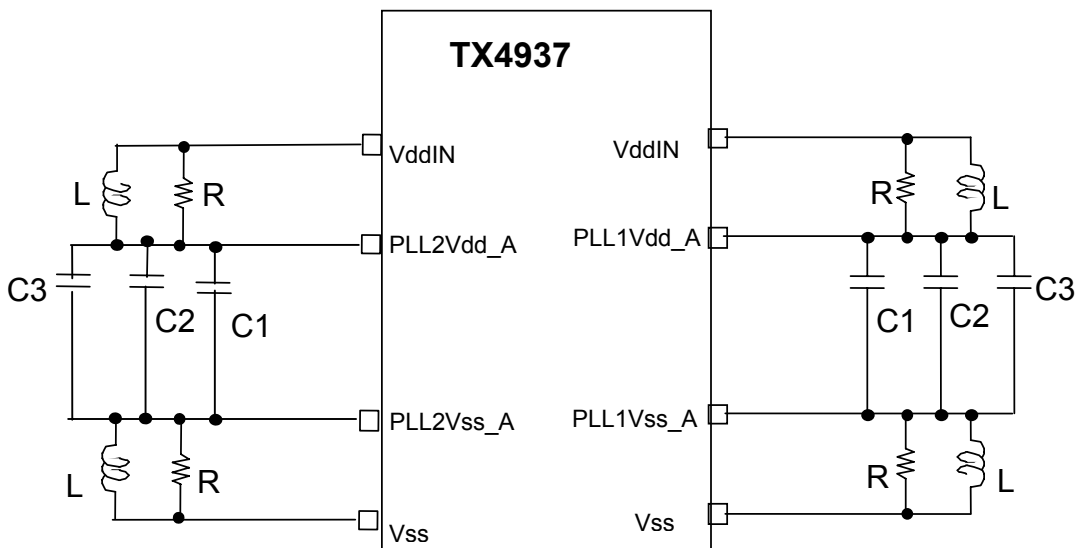
(*1) ID_SEL, PCICLKIN, C_BE[3:0], DEVSEL*, FRAME*, GNT[3:0]*, IRDY*, LOCK*, M66EN, PAR, PCIAD[31:0], PERR*, REQ[3:0], SERR*, STOP*, TRDY*

(*2) ID_SEL, PCICLKIN

(*3) PCICLK[5:0], PME*

5.4 Power circuit for PLL

Recommended circuit for PLL



Note) C1, CS, C3, R and L should be placed as closed to the processor as possible.

| PARAMETER | SYMBOL | AS a reference Value | UNIT |
|-----------------------------|--------|----------------------|------|
| Resistor | R | 5.6 | ohm |
| Inductance | L | 2.2 | μH |
| Capacitor | C1 | 1 | nF |
| | C2 | 82 | nF |
| | C3 | 10 | μF |
| VddIN, PLL1Vdd_A, PLL2Vdd_A | | 1.5V ± 0.1V | V |

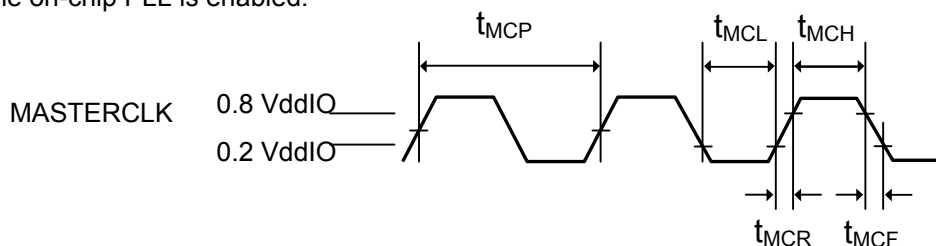
5.5 AC CHARACTERISTICS

MASTERCLK AC Characteristics

(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, VSS = 0V)

| PARAMETER | SYM | CONDITION | MIN. | MAX. | UNIT |
|------------------------------|-----------|-----------|------|------|------|
| MASTERCLK Period | t_{MCP} | | 1.5 | 30 | ns |
| MASTERCLK Frequency (*) | f_{MCK} | | 12.5 | 133 | MHz |
| MASTERCLK High | t_{MCH} | | 3 | | ns |
| MASTERCLK Low | t_{MCL} | | 3 | | ns |
| Internal Operating Frequency | f_{CPU} | | 50 | 300 | MHz |
| MASTERCLK Rise Time | t_{MCR} | | | 2 | ns |
| MASTERCLK Fall Time | t_{MCF} | | | 2 | ns |

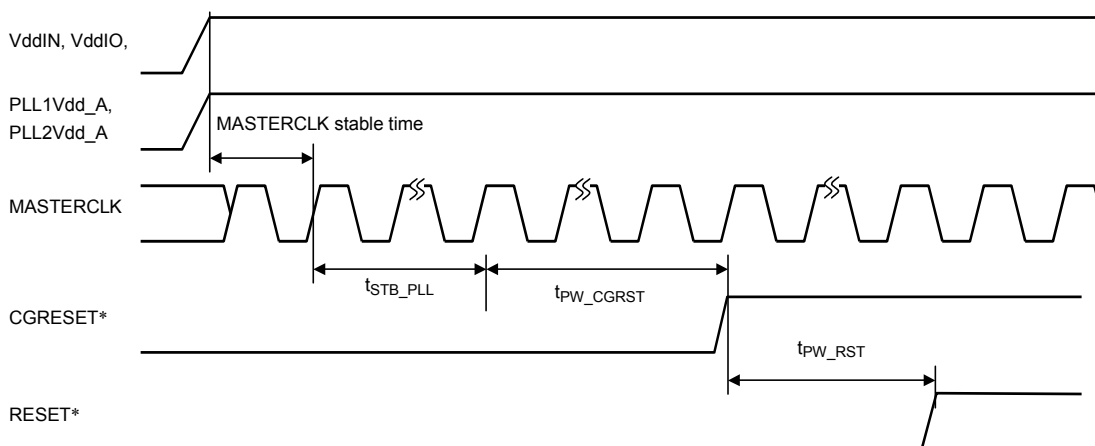
(*1) Proper circuit operation of the TX4937 is guaranteed only when power supply to it is stable and the on-chip PLL is enabled.



Power On AC Characteristics

(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, VSS = 0V)

| PARAMETER | SYM | CONDITION | MIN. | MAX. | UNIT |
|---------------------|-----------------|-----------|------|------|------|
| PLL stable time | t_{STB_PLL} | | 10 | | ms |
| CGRESET* width time | t_{PW_CGRST} | | 1 | | ms |
| RESET* width time | t_{MCF} | | 1 | - | ms |

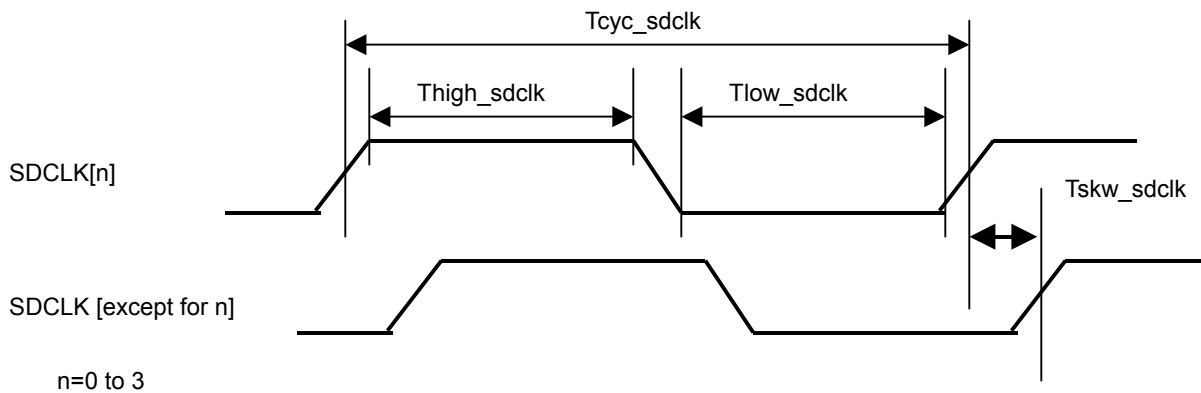


SDRAM Interface AC Characteristics

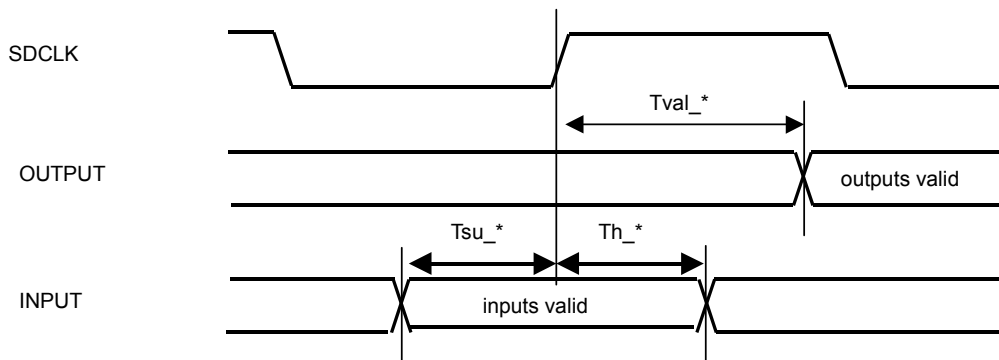
(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, VSS = 0V)

| Signal Name | I/O | Load (pF) | Buffer Type | SYM | Descriptions | MIN (ns) | MAX (ns) |
|-------------|----------------------------------|-----------|-------------|-------------|---|----------|----------|
| SDCLK[3:0] | O | 50 | 16mA | Tcyc_sdclk | Clock Cycle Time | 10 | - |
| | | | | Thigh_sdclk | Clock High Time | 3 | - |
| | | | | Tlow_sdclk | Clock Low Time | 3 | - |
| | | | | Tskw_sdclk | Clock Skew | -1.0 | 1.0 |
| SDCLKIN | I | - | - | Tbp | Clock Input Timing (Non bypass mode) | 0 | 4.0 |
| ADDR[19:5] | O | 150 | 16mA | Tval_addr1 | Address Output Delay (*1) | 1.5 | 6.5 |
| SDCS[3:0]* | O | 100 | 16mA | Tval_sdc | Output Delay for Chip Select | 1.5 | 6.5 |
| RAS* | O | 150 | 16mA | Tval_ra | Output Delay for RAS (*1) | 1.5 | 6.5 |
| CAS* | O | 150 | 16mA | Tval_ca | Output Delay for CAS (2 Cycle Bus Operation) | 1.5 | 6.5 |
| WE* | O | 150 | 16mA | Tval_we | Output Delay for Write Enable (2 Cycle Bus Operation) | 1.5 | 6.5 |
| CKE | O | 150 | 16mA | Tval_cke | Output Delay for Clock Enable | 1.5 | 6.5 |
| DQM[7:0] | O | 50 | 16mA | Tval_dqm | Output Delay for Data Mask (*1) | 1.5 | 6.5 |
| DATA[63:0] | I/O | 50 | 16mA | Tval_data1 | Output Delay for Data (High <->low) (*1) | 1.5 | 6.5 |
| | | | | Tval_data1v | Output Delay for Data (Hi-Z -> valid) | 1.5 | 6.5 |
| | | | | Tval_data1z | Output Delay for Data (valid->Hi-Z) | 1.5 | 6.5 |
| | | | | Tsu_data1b | Data Setup Time (Bypass mode) | 3.5 | - |
| | | | | Th_data1b | Data Hold Time (Bypass mode) | 0.5 | - |
| | | | | Tsu_data1nb | Data Setup Time (Non bypass mode) | 1.5 | - |
| Th_data1nb | Data Hold Time (Non bypass mode) | 1.0 | - | | | | |

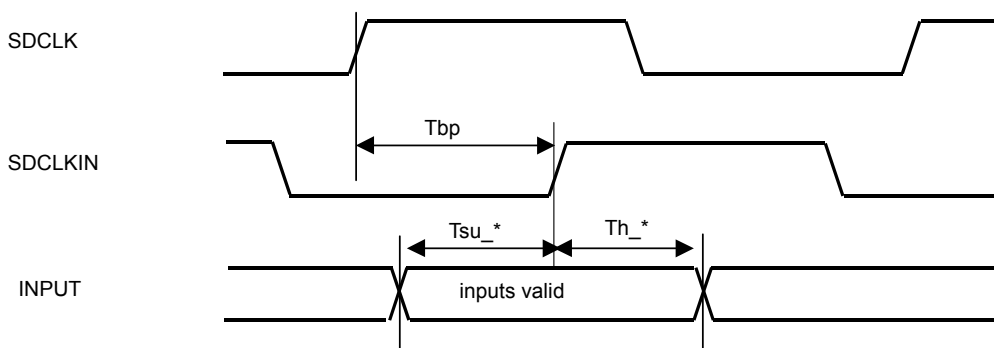
(*1) An SDRAM bus transaction can complete in no more than two clock cycles through programming the SDRAMC and Configuration registers.



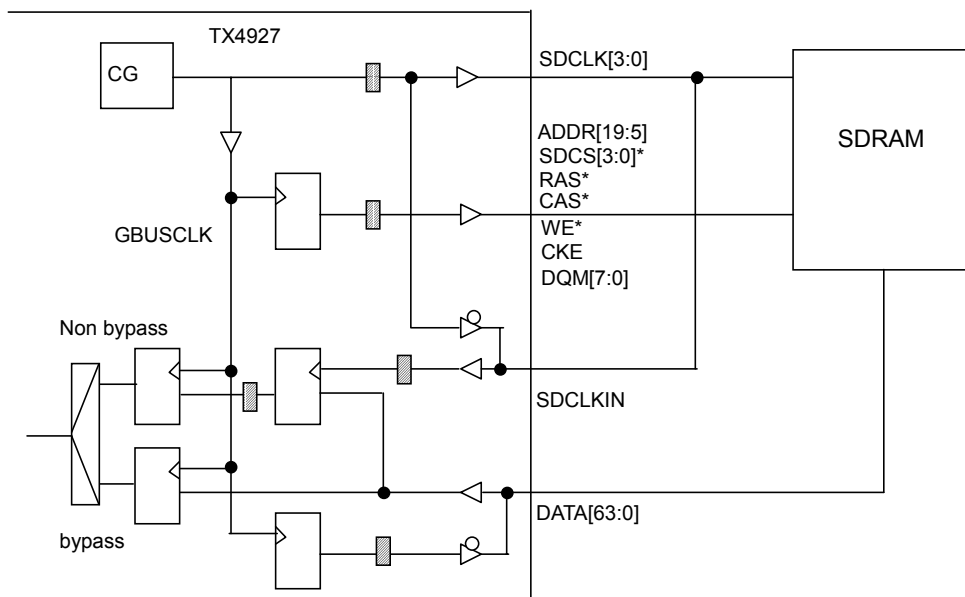
Clock and Skew



Output Signals and when bypass mode input Signals (SDCLK basis)



When non bypass mode input signals (SDCLK basis)

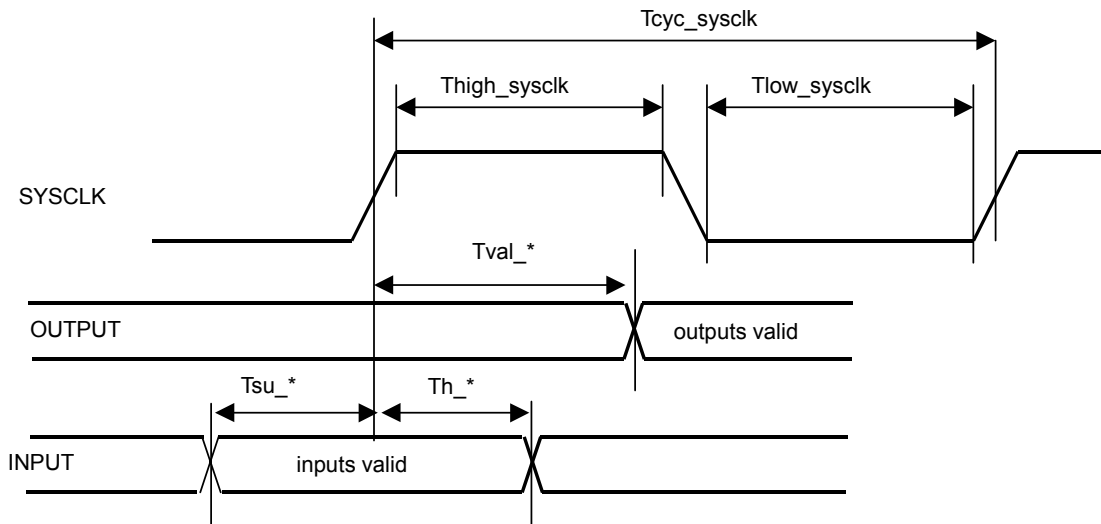


SDRAM Controller System Structure

External Bus Interface AC Characteristics

(Tc = 0 ~ 70°C, VddIO = 3.3V ± 0.2V, VddIN = 1.5V ± 0.1V, VSS = 0V)

| Signal Name | I/O | Load (pF) | Buffer Type | SYM | Descriptions | MIN (ns) | MAX (ns) |
|-------------|-----|-----------|-------------|--------------|--|----------|----------|
| SYSCLK | O | 50 | 8mA(fix) | Tcyc_sysclk | Clock Cycle Time | 10 | - |
| | | | | Thigh_sysclk | Clock High Time | 4 | - |
| | | | | Tlow_sysclk | Clock Low Time | 4 | - |
| ADDR[19:5] | O | 150 | 16mA | Tval_addr2 | Output Delay for Address | 1.5 | 6.5 |
| CE[7:0]* | O | 50 | 8mA(fix) | Tval_ce | Output Delay for Chip Enable | 1.5 | 8.5 |
| OE* | O | 50 | 8mA(fix) | Tval_oe | Output Delay for Output Enable | 1.5 | 8.5 |
| SWE* | O | 50 | 8mA(fix) | Tval_swe | Output Delay for Write Enable | 1.5 | 8.5 |
| BWE*[3:0] | O | 50 | 8mA(fix) | Tval_bwe | Output Delay for Byte Enable | 1.5 | 8.5 |
| ACE* | O | 50 | 8mA(fix) | Tval_ace | Output Delay for Address Clock Enable | 1.5 | 8.5 |
| BUSSPRT* | O | 50 | 8mA(fix) | Tval_busr | Output Delay for Bus Separate | 1.5 | 8.5 |
| DATA[31:0] | I/O | 50 | 16mA | Tval_data2 | Output Delay for Data (High <-> Low) | 1.5 | 6.5 |
| | | | | Tval_data2v | Output Delay for Data (Hi-Z -> valid) | 1.5 | 8.5 |
| | | | | Tval_data2z | Output Delay for Data (valid -> Hi-Z) | 1.5 | 8.5 |
| | | | | Tsu_data2 | Data Setup Time | 4.0 | - |
| | | | | Th_data2 | Data Hold Time | 0.5 | - |
| ACK* | I/O | 50 | 8mA(fix) | Tval_ack | Output Delay for ACK* (High <-> Low) | 1.5 | 8.5 |
| | | | | Tval_ackv | Output Delay for ACK* (Hi-Z -> valid) | 1.5 | 6.5 |
| | | | | Tval_ackz | Output Delay for ACK* (valid -> Hi-Z) | 1.5 | 8.5 |
| | | | | Tsu_ack | ACK* Setup Time | 4.0 | - |
| | | | | Th_ack | ACK* Hold Time | 0.5 | - |

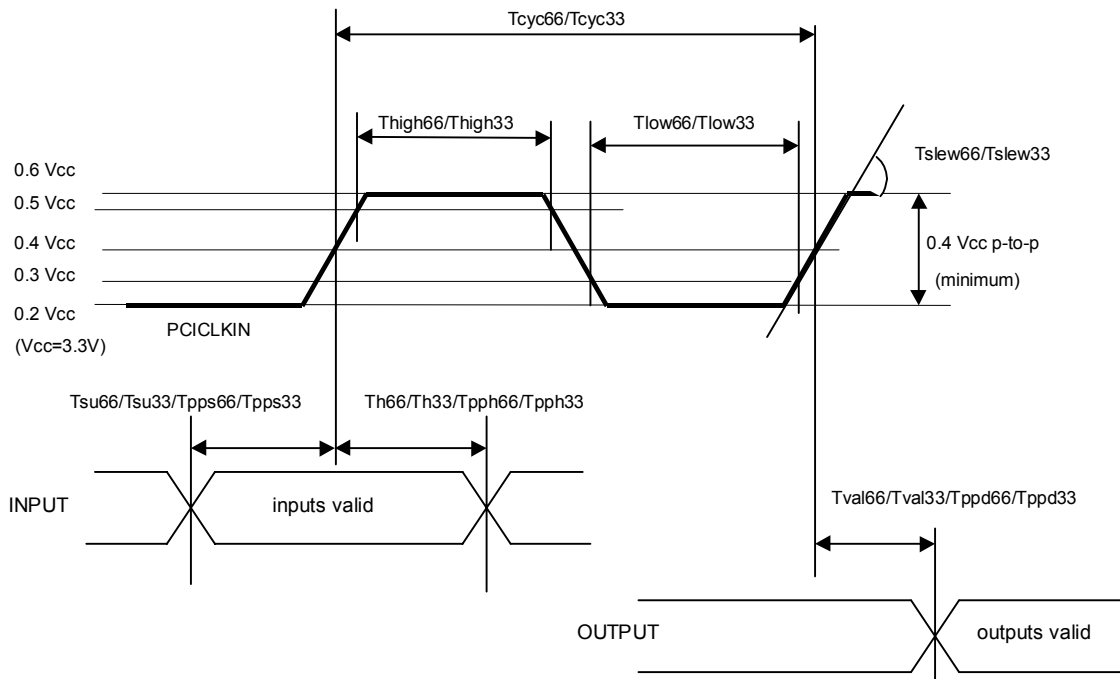


External Bus Interface

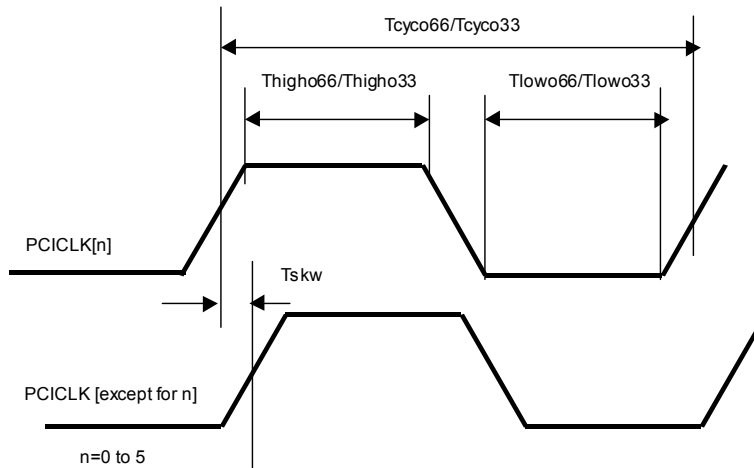
PCI Interface AC Characteristics

| Signal Name | I/O | PCI-bus Spec. | Load (pF) | SYM | Descriptions | MIN (ns) | MAX (ns) | | | | |
|---|-----|---------------|-----------|---------|---|--|--|----|---|--|--|
| PCICLKIN | I | 66MHz | - | Tcyc66 | Input Clock Cycle Time | 15 | 30 | | | | |
| | | | | Thigh66 | Input Clock High Time | 6 | - | | | | |
| | | | | Tlow66 | Input Clock Low Time | 6 | - | | | | |
| | | | | Tslew66 | Input Clock Through rate [V/ns] | 1.5 | 4 | | | | |
| | | 33MHz | - | Tcyc33 | Input Clock Cycle Time | 30 | 40 | | | | |
| | | | | Thigh33 | Input Clock High Time | 11 | - | | | | |
| | | | | Tlow33 | Input Clock Low Time | 11 | - | | | | |
| PCICLK[5:0] | O | 66MHz | 50 | Tcyc66 | Output Clock Cycle Time | 15 | 30 | | | | |
| | | | | Thigh66 | Output Clock High Time | 5 | - | | | | |
| | | | | Tlow66 | Output Clock Low Time | 6 | - | | | | |
| | | | | Tslew66 | Output Clock Through rate [V/ns] | 1 | 4 | | | | |
| | | 33MHz | 70 | Tcyc33 | Output Clock Cycle Time | 30 | 40 | | | | |
| | | | | Thigh33 | Output Clock High Time | 11 | - | | | | |
| | | | | Tlow33 | Output Clock Low Time | 11 | - | | | | |
| | | | 80 | Tskw | Output Clock Slew (point to point connection) | 0 | TBD | | | | |
| PCIAD[31:0] C_BE[3:0] PAR FRAME* IRDY* TRDY* STOP* DEVSEL* PERR* SERR* LOCK* M66EN PME* | I/O | 66MHz | 30 | Tval66 | Output Delay (bus connection) | 2 | 8 | | | | |
| | | | | - | Tsu66 | Setup Time (bus connection) | 4 | - | | | |
| | | | | | Th66 | Hold Time (bus connection) | 0 | - | | | |
| | I/O | 33MHz | 70 | - | Tval33 | Output Delay (bus connection) | 2 | 11 | | | |
| | | | | | Tsu33 | Setup Time (bus connection) | 7 | - | | | |
| | | | | | Th33 | Hold Time (bus connection) | 0 | - | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| | | | | | | | | | | | |
| ID_SEL REQ[3:0]* GNT[3:0]* | I | 66MHz | 30 | Tppd66 | Output Delay (point to point connection) | 2 | 8 | | | | |
| | | | | - | Tpps66 | Setup Time (point to point connection) | 5 | - | | | |
| | | | | | Tpph66 | Hold Time (point to point connection) | 0 | - | | | |
| | I/O | 33MHz | 70 | - | Tppd33 | Output Delay (point to point connection) | 2 | 12 | | | |
| | | | | | - | Tpps33 | Setup Time (point to point connection) | 10 | - | | |
| | | | | | | Tpph33 | Hold Time (point to point connection) | 0 | - | | |

TENTATIVE

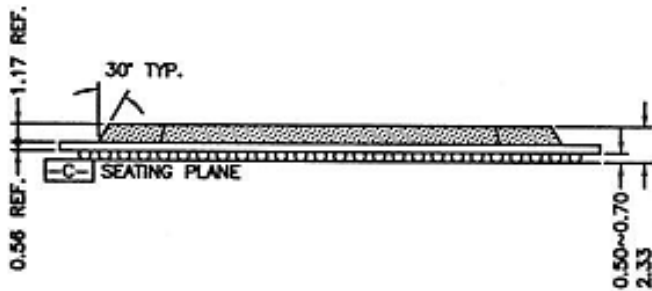
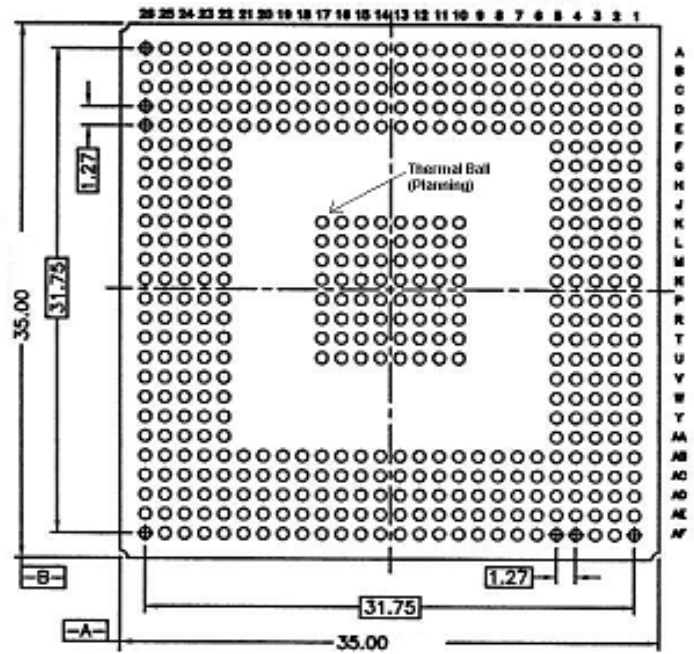
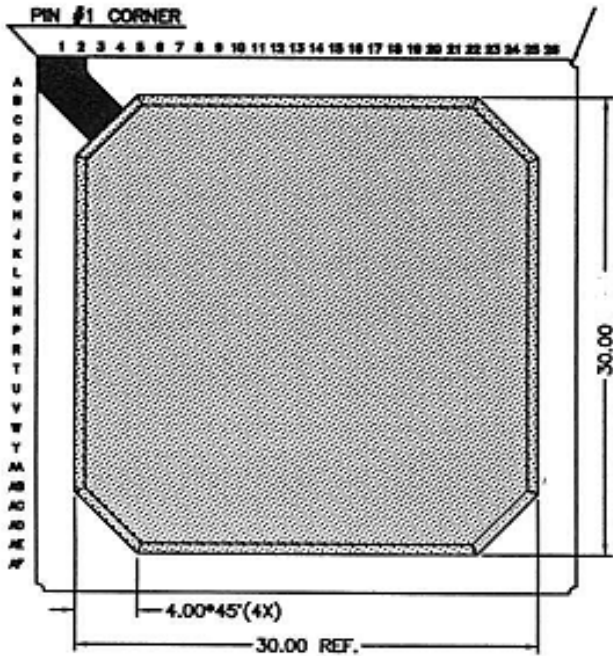


PCI Interface (3.3V)



PCI Clock Skew

6. Package



TENTATIVE

7. Differences Between the TMPR4927A and the TMPR4937

7.1 Product Name

TX4927A : TMPR4927ATB-200

TX4937 : TMPR4937XB-300

7.2 Package Type

TX4927A : TBGA420-pin

TX4937 : PBGA484-pin (64-pin are the thermal balls for radiation : GND)

Note: Pin compatible with TX4927 except the thermal balls

7.3 PIO[7:0] I/O buffer type

TX4927A : I/O buffer without the pull-up resistor

TX4937 : I/O buffer with the pull-up resistor

7.4 TX Core

TX4927A : TX49/H2 Core (0.18um process), Maximum operating frequency 200MHz, (266MHz)

TX4937 : TX49/H3 Core (0.13um process), Maximum operating frequency 300MHz, (333MHz)

7.5 SDRAM Controller

TX4927A : Maximum bus frequency 100MHz, Memory Size to 256Mbit

TX4937 : Maximum bus frequency 133MHz, Memory Size to 512Mbit

7.6 External Device Controller

TX4927A : Maximum bus frequency 100MHz

TX4937 : Maximum bus frequency 133MHz, Sync Flash Memory

7.7 DMA Controller

TX4927A : 4 channels

TX4937 : 8 channels (4 channels for ACLC)

7.8 Boot Configuration

ADDR[16] : TX4927A : Reserved (pull down prohibition)

TX4937 : The change of the clock frequency for PCIC1

ADDR[11:10] : TX4927A : A setup of the frequency ratio of PCICLK to CPUCLK

LL : 1/2.5, LH : 1/3, HL : 1/5, HH : 1/6

TX4937 : A setup of the frequency ratio of PCICLK to CPUCLK

CCFG[10]=0(Initial state)

LL : 1/8, LH : 1/9, HL : 1/10, HH : 1/11

CCFG[10]=1(At the time of a register setup)

LL : 1/4, LH : 1/4.5, HL : 1/5, HH : 1/5.5

ADDR[8:6] : TX4927A (A setup of boot)

HHH : The device connected to the external device controller ch0 (clock ratio 1/1)

HHL : The device connected to the external device controller ch0 (clock ratio 1/2)

HLH : The device connected to the external device controller ch0 (clock ratio 1/3)

HLL : The device connected to the external device controller ch0 (clock ratio 1/4)

LHH : PCI boot, LHL : reserved, LLH : reserved, LLL : reserved

TX4937 (A setup of boot)

HHH : The device connected to the external device controller ch0 (clock ratio 1/1)

HHL : The device connected to the external device controller ch0 (clock ratio 1/2)

HLH : The device connected to the external device controller ch0 (clock ratio 1/3)

HLL : The device connected to the external device controller ch0 (clock ratio 1/4)

LHH : PCI boot, LHL : reserved, LLH : reserved, LLL : reserved

ADDR[5] : TX4927A : Reserved (pull down prohibition)

TX4937 : Initial setting of the drive capability of multi drive I/O

ADDR[19:0], CKE, RAS*, CAS*, WE*, SDCS[3:0], SDCLK[3:0], SDCLKIN

L = 8mA, H = 16mA

ADDR[4] : TX4927A : Reserved (pull down prohibition)

TX4937 : Initial setting of the drive capability of multi drive I/O

DATA[63:0],CB[7:0].DQM[7:0]

L = 8mA, H = 16mA

ADDR[3] : TX4927A : Reserved (pull down prohibition)

TX4937 : A setup of the clock ratio of CPUCLK/GBUSCLK

(Five kinds of setup is changed possible by 3 bits of ADDR [3] and [1:0].)

HHH : 1:2, HHL : 1:2.5, HLH : 1:3, HLL : 1:4, LHH : 1:4.5

LHL : reserved, LLH : reserved, LLL : reserved

Note: A setup of the clock ratio same in the state of ADDR[3] =H as TX4927A.

8. HISTORY

7/Jan/02 Modified from TX4927 Datasheet

14/Apr/02 Modified from TX4927 Datasheet

16/Apr/02 PU notation addition of Signal PIO [7:0], a Thermal ball information addition, a difference addition with TX4927

EJC-TMPR4927TB-42

16 / Apr / 02

TOSHIBA CORPORATIO