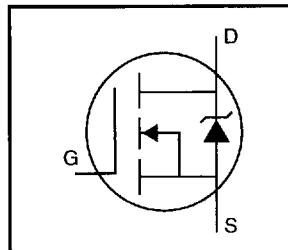


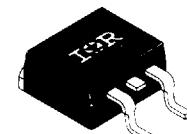
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive

 $V_{DSS} = 50V$ $R_{DS(on)} = 0.012\Omega$ $I_D = 80A$ **Description**

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



SMD-220

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	80 ⑤	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	57 ⑤	
I_{DM}	Pulsed Drain Current ①	320	
$P_D @ T_C = 25^\circ C$	Power Dissipation	150	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.7	
	Linear Derating Factor	1.0	W/ $^\circ C$
	Linear Derating Factor (PCB Mount)**	0.025	
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	700	mJ
I_{AR}	Avalanche Current ①	48	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +175	$^\circ C$
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R_{eJC}	Junction-to-Case	—	—	1.0	$^\circ C/W$
R_{eJA}	Junction-to-Ambient (PCB mount)**	—	—	40	
R_{eJA}	Junction-to-Ambient	—	—	62	

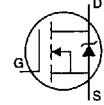
** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	50	—	—	V	$V_{GS}=0V, I_D = 250\mu\text{A}, T_J > -40^\circ\text{C}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.012	Ω	$V_{GS}=10V, I_D=48\text{A}$ ④
		—	—	0.018		$V_{GS}=5.0V, I_D=40\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	21	—	—	S	$V_{DS}=25V, I_D=48\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=50V, V_{GS}=0V$
		—	—	250		$V_{DS}=40V, V_{GS}=0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
Q_g	Total Gate Charge	—	—	110	nC	$I_D=40\text{A}, V_{DS}=44V, V_{GS}=5.0V$
		—	—	190		$I_D=48\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	23		$V_{DS}=44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	51		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.4	—	ns	$V_{DD}=28V$
t_r	Rise Time	—	90	—		$I_D=48\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	140	—		$R_G=5.0\Omega$
t_f	Fall Time	—	140	—		$R_D=0.56\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3300	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	1300	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	410	—		$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	80 ⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ①	—	—	320		
V_{SD}	Diode Forward Voltage	—	—	1.7	V	$T_J=25^\circ\text{C}, I_S=48\text{A}, V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	97	150	ns	$T_J=25^\circ\text{C}, I_F=48\text{A}$
Q_{rr}	Reverse Recovery Charge	—	0.31	0.47	μC	$dI/dt=100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ $I_{SD}\leq 48\text{A}$, $di/dt\leq 180\text{A}/\mu\text{s}$, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq 175^\circ\text{C}$ ② $V_{DD}=25V$, starting $T_J=25^\circ\text{C}$, $L=303\mu\text{H}$, $R_G=25\Omega$, $I_{AS}=48\text{A}$ (See Figure 12)④ Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\%$.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

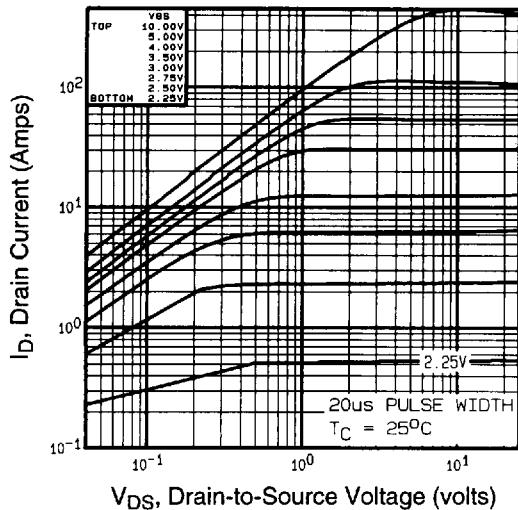


Fig 1. Typical Output Characteristics,
 $T_c = 25^\circ\text{C}$

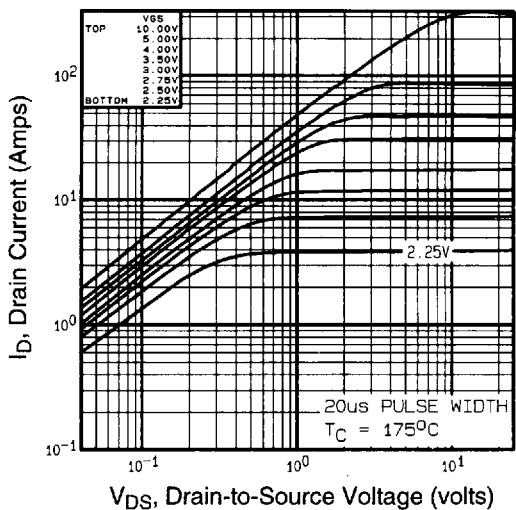


Fig 2. Typical Output Characteristics,
 $T_c = 175^\circ\text{C}$

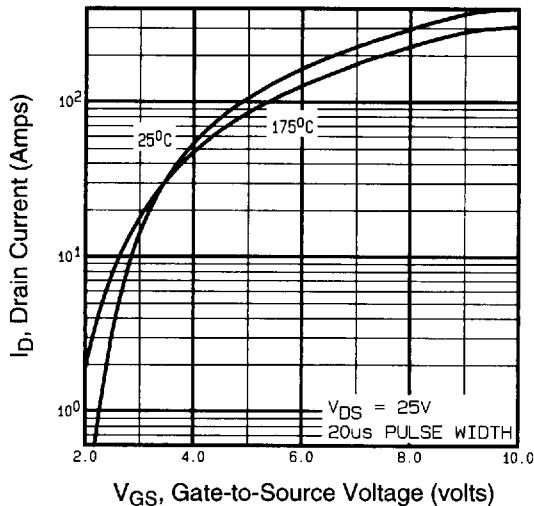


Fig 3. Typical Transfer Characteristics

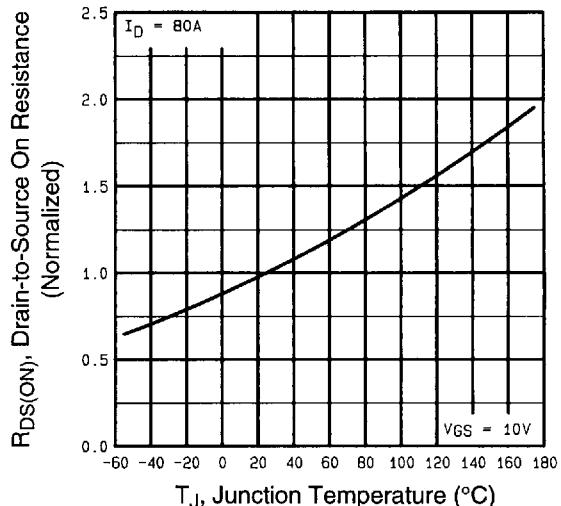


Fig 4. Normalized On-Resistance
Vs. Temperature

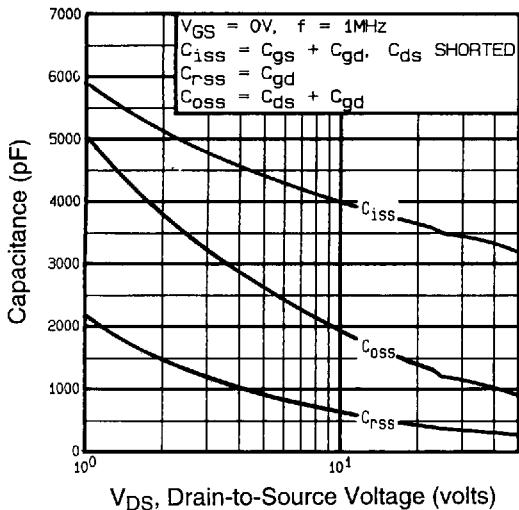


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

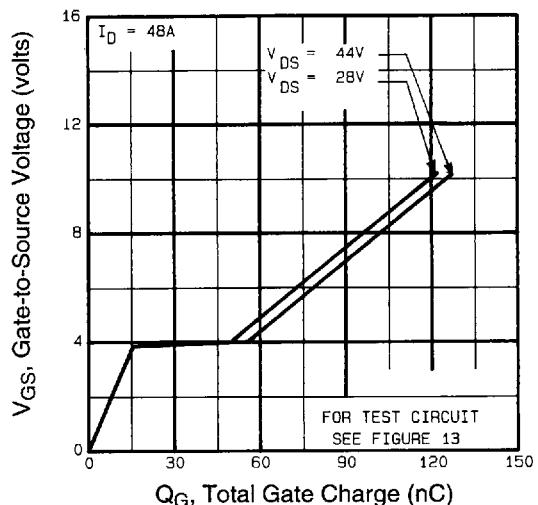


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

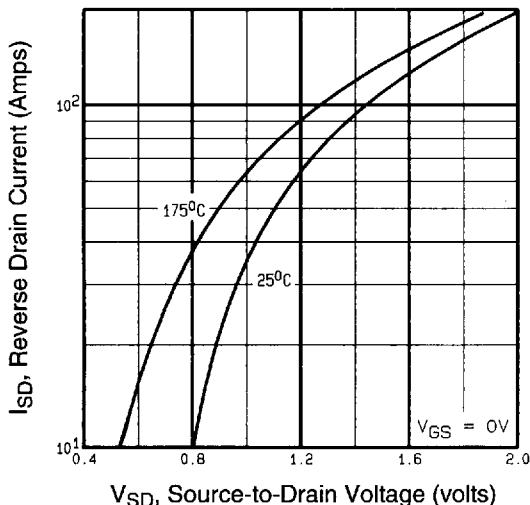


Fig 7. Typical Source-Drain Diode
Forward Voltage

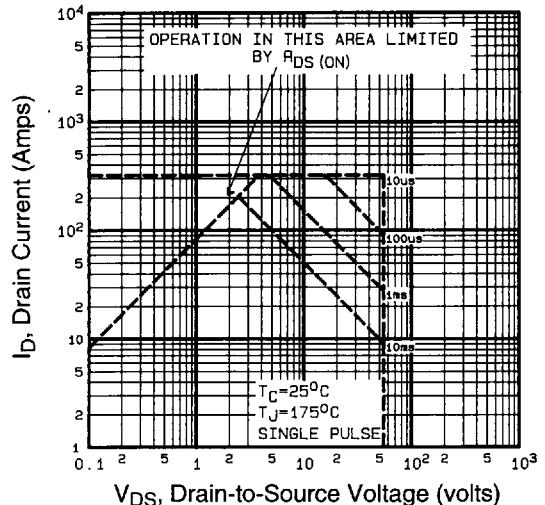


Fig 8. Maximum Safe Operating Area

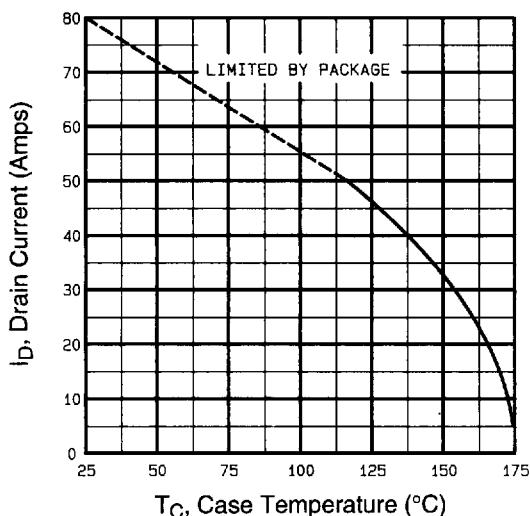


Fig 9. Maximum Drain Current Vs. Case Temperature

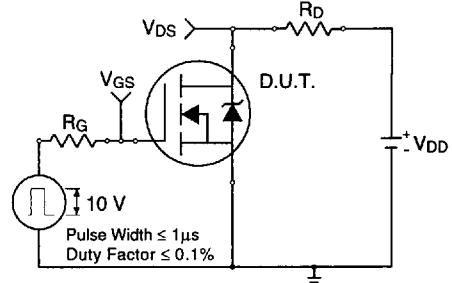


Fig 10a. Switching Time Test Circuit

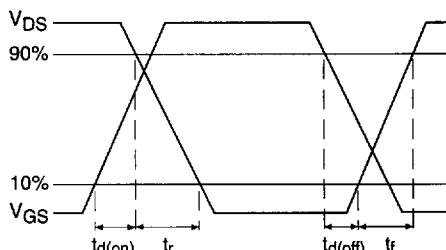


Fig 10b. Switching Time Waveforms

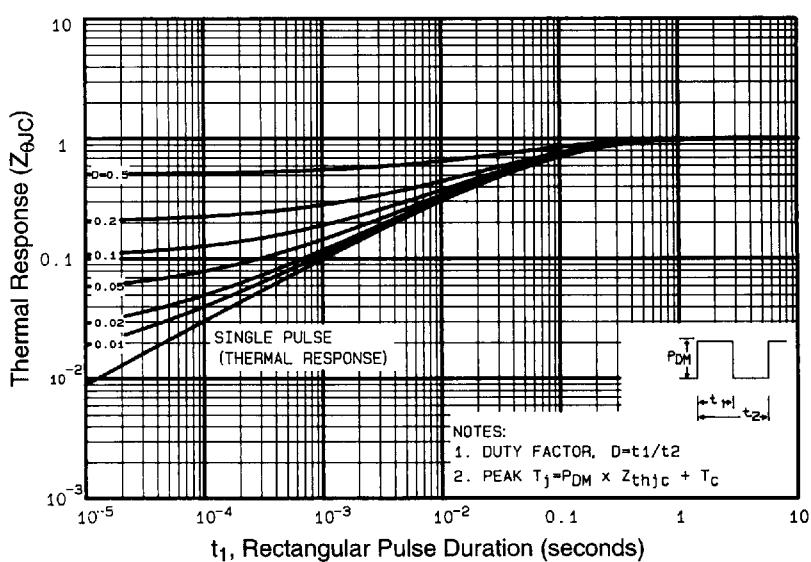


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

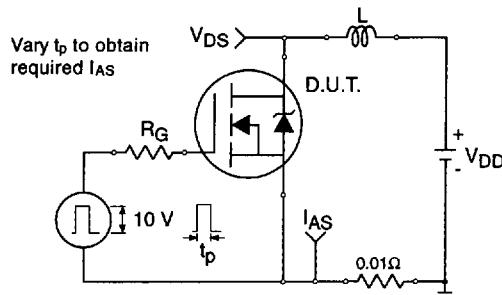


Fig 12a. Unclamped Inductive Test Circuit

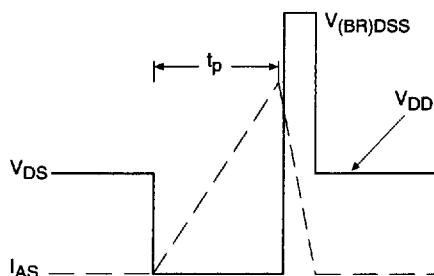


Fig 12b. Unclamped Inductive Waveforms

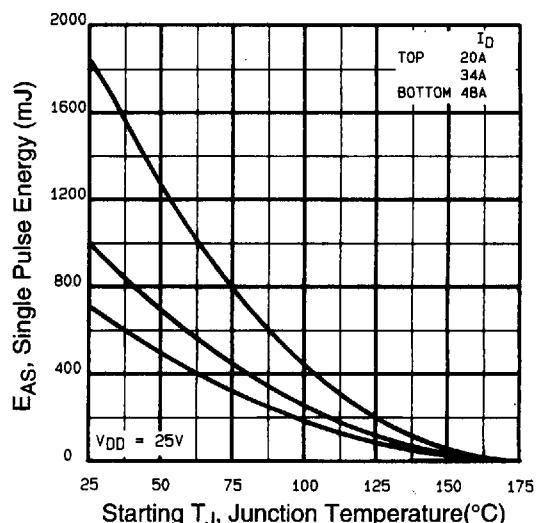


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

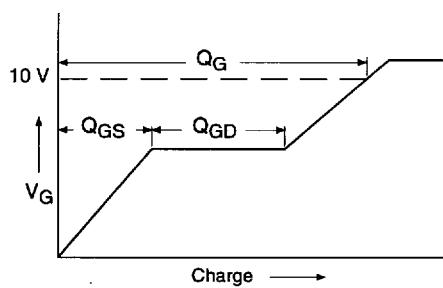


Fig 13a. Basic Gate Charge Waveform

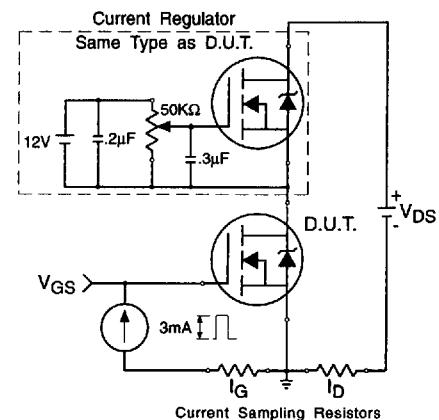
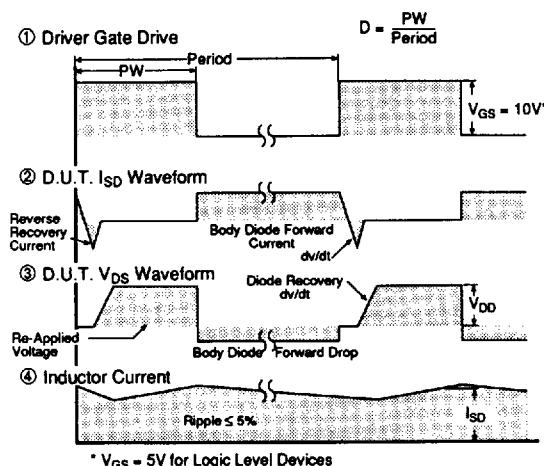
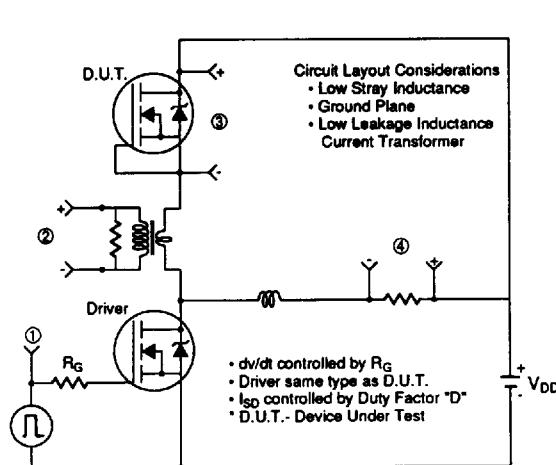


Fig 13b. Gate Charge Test Circuit

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

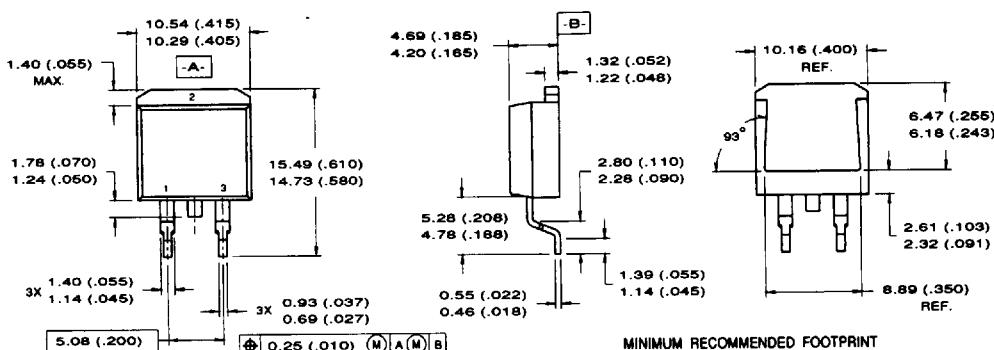


Appendix B

Package Outline

SMD-220 Outline

Dimensions are shown in millimeters (inches)

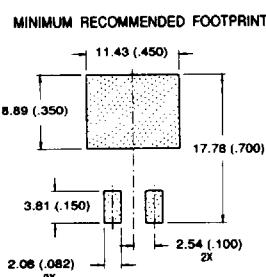


NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982
- 3 CONTROLLING DIMENSION: INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

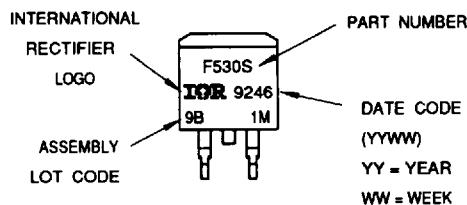


Part Marking Information

SMD-220

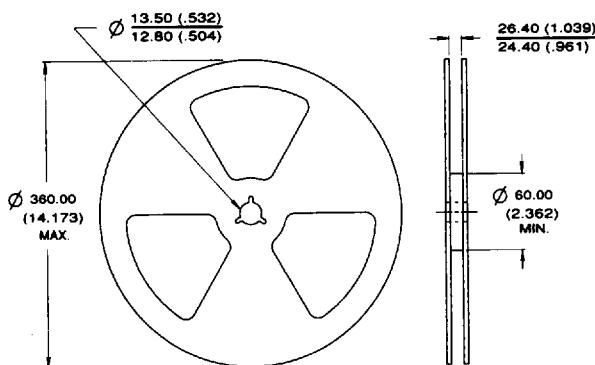
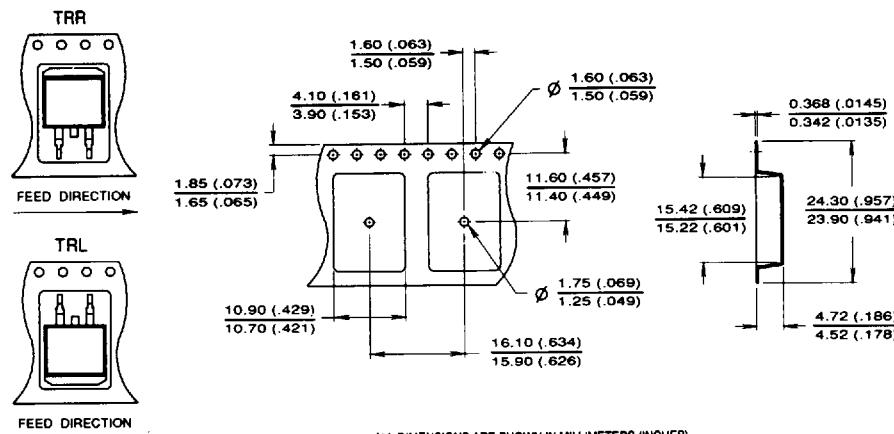
Appendix C

EXAMPLE: THIS IS AN IRF530S WITH
ASSEMBLY LOT CODE 9B1M



Tape & Reel Information

SMD-220 Tape & Reel

Appendix D

SMD-220 Tape & Reel

When ordering, indicate the part number, part orientation, and the quantity. Quantities are in multiples of 800 pieces per reel for both TRL and TRR.



Printed on Signet recycled offset:
made from 50% recycled waste paper, including
10% de-inked, post-consumer waste.



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I²R Rectifier

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