



Integrated Device Technology, Inc.

**FAST CMOS
OCTAL REGISTERED
TRANSCEIVERS**

**IDT29FCT52A/B/C
IDT29FCT53A/B/C**

T-52-31

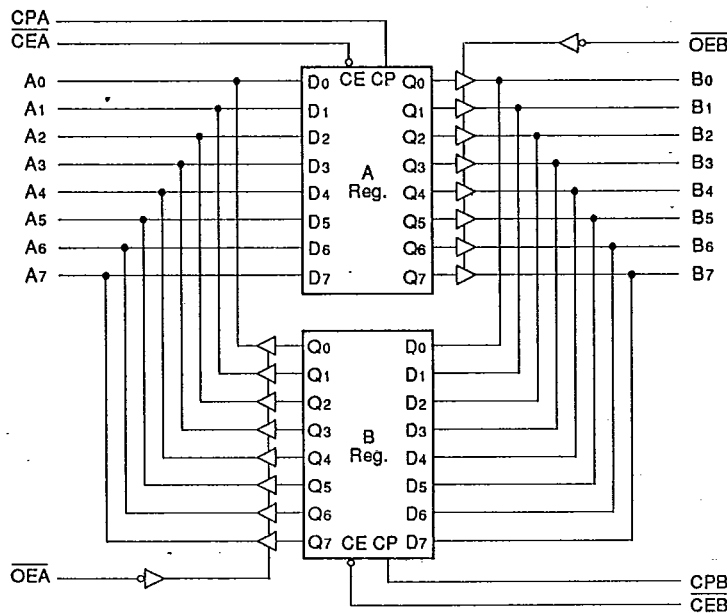
FEATURES:

- Equivalent to AMD's Am2952/53 and National's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed
- IDT29FCT52B/53B 25% faster than FAST™
- IDT29FCT52C/53C 37% faster than FAST™
- IOL = 64mA (commercial) and 48mA (military)
- IIH and IIL only 5µA max.
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC, 28-pin LCC and PLCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52A/B/C and IDT29FCT53A/B/C are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual-metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA. The IDT29FCT52A/B/C is a non-inverting option of the IDT29FCT53A/B/C.

FUNCTIONAL BLOCK DIAGRAM⁽¹⁾



NOTE:
1. IDT29FCT52 function is shown.

2533 drw 01

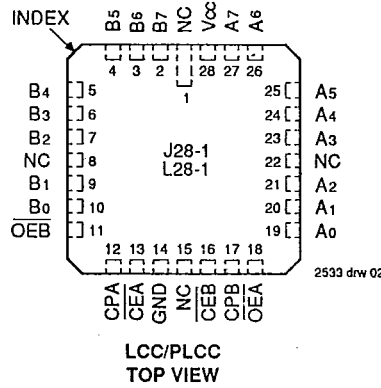
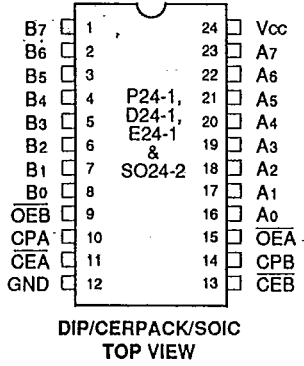
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of National Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1990

PIN CONFIGURATIONS

T-52-31



PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
\overline{CEA}	I	Clock Enable for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When \overline{CEA} is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
\overline{OEB}	I	Output Enable for the A Register. When \overline{OEB} is LOW, the A Register outputs are enabled onto the B0-7 lines. When \overline{OEB} is HIGH, the B0-7 outputs are in the high impedance state.
CPB	I	Clock for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
\overline{CEB}	I	Clock Enable for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When \overline{CEB} is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
\overline{OEA}	I	Output Enable for the B Register. When \overline{OEA} is LOW, the B Register outputs are enabled onto the A0-7 lines. When \overline{OEA} is HIGH, the A0-7 outputs are in the high impedance state.

2533 tbl 05

REGISTER FUNCTION TABLE⁽¹⁾
(Applies to A or B Register)

D	Inputs		Internal Q	Function
	CP	CE		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2533 tbl 06

OUTPUT CONTROL⁽¹⁾

\overline{OE}	Internal Q	Y-Outputs		Function
		52	53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2533 tbl 07

NOTE:
1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2533 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
- Inputs and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
CIO	I/O Capacitance	VOU = 0V	8	12	pF

NOTE:

2533 tbl 02

- This parameter is guaranteed by characterization data and not tested.

T-52-31

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: VLC = 0.2V; VHC = Vcc - 0.2V

Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
VIH	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
VIL	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
IiH	Input HIGH Current (Except I/O Pins)	Vcc = Max. VI = Vcc VI = 2.7V VI = 0.5V	—	—	5	µA	
IiL	Input LOW Current (Except I/O Pins)		—	—	-5 ⁽⁴⁾		
			VI = GND	—	—		-5
IiH	Input HIGH Current (I/O Pins Only)	Vcc = Max. VI = Vcc VI = 2.7V VI = 0.5V VI = GND	—	—	15	µA	
IiL	Input LOW Current (I/O Pins Only)		—	—	-15 ⁽⁴⁾		
			VI = GND	—	—		-15
VIK	Clamp Diode Voltage	Vcc = Min., IN = -18mA	—	-0.7	-1.2	V	
Ios	Short Circuit Current	Vcc = Max. ⁽³⁾ , Vo = GND	-60	-120	—	mA	
VOH	Output HIGH Voltage	Vcc = 3V, VIN = VLC or VHC, IOH = -32µA	VHC	Vcc	—	V	
		Vcc = Min. VIN = VIH or VIL	IOH = -300µA	VHC	Vcc		—
			IOH = -15mA MIL.	2.4	4.0		—
			IOH = -24mA COM'L.	2.4	4.0		—
VOL	Output LOW Voltage	Vcc = 3V, VIN = VLC or VHC, IOL = 300µA	—	GND	VLC	V	
		Vcc = Min. VIN = VIH or VIL	IOL = 300µA	—	GND		VLC ⁽⁴⁾
			IOL = 48mA MIL. ⁽⁵⁾	—	0.3		0.55
			IOL = 64mA COM'L. ⁽⁵⁾	—	0.3		0.55

NOTES:

2533 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- These are maximum IOL values per output, for 8 outputs turned on simultaneously. Total maximum IOL (all outputs) is 512mA for commercial and 384mA for military. Derate IOL for number of outputs exceeding 8 turned on simultaneously.



POWER SUPPLY CHARACTERISTICS

T-52-31

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.5	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OEA or OEB = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OEA or OEB = GND One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	2.0	4.0	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.5	6.0	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle OEA or OEB = GND Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	4.3	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.5	16.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC} DH + I_{CCD} (f_{CP}/2 + f_iN_i)
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

2533 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T-52-31

Symbol	Parameter	Condition ⁽¹⁾	IDT29FCT52A/53A				IDT29FCT52B/53B				IDT29FCT52C/53C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
IPLH tPHL	Propagation Delay CPA, CPB to A _n , B _n	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	2.0	6.3	2.0	7.3	ns
IPZH tPZL	Output Enable Time OEA or OEB to A _n or B _n		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	7.0	1.5	8.0	ns
IPHZ tPLZ	Output Disable Time OEA or OEB to A _n or B _n		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	1.5	6.5	1.5	7.5	ns
tsu	Set-up Time HIGH or LOW A _n , B _n to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW A _n , B _n to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tsu	Set-up Time HIGH or LOW CEA, CEB to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW CEA, CEB to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width, HIGH ⁽³⁾ or LOW CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

NOTES:

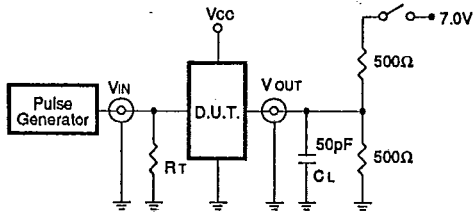
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2533 b1 08



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



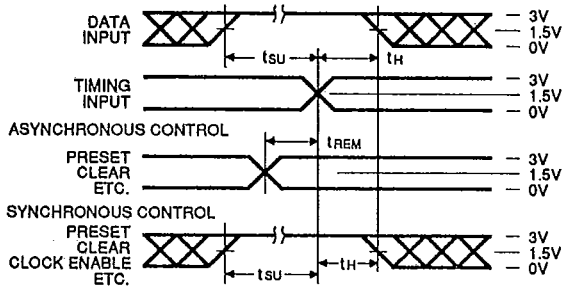
SWITCH POSITION

T-52-31

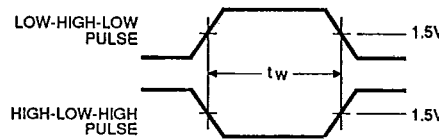
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS: 2533 tbl 09
 CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Zout of the Pulse Generator.

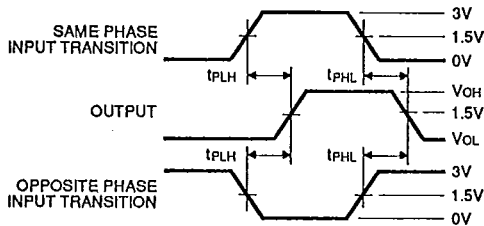
SET-UP, HOLD AND RELEASE TIMES



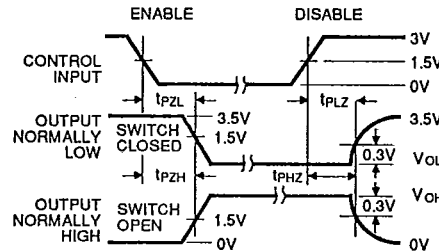
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



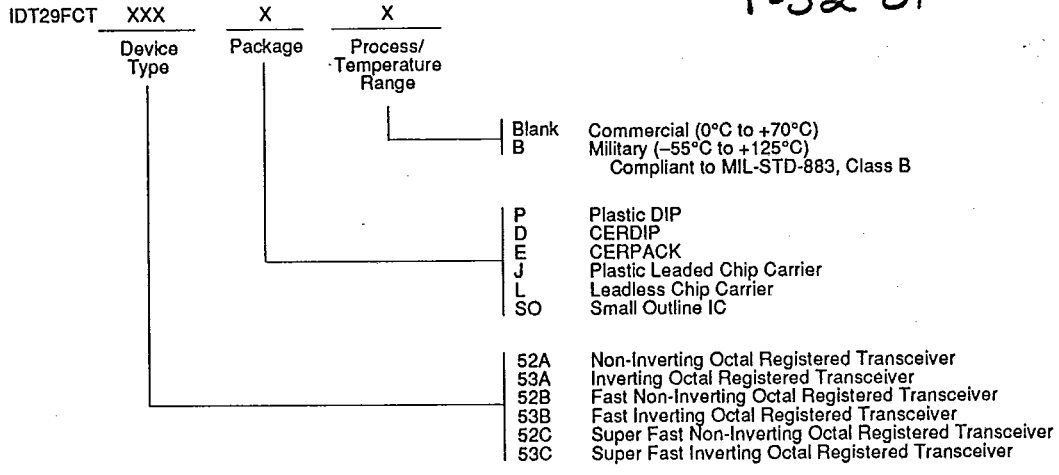
- NOTES 2533 drw 04
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
 - Pulse Generator for All Pulses; Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

IDT29FCT52A/B/C, IDT29FCT53A/B/C
FAST CMOS OCTAL REGISTERED TRANSCEIVERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION

T-52-31



2533 dnr 03

