

256K x 16-Bit EDO-Dynamic RAM

HYB 514265BJ-400/40/-45/-50 HYB 314265BJ(L)-45/-50

Preliminary Information

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- EDO - Hyper Page Mode
- Performance:

| | -400 | -40 | -45 | -50 | |
|-----------|------|-----|-----|-----|-----|
| t_{rc} | 69 | 69 | 79 | 89 | ns |
| t_{rac} | 40 | 40 | 45 | 50 | ns |
| t_{cac} | 10 | 10 | 12 | 13 | ns |
| t_{aa} | 20 | 20 | 22 | 25 | ns |
| t_{hpc} | 12,5 | 15 | 18 | 20 | ns |
| t_{hpc} | 80 | 66 | 55 | 50 | MHz |

- Low Power dissipation
 - Active(max.):
120mA / 120mA / 105mA / 95 mA
 - Standby : TTL Inputs (max.) 2.0 mA
 - Standby: CMOS Inputs (max.) 1.0 mA
 - Standby (L-version) 200 μ A

- Power Supply:

| | | |
|--------------------|--------|-------------|
| HYB 514265BJ-400 | +5 V | $\pm 5\%$ |
| HYB 514265BJ-40 | +5 V | $\pm 10\%$ |
| HYB 514265BJ-45 | +5 V | $\pm 10\%$ |
| HYB 514265BJ-50 | +5 V | $\pm 10\%$ |
| HYB 314265BJ(L)-45 | +3.3 V | $\pm 0.3 V$ |
| HYB 314265BJ(L)-50 | +3.3 V | $\pm 0.3 V$ |

- Read, write, read-modify-write, \overline{CAS} -before \overline{RAS} refresh, \overline{RAS} only refresh, hidden refresh mode
- Low Power Version (L) with Self Refresh and 250 μ A self refresh current
- 2 \overline{CAS} / 1 \overline{WE} control
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
512 refresh cycles / 128 ms (L-version)
- Plastic Packages: P-SOJ-40-3 400 mil width

The HYB 5(3)14265BJ(L) is the new generation dynamic RAM organized as 262 144 words by 16-bit. The HYB 5(3)14265BJ(L) utilizes the SIEMENS 16M-CMOS submicron silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5(3)14265BJ(L) to be packed in a standard plastic 400mil wide P-SOJ-40-3 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment.

The HYB314265BJL parts have a very low power "sleep mode" supported by Self Refresh.

Ordering Information

| Type | Ordering Code | Package | Description |
|------------------------|---------------|------------|--|
| 5 V versions: | | | |
| HYB 514265BJ-400 | Q67100-3033 | P-SOJ-40-3 | 5 V 40 ns 256 K x 16 EDO-DRAM |
| HYB 514265BJ-40 | Q67100-3039 | P-SOJ-40-3 | 5 V 40 ns 256 K x 16 EDO-DRAM |
| HYB 514265BJ-45 | Q67100-3035 | P-SOJ-40-3 | 5 V 45 ns 256 K x 16 EDO-DRAM |
| HYB 514265BJ-50 | Q67100-3036 | P-SOJ-40-3 | 5 V 50 ns 256 K x 16 EDO-DRAM |
| 3.3 V versions: | | | |
| HYB 314265BJ-45 | on request | P-SOJ-40-3 | 3.3 V 45 ns 256 K x 16 EDO- DRAM |
| HYB 314265BJ-50 | on request | P-SOJ-40-3 | 3.3 V 50 ns 256 K x 16 EDO- DRAM |
| HYB 314265BJL-45 | on request | P-SOJ-40-3 | 3.3 V Low Power 45 ns 256 K x 16 EDO- DRAM |
| HYB 314265BJL-50 | on request | P-SOJ-40-3 | 3.3 V Low Power 50 ns 256 K x 16 EDO-DRAM |

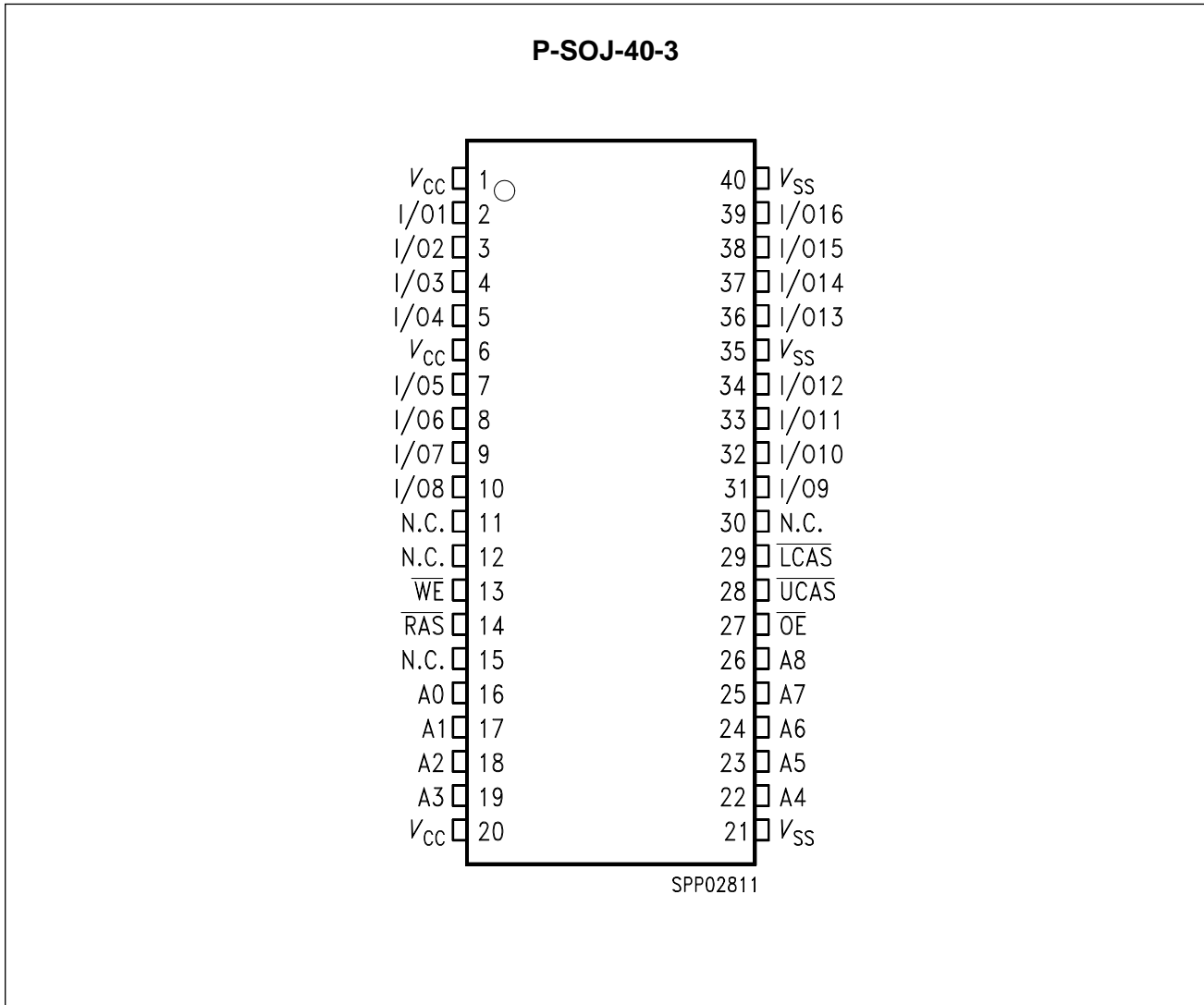
Truth Table

| RAS | LCAS | UCAS | WE | OE | I/O1-I/O8 | I/O9-I/O16 | Operation |
|-----|------|------|----|----|------------|------------|------------------|
| H | H | H | H | H | High-Z | High-Z | Standby |
| L | H | H | H | H | High-Z | High-Z | Refresh |
| L | L | H | H | L | Dout | High-Z | Lower byte read |
| L | H | L | H | L | High-Z | Dout | Upper byte read |
| L | L | L | H | L | Dout | Dout | Word read |
| L | L | H | L | H | Din | Don't care | Lower byte write |
| L | H | L | L | H | Don't care | Din | Upper byte write |
| L | L | L | L | H | Din | Din | Word write |
| L | L | L | H | H | High-Z | High-Z | |

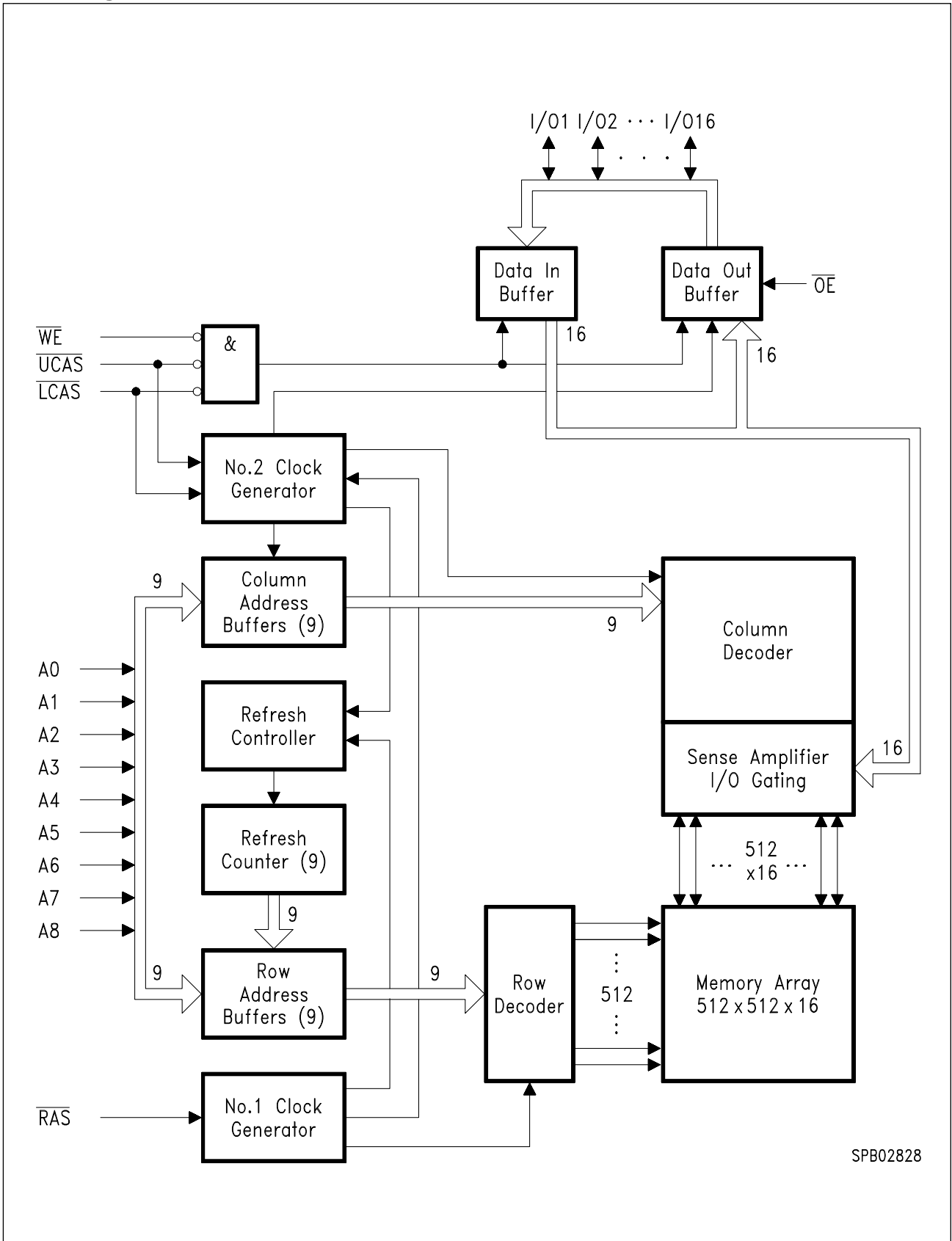
Pin Names

| | |
|-----------------|--|
| A0-A8 | Address Inputs |
| RAS | Row Address Strobe |
| UCAS, LCAS | Column Address Strobe |
| WE | Read/Write Input |
| OE | Output Enable |
| I/O1 – I/O16 | Data Input/Output |
| V _{CC} | Power Supply: + 5 V for HYB 514265, + 3.3 V for HYB 314265 |
| V _{SS} | Ground (0 V) |
| N.C. | No Connection |

Pin Configuration (top view)



Block Diagram



Absolute Maximum Ratings

| | |
|---|---|
| Operating temperature range | 0 to + 70 °C |
| Storage temperature range..... | - 55 to + 150 °C |
| Input/output voltage for HYB 514265..... | - 0.5 to min. ($V_{CC} + 0.5, 7.0$) V |
| Power supply voltage for HYB 514265 | - 1 to + 7 V |
| Input/output voltage for HYB 314265..... | - 0.5 to min. ($V_{CC} + 0.5, 4.6$) V |
| Power supply voltage for HYB 314265 | - 0.5 to + 4.6 V |
| Data out current (short circuit) | 50 mA |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics for HYB514265

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{CC} = 5$ V ± 10 % (± 5 % for -400 version) , $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|------------|--------------|-------------------------|---------|---------|
| | | min. | max. | | |
| Input high voltage | V_{IH} | 2.4 | $V_{CC} + 0.5$ | V | 1 |
| Input low voltage | V_{IL} | - 0.5 | 0.8 | V | 1 |
| Output high voltage ($I_{OUT} = - 5.0$ mA) | V_{OH} | 2.4 | - | V | 1 |
| Output low voltage ($I_{OUT} = 4.2$ mA) | V_{OL} | - | 0.4 | V | 1 |
| Input leakage current, any input (0 V < $V_{IN} < 7$ V, all other inputs = 0 V) | $I_{I(L)}$ | - 10 | 10 | μ A | 1 |
| Output leakage current (DO is disabled, 0 V < $V_{OUT} < V_{CC}$) | $I_{O(L)}$ | - 10 | 10 | μ A | 1 |
| Average V_{CC} supply current: -400 version -40 version -45 version -50 version | I_{CC1} | - | 120 120 105 95 | mA | 2, 3, 4 |
| Standby V_{CC} supply current ($RAS = LCAS = UCAS = WE = V_{IH}$) | I_{CC2} | - | 2 | mA | - |
| Average V_{CC} supply current during \overline{RAS} -only refresh cycles: -400 version -40 version -45 version -50 version | I_{CC3} | - | 120 120 105 95 | mA | 2, 4 |

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--|-----------|--------------|-------------------------|---------------|---------|
| | | min. | max. | | |
| Average V_{CC} supply current during hyper page mode (EDO) operation: -400 version -40 version -45 version -50 version | I_{CC4} | – | 110 90 75 65 | mA | 2, 3, 4 |
| Standby V_{CC} supply current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2\text{ V}$) | I_{CC5} | – | 1 | mA | 1 |
| Standby V_{CC} supply current (L-version only) ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2\text{ V}$) | I_{CC5} | – | 200 | μA | 1 |
| Average V_{CC} supply current during CAS-before-RAS refresh mode: -400 version -40 version -45 version -50 version | I_{CC6} | – | 120 120 105 95 | mA | 2, 4 |

DC Characteristics for 314265

$T_A = 0$ to $70\text{ }^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 2\text{ ns}$

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|------------|--------------|----------------|---------------|----------------|
| | | min. | max. | | |
| Input high voltage | V_{IH} | 2.0 | $V_{CC} + 0.5$ | V | 1 |
| Input low voltage | V_{IL} | – 0.5 | 0.8 | V | 1 |
| TTL Output high voltage ($I_{OUT} = -2.0\text{ mA}$) | V_{OH} | 2.4 | – | V | 1 |
| TTL Output low voltage ($I_{OUT} = 2\text{ mA}$) | V_{OL} | – | 0.4 | V | 1 |
| CMOS Output high voltage ($I_{OUT} = -100\text{ }\mu\text{A}$) | V_{OH} | 2.4 | – | V | 1 |
| CMOS Output low voltage ($I_{OUT} = 100\text{ }\mu\text{A}$) | V_{OL} | – | 0.4 | V | 1 |
| Input leakage current, any input ($0\text{ V} < V_{IN} < V_{CC} + 0.3\text{ V}$, all other inputs = 0 V) | $I_{I(L)}$ | – 10 | 10 | μA | 1 |
| Output leakage current (DO is disabled, $0\text{ V} < V_{OUT} < V_{CC} + 0.3\text{ V}$) | $I_{O(L)}$ | – 10 | 10 | μA | 1 |
| Average V_{CC} supply current: -45 version -50 version | I_{CC1} | – | 105 95 | mA | 2, 3, 4 |
| Standby V_{CC} supply current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{IH}$) | I_{CC2} | – | 2 | mA | – |

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|-----------|--------------|-----------|---------|----------------|
| | | min. | max. | | |
| Average V_{CC} supply current during RAS-only refresh cycles: -45 version -50 version | I_{CC3} | – | 105 95 | mA | 2, 4 |
| Average V_{CC} supply current during hyper page mode (EDO) operation: -45 version -50 version | I_{CC4} | – | 75 65 | mA | 2, 3, 4 |
| Standby V_{CC} supply current ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2 V$) | I_{CC5} | – | 1 | mA | 1 |
| Standby V_{CC} supply current (L-version only) ($\overline{RAS} = \overline{LCAS} = \overline{UCAS} = \overline{WE} = V_{CC} - 0.2 V$) | I_{CC5} | – | 200 | μA | 1 |
| Average V_{CC} supply current during \overline{CAS} -before- \overline{RAS} refresh mode: -45 version -50 version | I_{CC6} | – | 105 95 | mA | 2, 4 |
| Self Refresh Current (L-version only) CBR cycle with $\overline{RAS} > t_{rasss}(\text{min})$, CAS held low; $\overline{WE} = V_{CC} - 0.2 V$, Addresses and Din = $V_{CC} - 0.2 V$ or 0.2 V | I_{CC7} | – | 250 | μA | |

Capacitance

$T_A = 0$ to 70 °C; $f = 1$ MHz

| Parameter | Symbol | Limit Values | | Unit |
|--|----------|--------------|------|------|
| | | min. | max. | |
| Input capacitance (A0 to A8) | C_{11} | – | 5 | pF |
| Input capacitance (\overline{RAS} , \overline{UCAS} , \overline{LCAS} , \overline{WE} , \overline{OE}) | C_{12} | – | 7 | pF |
| Output capacitance (I/O1 to I/O16) | C_{10} | – | 7 | pF |

AC Characteristics ^{5) 6)}

$T_A = 0$ to 70 °C, $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -400 | | -40 | | | |
| | | min. | max. | min. | max. | | |

Common Parameters

| | | | | | | | |
|----------------------------------|-----------|-----|-----|----|-----|----|---|
| Random read or write cycle time | t_{RC} | 69 | – | 69 | – | ns | |
| RAS precharge time | t_{RP} | 25 | – | 25 | – | ns | |
| RAS pulse width | t_{RAS} | 40 | 10k | 40 | 10k | ns | |
| CAS pulse width | t_{CAS} | 4.5 | 10k | 6 | 10k | ns | |
| CAS precharge time | t_{CP} | 4 | – | 5 | – | ns | |
| Row address setup time | t_{ASR} | 0 | – | 0 | – | ns | |
| Row address hold time | t_{RAH} | 5 | – | 5 | – | ns | |
| Column address setup time | t_{ASC} | 0 | – | 0 | – | ns | |
| Column address hold time | t_{CAH} | 5 | – | 5 | – | ns | |
| RAS to CAS delaytime | t_{RCD} | 9 | 30 | 9 | 30 | ns | |
| RAS to column address delay time | t_{RAD} | 7 | 20 | 7 | 20 | ns | |
| RAS hold time | t_{RSH} | 6 | – | 6 | – | ns | |
| CAS hold time | t_{CSH} | 32 | – | 32 | – | ns | |
| CAS to RAS precharge time | t_{CRP} | 5 | – | 5 | – | ns | |
| Transition time(rise and fall) | t_T | 1 | 50 | 1 | 50 | ns | 7 |
| Refresh period | t_{REF} | 16 | – | 16 | – | ms | |

Read Cycle

| | | | | | | | |
|---------------------------------------|-----------|----|----|----|----|----|------|
| Access time from RAS | t_{RAC} | – | 40 | – | 40 | ns | 8, 9 |
| Access time from CAS | t_{CAC} | – | 10 | – | 10 | ns | 8, 9 |
| Access time from column address | t_{AA} | – | 17 | – | 20 | ns | 8,10 |
| OE access time | t_{OEA} | – | 10 | – | 10 | ns | |
| Column address to RAS lead time | t_{RAL} | 20 | – | 20 | – | ns | |
| Read command setup time | t_{RCS} | 0 | – | 0 | – | ns | |
| Read command hold time | t_{RCH} | 0 | – | 0 | – | ns | 11 |
| Read command hold time ref. to RAS | t_{RRH} | 0 | – | 0 | – | ns | 11 |
| CAS to output inlow-Z | t_{CLZ} | 0 | – | 0 | – | ns | 8 |
| Output buffer turn-off delay from CAS | t_{OFF} | 0 | – | 0 | 10 | ns | 12 |

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|---|-----------|--------------|------|------|------|------|------|
| | | -400 | | -40 | | | |
| | | min. | max. | min. | max. | | |
| Output buffer turn-off delay from \overline{OE} | t_{OEZ} | 0 | 10 | 0 | 10 | ns | 12 |
| Data to \overline{OE} low delay | t_{DZO} | 0 | – | 0 | – | ns | 13 |
| \overline{CAS} high to data delay | t_{CDD} | 8 | – | 8 | – | ns | 14 |
| \overline{OE} high to data delay | t_{ODD} | 8 | – | 8 | – | ns | 14 |
| Data to \overline{CAS} low delay | t_{DZC} | 0 | – | 0 | – | ns | 13 |

Write Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|----|
| Write command hold time | t_{WCH} | 5 | – | 5 | – | ns | |
| Write command pulse width | t_{WCP} | 5 | – | 5 | – | ns | |
| Write command setup time | t_{WCS} | 0 | – | 0 | – | ns | 15 |
| Write command to \overline{RAS} lead time | t_{RWL} | 10 | – | 10 | – | ns | |
| Write command to \overline{CAS} lead time | t_{CWL} | 10 | – | 10 | – | ns | |
| Data setup time | t_{DS} | 0 | – | 0 | – | ns | 16 |
| Data hold time | t_{DH} | 5 | – | 5 | – | ns | 16 |
| Data to \overline{CAS} low delay | t_{DZC} | 0 | – | 0 | – | ns | 13 |

Read-modify-Write Cycle

| | | | | | | | |
|--|-----------|----|---|----|---|----|----|
| Read-write cycle time | t_{RWC} | 93 | – | 93 | – | ns | |
| \overline{RAS} to \overline{WE} delay time | t_{RWD} | 52 | – | 52 | – | ns | 15 |
| \overline{CAS} to \overline{WE} delay time | t_{CWD} | 22 | – | 22 | – | ns | 15 |
| Column address to \overline{WE} delay time | t_{AWD} | 32 | – | 32 | – | ns | 15 |
| \overline{OE} command hold time | t_{OEH} | 5 | – | 5 | – | ns | |

Hyper Page Mode (EDO) Cycle

| | | | | | | | |
|--|------------|------|------|----|------|----|---|
| Hyper page mode cycle time | t_{HPC} | 12.5 | – | 15 | – | ns | |
| Access time from \overline{CAS} precharge | t_{CPA} | – | 17 | – | 21 | ns | 7 |
| Output data hold time | t_{COH} | 3 | – | 3 | – | ns | |
| \overline{RAS} pulse width in hyper page mode | t_{RAS} | 40 | 200k | 40 | 200k | ns | |
| \overline{RAS} hold time from \overline{CAS} precharge | t_{RHCP} | 17 | – | 21 | – | ns | |

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -400 | | -40 | | | |
| | | min. | max. | min. | max. | | |

Hyper Page Mode (EDO) Read-Modify-Write Cycle

| | | | | | | | |
|--|------------|----|---|----|---|----|--|
| Hyper page mode read/write cycle time | t_{PRWC} | 55 | – | 55 | – | ns | |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time | t_{CPWD} | 35 | – | 35 | – | ns | |

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ setup time | t_{CSR} | 5 | – | 5 | – | ns | |
| $\overline{\text{CAS}}$ hold time | t_{CHR} | 5 | – | 5 | – | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | t_{RPC} | 5 | – | 5 | – | ns | |
| Write to $\overline{\text{RAS}}$ precharge time | t_{WRP} | 10 | – | 10 | – | ns | |
| Write to $\overline{\text{RAS}}$ hold time | t_{WRH} | 10 | – | 10 | – | ns | |

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

| | | | | | | | |
|--|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ precharge time | t_{CPT} | 25 | – | 25 | – | ns | |
|--|-----------|----|---|----|---|----|--|

AC Characteristics ⁵⁾⁶⁾

16E

$T_A = 0$ to 70 °C, $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -45 | | -50 | | | |
| | | min. | max. | min. | max. | | |

Common Parameters

| | | | | | | | |
|---|-----------|----|-----|----|-----|----|---|
| Random read or write cycle time | t_{RC} | 79 | – | 89 | – | ns | |
| \overline{RAS} precharge time | t_{RP} | 30 | – | 35 | – | ns | |
| RAS pulse width | t_{RAS} | 45 | 10k | 50 | 10k | ns | |
| CAS pulse width | t_{CAS} | 7 | 10k | 8 | 10k | ns | |
| \overline{CAS} precharge time | t_{CP} | 7 | – | 8 | – | ns | |
| Row address setup time | t_{ASR} | 0 | – | 0 | – | ns | |
| Row address hold time | t_{RAH} | 7 | – | 8 | – | ns | |
| Column address setup time | t_{ASC} | 0 | – | 0 | – | ns | |
| Column address hold time | t_{CAH} | 7 | – | 8 | – | ns | |
| RAS to CAS delay time | t_{RCD} | 11 | 33 | 12 | 37 | ns | |
| \overline{RAS} to column address delay | t_{RAD} | 9 | 23 | 10 | 25 | ns | |
| RAS hold time | t_{RSH} | 12 | | 13 | – | ns | |
| \overline{CAS} hold time | t_{CSH} | 36 | | 40 | – | ns | |
| \overline{CAS} to \overline{RAS} precharge time | t_{CRP} | 5 | – | 5 | – | ns | |
| Transition time (rise and fall) | t_T | 1 | 50 | 1 | 50 | ns | 7 |
| Refresh period | t_{REF} | – | 16 | – | 16 | ms | |
| Refresh period (L-version only) | t_{REF} | – | 128 | – | 128 | ms | |

Read Cycle

| | | | | | | | |
|---|-----------|----|----|----|----|----|------|
| Access time from \overline{RAS} | t_{RAC} | – | 45 | – | 50 | ns | 8, 9 |
| Access time from \overline{CAS} | t_{CAC} | – | 12 | – | 13 | ns | 8, 9 |
| Access time from column address | t_{AA} | – | 22 | – | 25 | ns | 8,10 |
| \overline{OE} access time | t_{OEA} | – | 12 | – | 13 | ns | |
| Column address to \overline{RAS} lead time | t_{RAL} | 23 | – | 25 | – | ns | |
| Read command setup time | t_{RCS} | 0 | – | 0 | – | ns | |
| Read command hold time | t_{RCH} | 0 | – | 0 | – | ns | 11 |
| Read command hold time referenced to \overline{RAS} | t_{RRH} | 0 | – | 0 | – | ns | 11 |
| \overline{CAS} to output in low-Z | t_{CLZ} | 0 | – | 0 | – | ns | 8 |

AC Characteristics (cont'd) ⁵⁾⁶⁾

16E

$T_A = 0$ to 70 °C, $t_r = 2$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|--|-----------|--------------|------|------|------|------|------|
| | | -45 | | -50 | | | |
| | | min. | max. | min. | max. | | |
| Output buffer turn-off delay | t_{OFF} | 0 | 12 | 0 | 13 | ns | 12 |
| Output turn-off delay from \overline{OE} | t_{OEZ} | 0 | 12 | 0 | 13 | ns | 12 |
| Data to \overline{CAS} low delay | t_{DZC} | 0 | – | 0 | – | ns | 13 |
| Data to \overline{OE} low delay | t_{DZO} | 0 | – | 0 | – | ns | 13 |
| CAS high to data delay | t_{CDD} | 10 | – | 10 | – | ns | 14 |
| OE high to data delay | t_{ODD} | 10 | – | 10 | – | ns | 14 |

Write Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|----|
| Write command hold time | t_{WCH} | 7 | – | 8 | – | ns | |
| Write command pulse width | t_{WCP} | 7 | – | 8 | – | ns | |
| Write command setup time | t_{WCS} | 0 | – | 0 | – | ns | 15 |
| Write command to \overline{RAS} lead time | t_{RWL} | 12 | – | 13 | – | ns | |
| Write command to \overline{CAS} lead time | t_{CWL} | 12 | – | 13 | – | ns | |
| Data setup time | t_{DS} | 0 | – | 0 | – | ns | 16 |
| Data hold time | t_{DH} | 7 | – | 8 | – | ns | 16 |

Read-modify-Write Cycle

| | | | | | | | |
|--|-----------|-----|---|-----|---|----|----|
| Read-write cycle time | t_{RWC} | 107 | – | 118 | – | ns | |
| \overline{RAS} to \overline{WE} delay time | t_{RWD} | 59 | – | 64 | – | ns | 15 |
| \overline{CAS} to \overline{WE} delay time | t_{CWD} | 26 | – | 27 | – | ns | 15 |
| Column address to \overline{WE} delay time | t_{AWD} | 36 | – | 39 | – | ns | 15 |
| \overline{OE} command hold time | t_{OEH} | 7 | – | 10 | – | ns | |

Hyper Page Mode (EDO) Cycle

| | | | | | | | |
|--|------------|----|------|----|------|----|---|
| Hyper page mode (EDO) cycle time | t_{HPC} | 18 | – | 20 | – | ns | |
| Access time from \overline{CAS} precharge | t_{CPA} | – | 25 | – | 27 | ns | 7 |
| Output data hold time | t_{COH} | 5 | – | 5 | – | ns | |
| \overline{RAS} pulse width in EDO mode | t_{RAS} | 45 | 200k | 50 | 200k | ns | |
| \overline{CAS} precharge to \overline{RAS} Delay | t_{RHPC} | 25 | – | 27 | – | ns | |

AC Characteristics (cont'd) ⁵⁾⁶⁾

$T_A = 0$ to 70 °C, $t_T = 2$ ns

| Parameter | Symbol | Limit Values | | | | Unit | Note |
|-----------|--------|--------------|------|------|------|------|------|
| | | -45 | | -50 | | | |
| | | min. | max. | min. | max. | | |

Hyper Page Mode (EDO) Read-modify-Write Cycle

| | | | | | | | |
|---|------------|----|---|----|---|----|--|
| Hyper page mode (EDO) read-write cycle time | t_{PRWC} | 51 | – | 58 | – | ns | |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ | t_{CPWD} | 41 | – | 41 | – | ns | |

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

| | | | | | | | |
|---|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ setup time | t_{CSR} | 5 | – | 10 | – | ns | |
| $\overline{\text{CAS}}$ hold time | t_{CHR} | 10 | – | 10 | – | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | t_{RPC} | 5 | – | 5 | – | ns | |
| Write to $\overline{\text{RAS}}$ precharge time | t_{WRP} | 10 | – | 10 | – | ns | |
| Write hold time referenced to $\overline{\text{RAS}}$ | t_{WRH} | 10 | – | 10 | – | ns | |

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Cycle

| | | | | | | | |
|--|-----------|----|---|----|---|----|--|
| $\overline{\text{CAS}}$ precharge time | t_{CPT} | 30 | – | 35 | – | ns | |
|--|-----------|----|---|----|---|----|--|

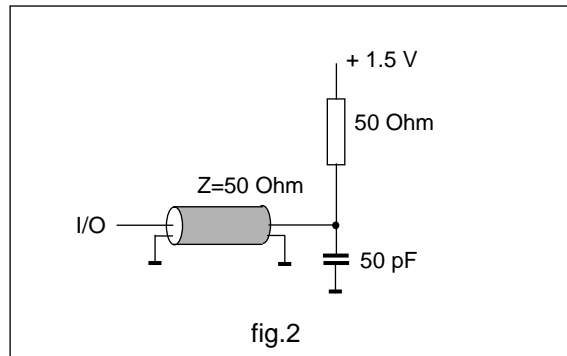
Self Refresh Cycle (L-version)

| | | | | | | | |
|-------------------------------------|------------|------|---|------|---|----|----|
| $\overline{\text{RAS}}$ pulse width | t_{RASS} | 100k | – | 100k | – | ns | 17 |
| $\overline{\text{RAS}}$ precharge | t_{RPS} | 110 | – | 95 | – | ns | 17 |
| $\overline{\text{CAS}}$ hold time | t_{CHS} | – 50 | – | – 50 | – | ns | 17 |

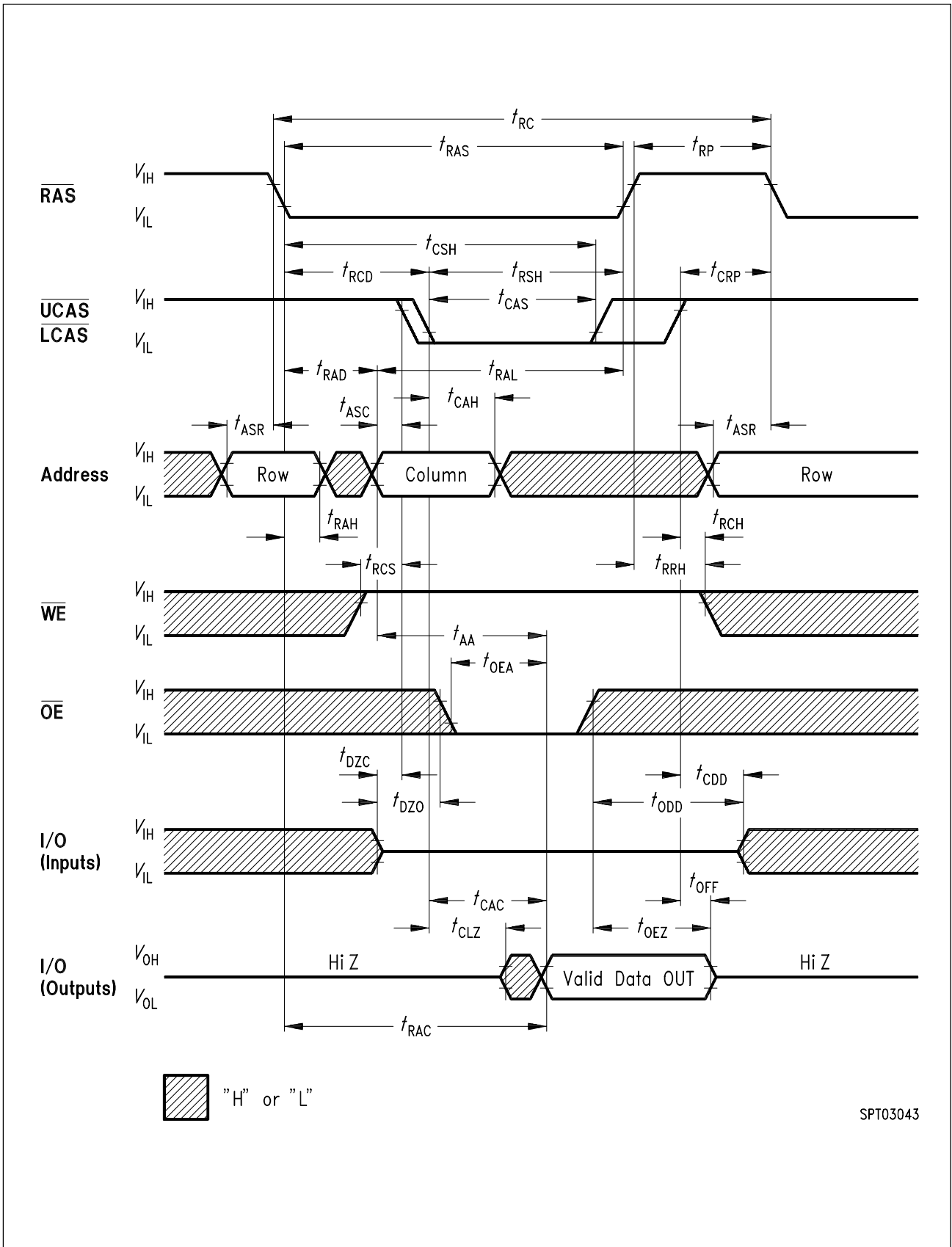
Notes:

- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while $\text{RAS} = V_{IL}$. In case of I_{CC4} it can be changed once or less during a hyper page mode (EDO) cycle
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 6) AC measurements assume $t_T = 2$ ns.

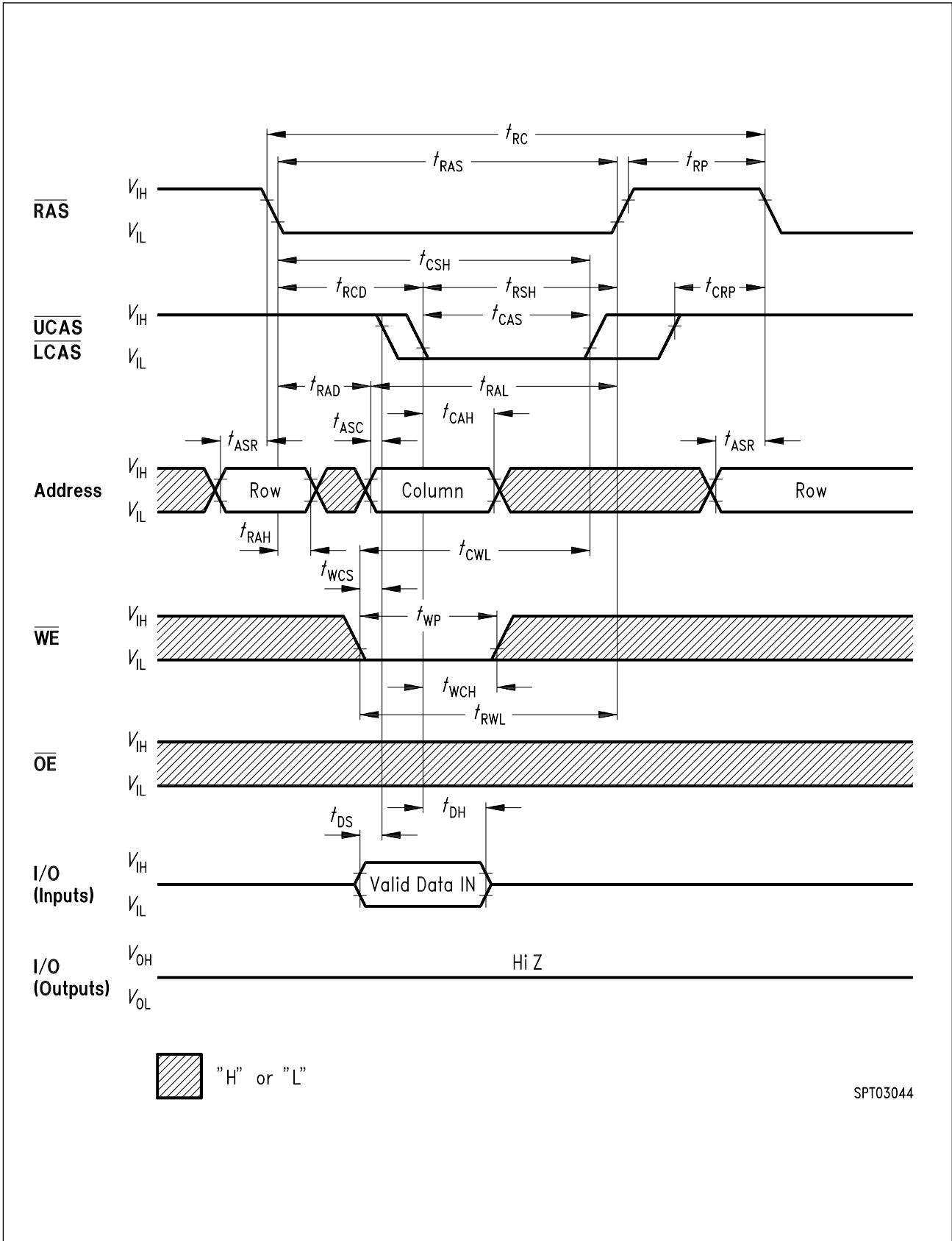
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 50 pF at $V_{OL} = 0.8 V$ and $V_{OH} = 2.0 V$. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{AA} , t_{CPA} , t_{OEA} . t_{CAC} is measured from tristate



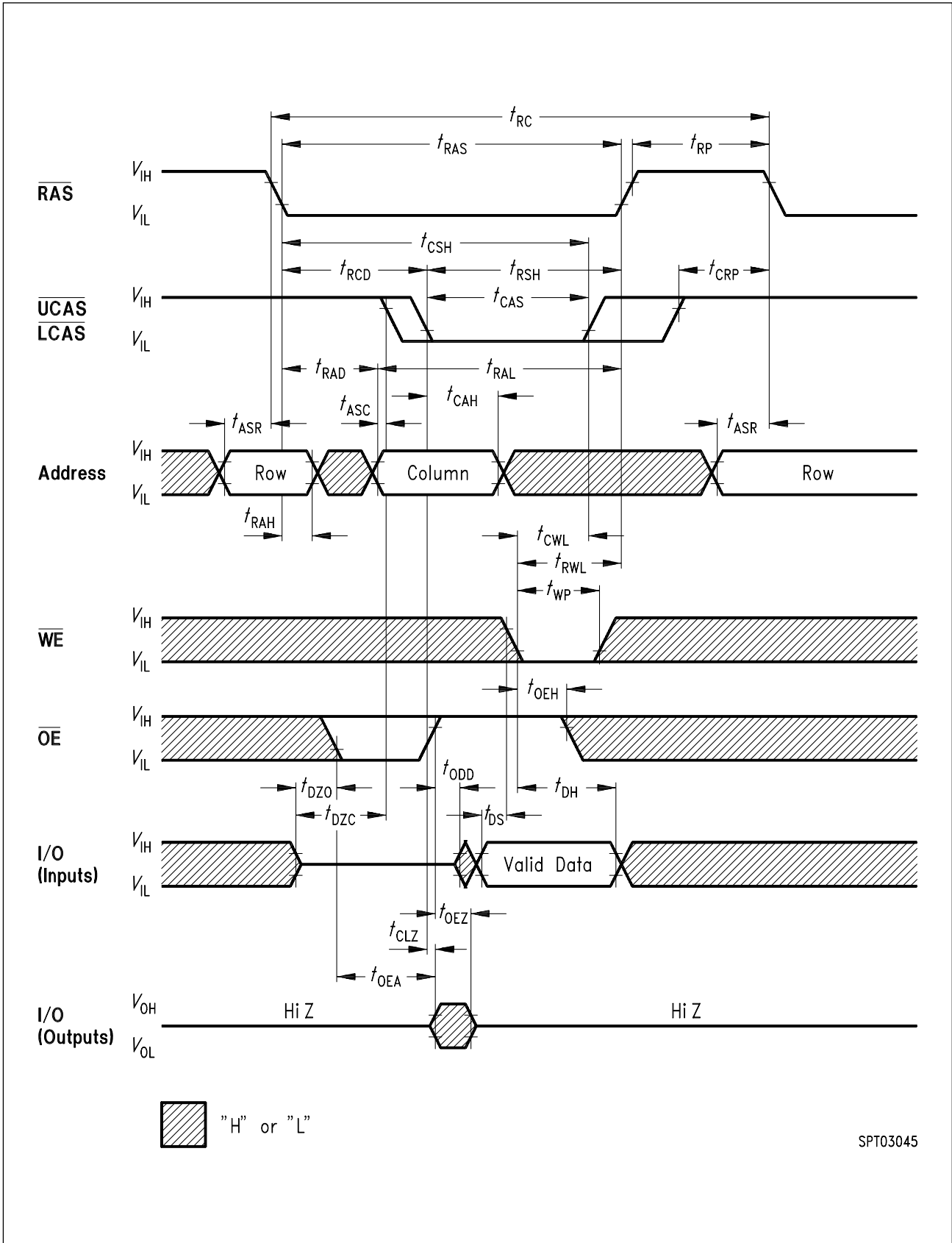
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{CAC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{AA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$, $t_{OEZ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD (min.)}$, $t_{CWD} > t_{CWD (min.)}$ and $t_{AWD} > t_{AWD (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{WE} leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
- If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
- If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.



Read Cycle

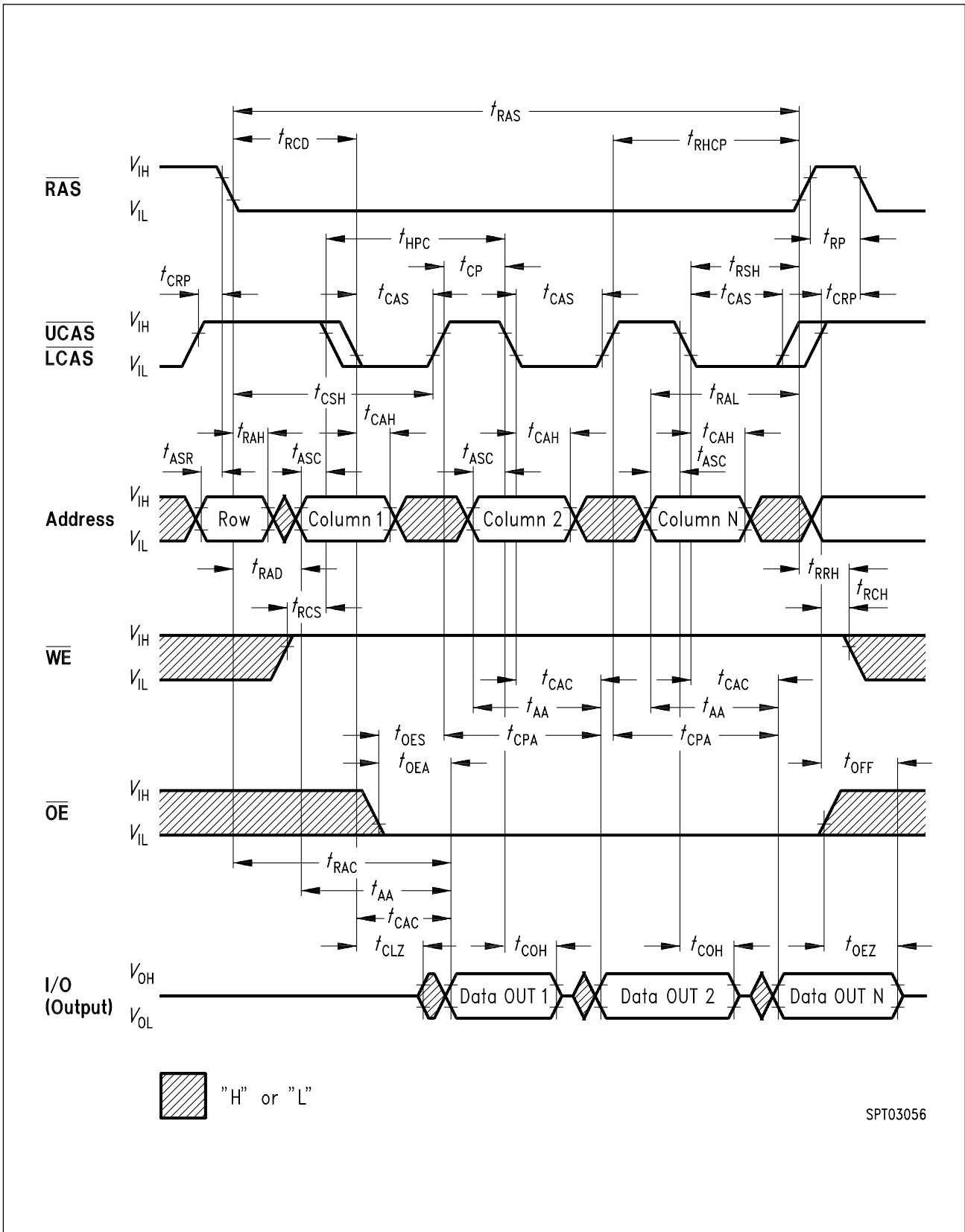


Write Cycle (Early Write)

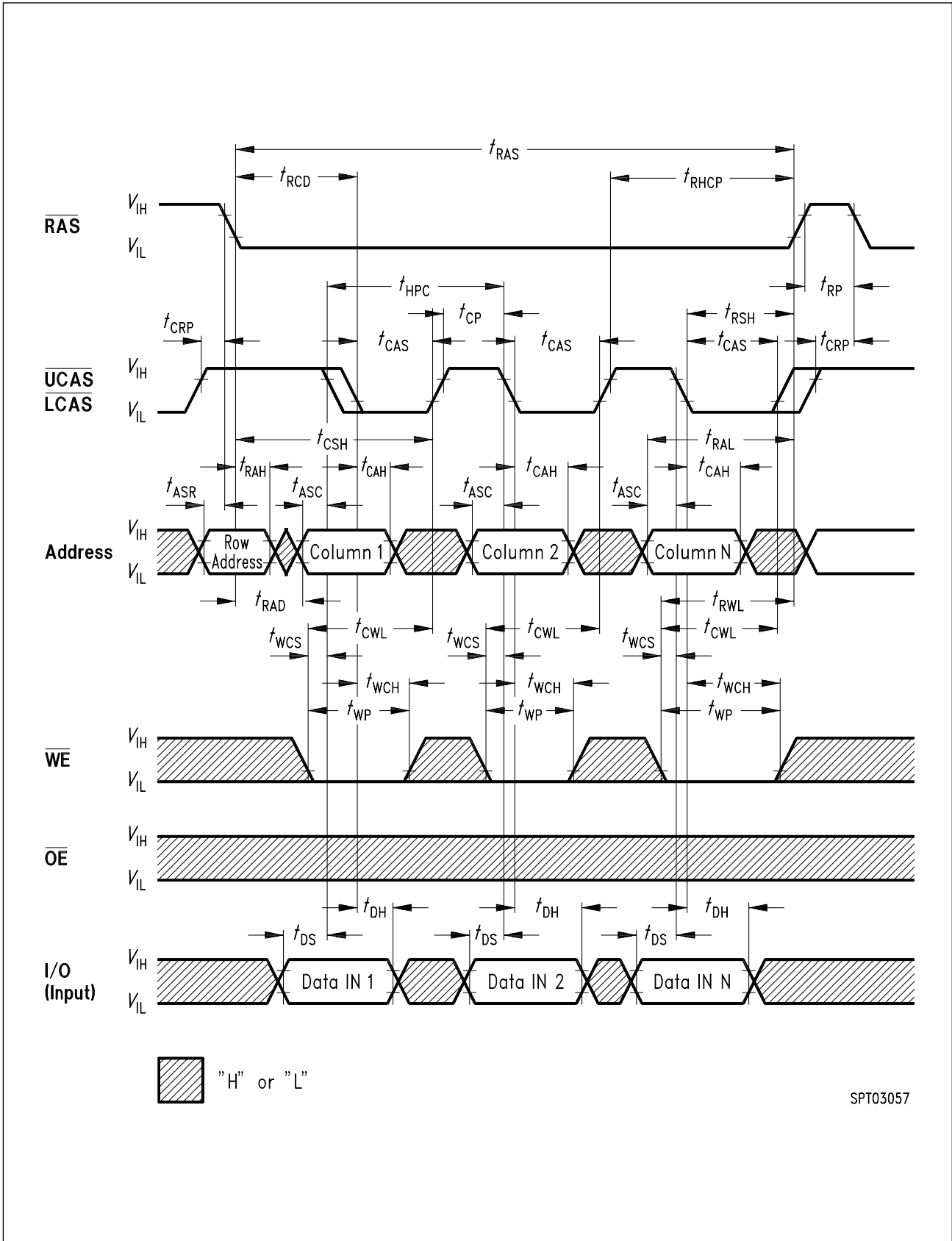


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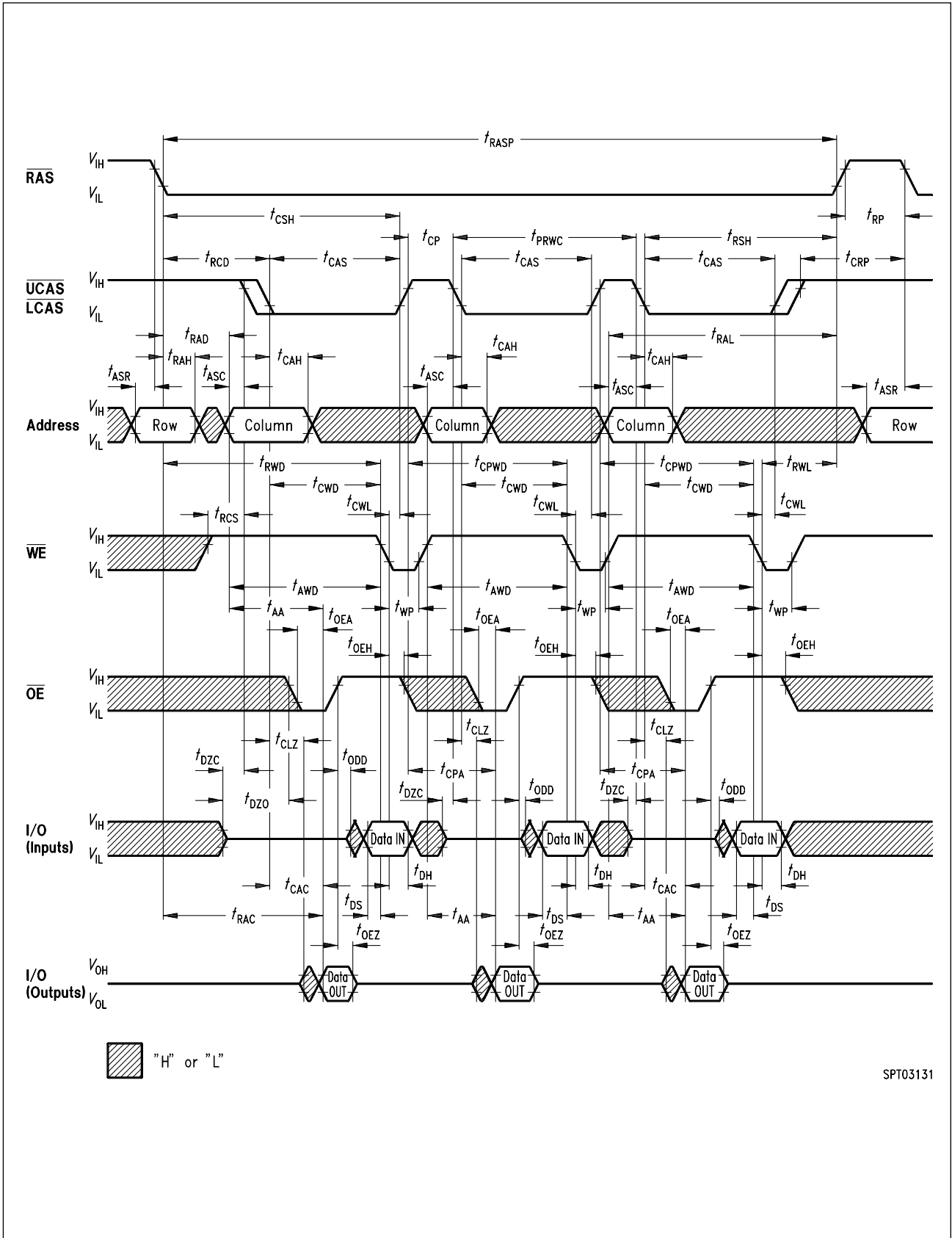
Write Cycle (\overline{OE} Controlled Write)



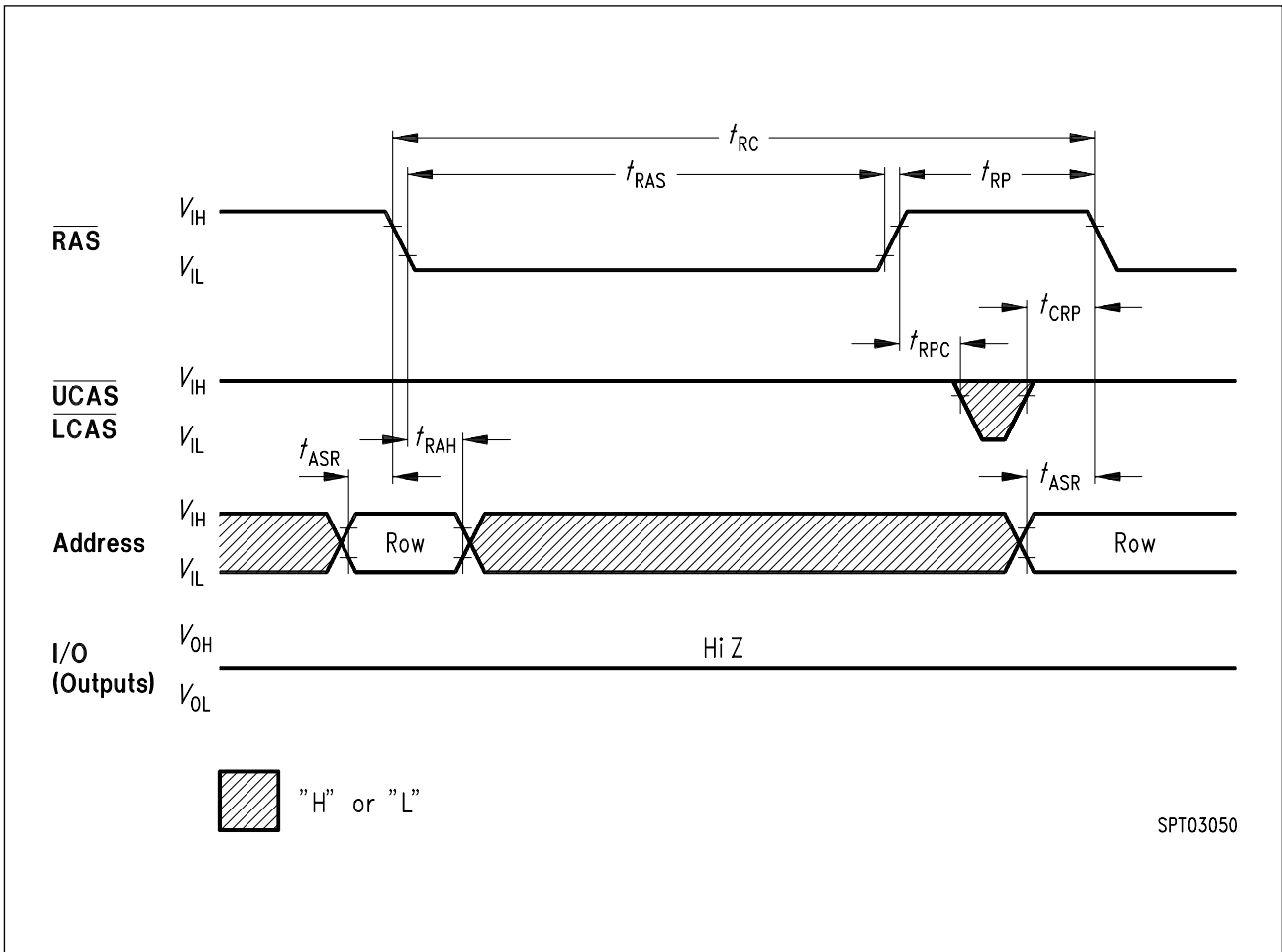
Hyper Page Mode (EDO) Read Cycle



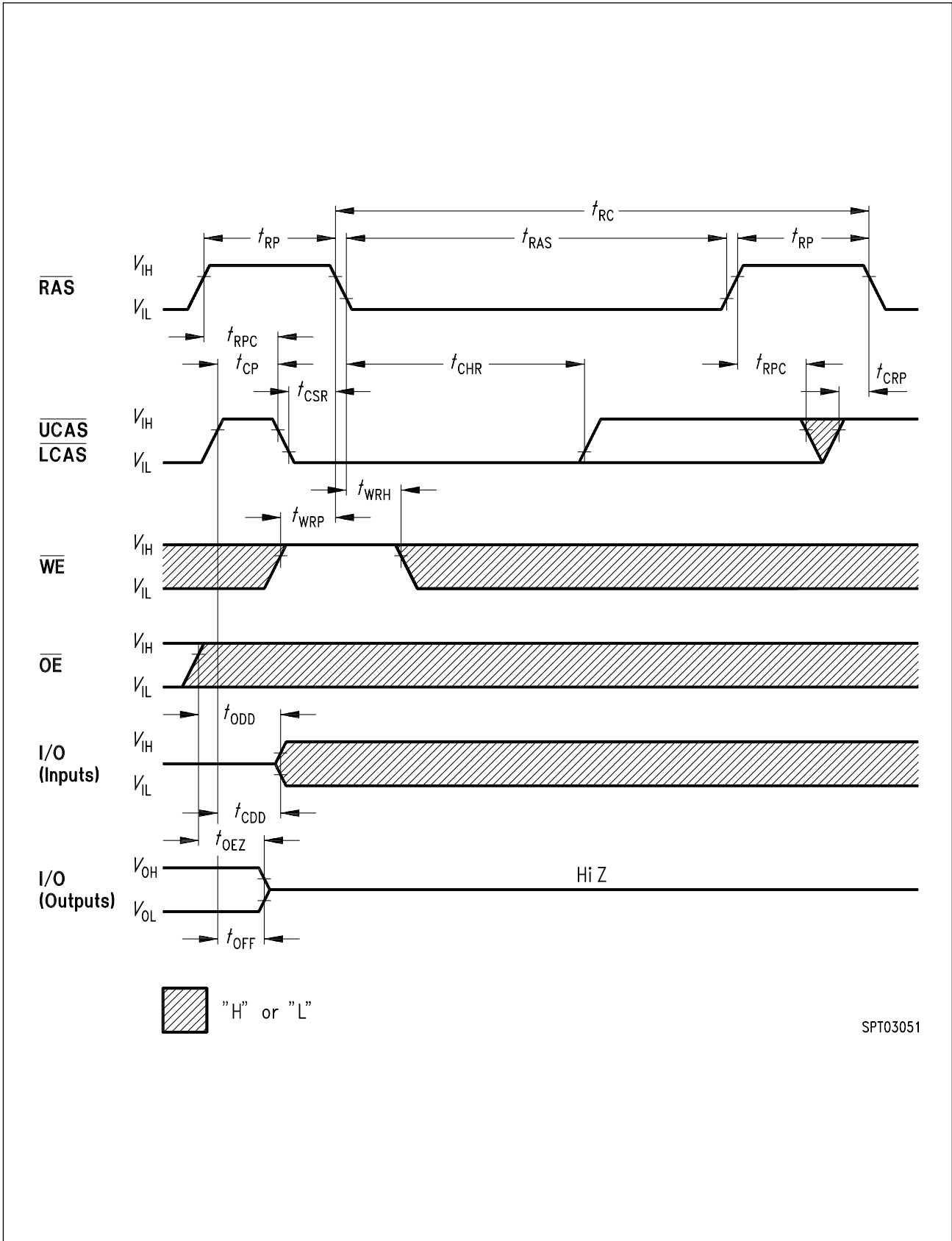
Hyper Page Mode (EDO) Early Write Cycle



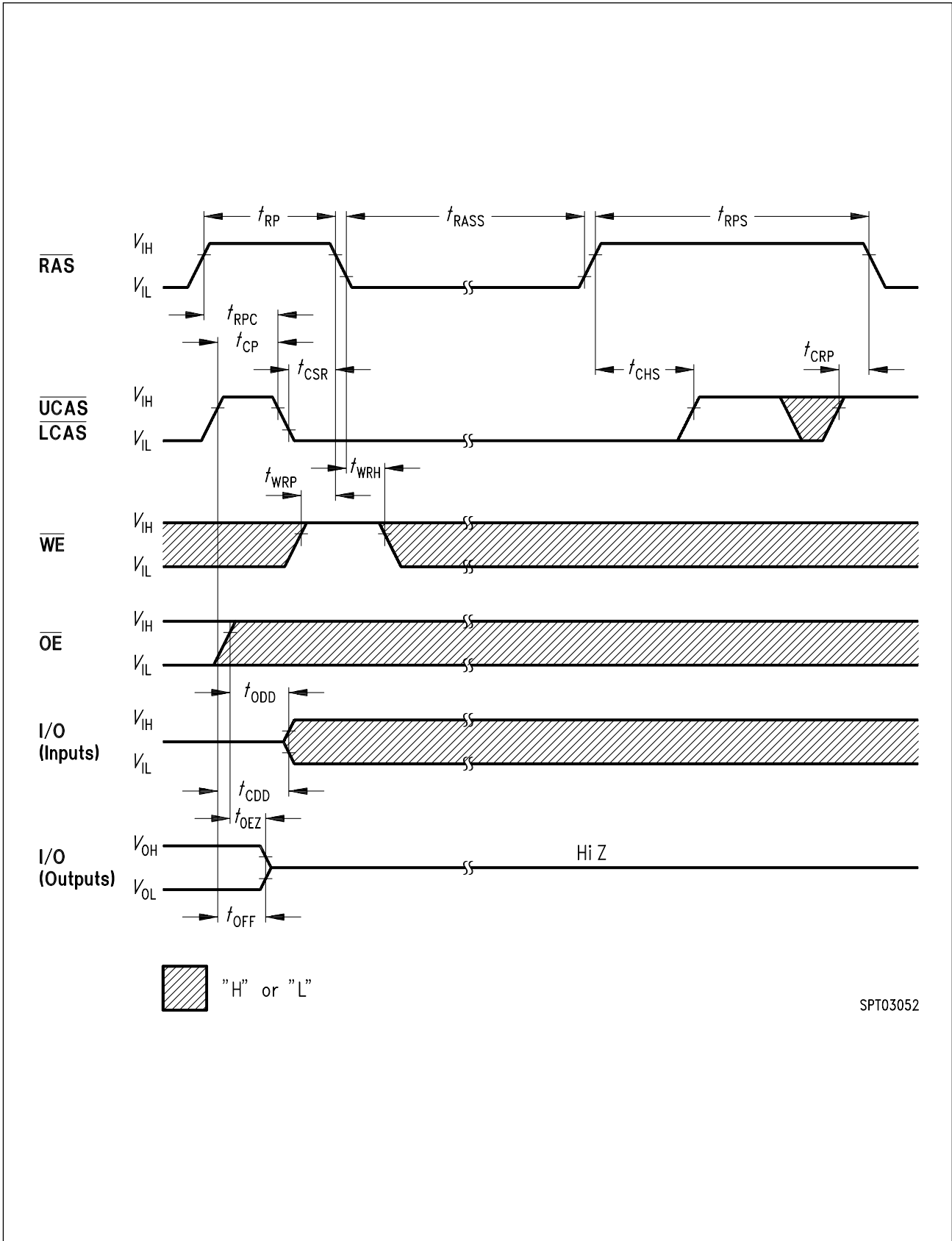
Hyper Page Mode (EDO) Late Write and Read-Modify-Write Cycles



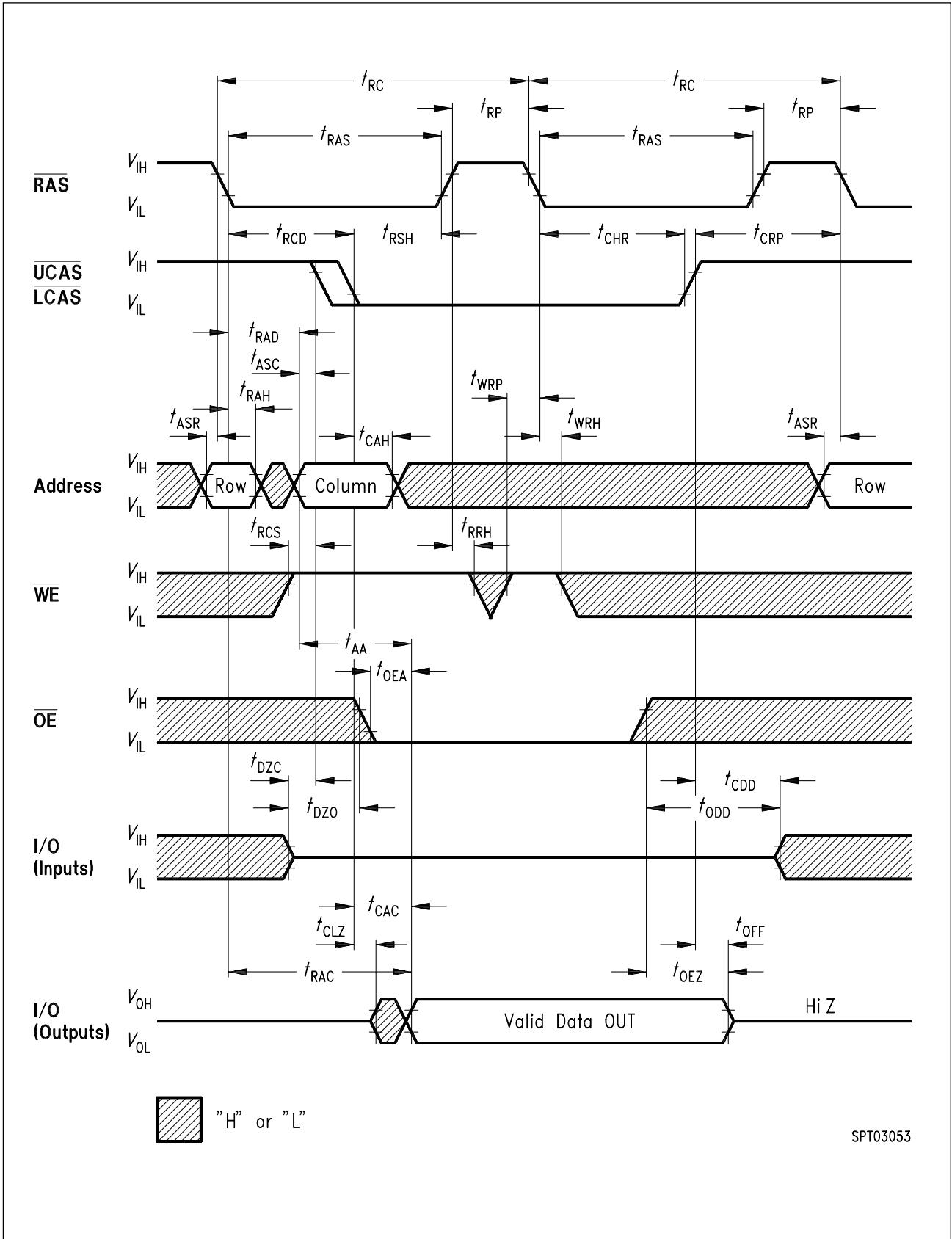
$\overline{\text{RAS}}$ -Only Refresh Cycle



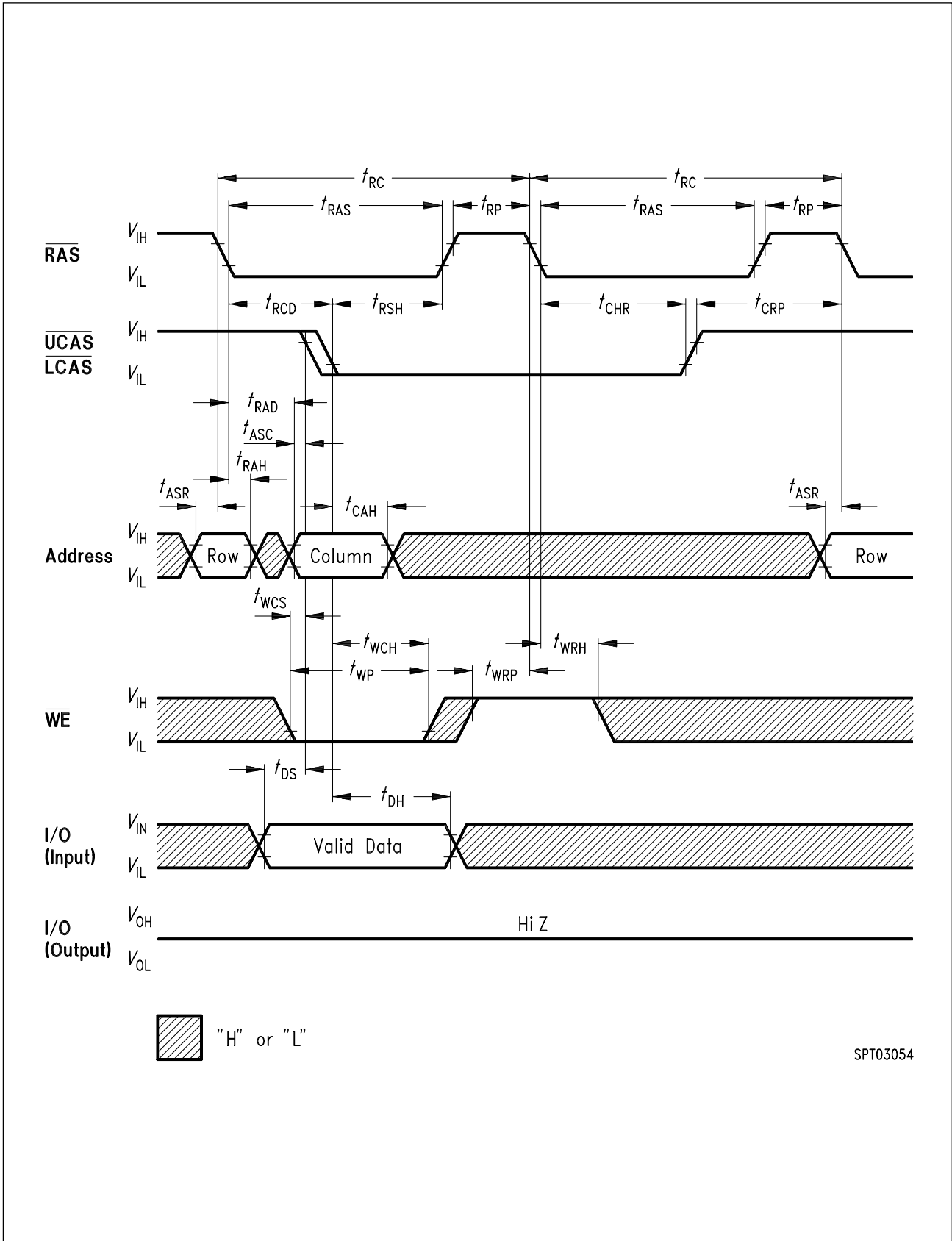
CAS-Before-RAS Refresh Cycle



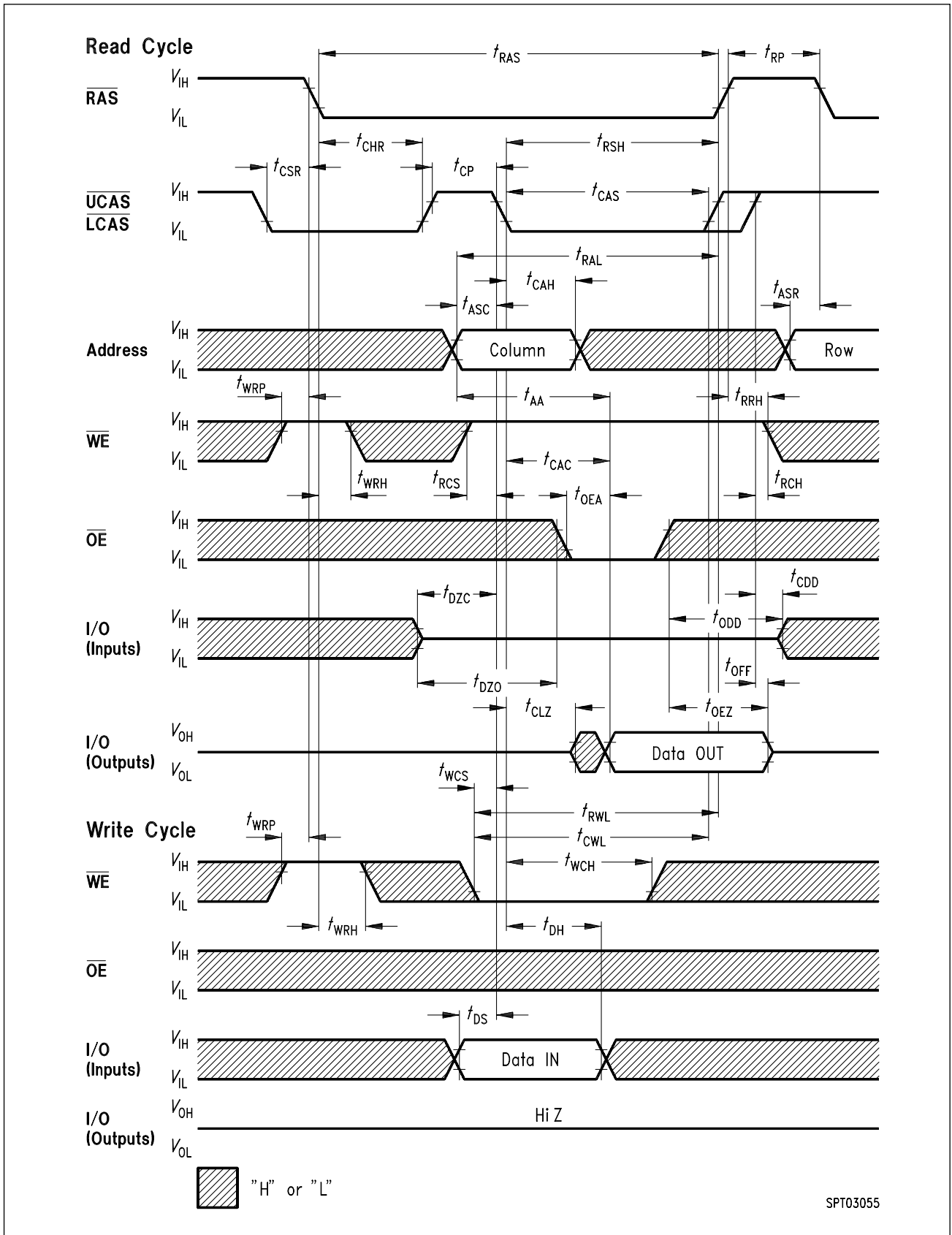
CAS before RAS Self Refresh Cycle



Hidden Refresh Cycle (Read)



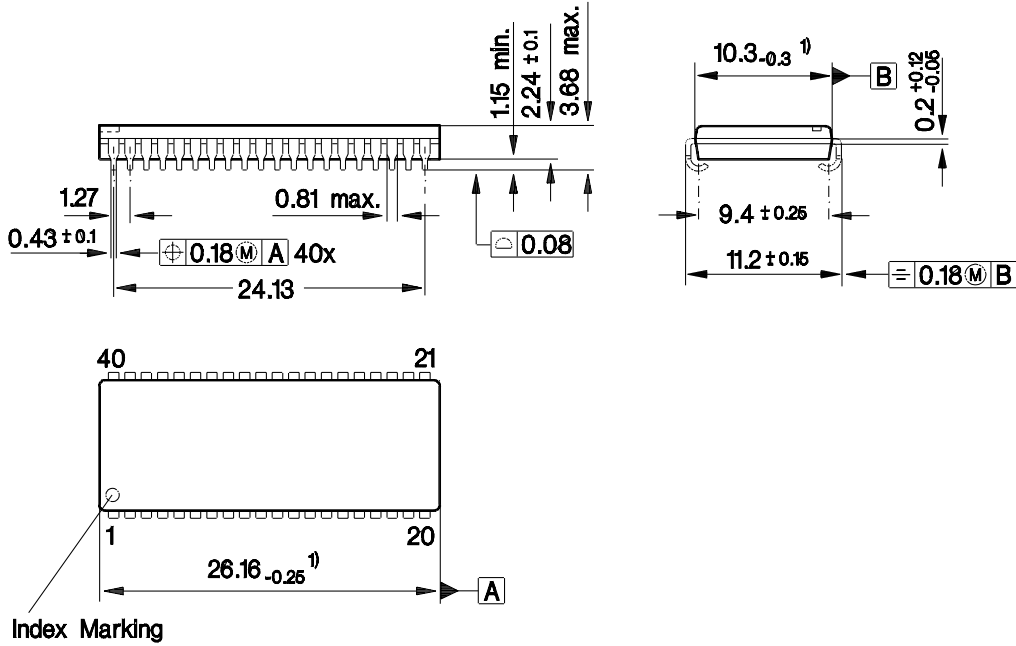
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle

Package Outlines

P-SOJ-40-3
(Small Outline J-Leaded Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPJ09018

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm