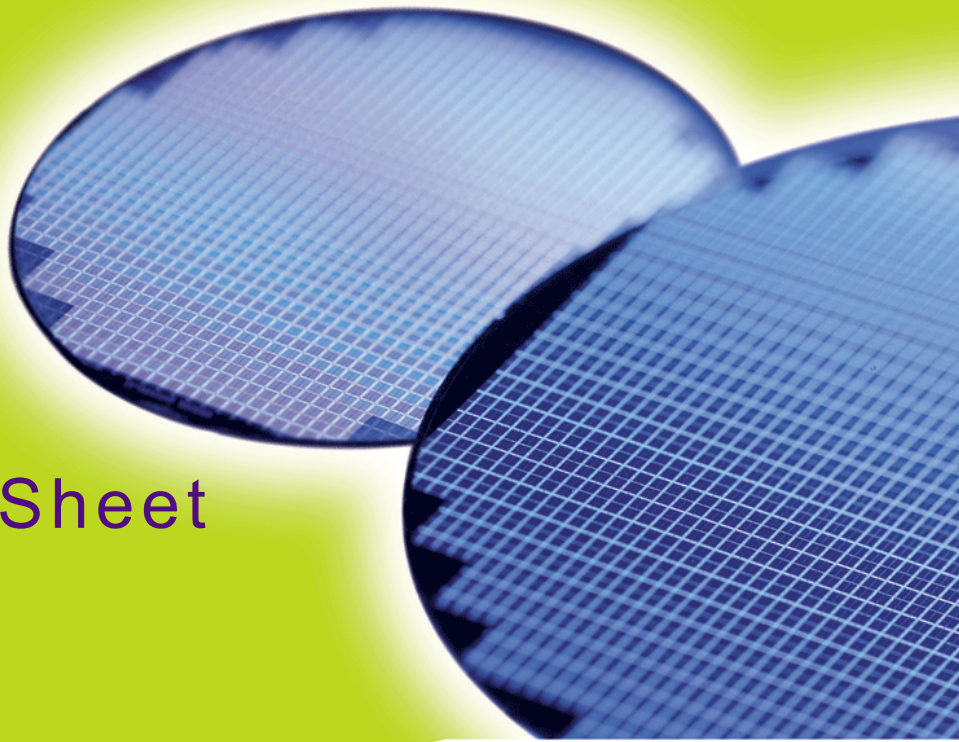


HYB18T512400BF
HYB18T512800BF
HYB18T512160BF

512-Mbit Double-Data-Rate-Two SDRAM
DDR2 SDRAM
RoHS Compliant Products



Internet Data Sheet

Rev. 1.05

HYB18T512xxxBF-[2.5...5]
512-Mbit Double-Data-Rate-Two SDRAM

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1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate-Two SDRAM product family and describes its main characteristics.

1.1 Features

The 512-Mbit Double-Data-Rate-Two SDRAM offers the following key features:

- 1.8 V \pm 0.1 V Power Supply
- 1.8 V \pm 0.1 V (SSTL_18) compatible I/O
- DRAM organizations with 4, 8 and 16 data in/outputs
- Double Data Rate architecture: two data transfers per clock cycle four internal banks for concurrent operation
- Programmable CAS Latency: 3, 4, 5 and 6
- Programmable Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- DQS can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality.
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Average Refresh Period 7.8 μs at a T_{CASE} lower than 85 °C, 3.9 μs between 85 °C and 95 °C
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- Full and reduced Strength Data-Output Drivers
- 1kB page size for $\times 4$ & $\times 8$, 2kB page size for $\times 16$
- Packages: P-TFBGA-60 for $\times 4$ & $\times 8$ components P-TFBGA-84 for $\times 16$ components
- RoHS Compliant Products¹⁾
- All Speed grades faster than DDR400 comply with DDR400 timing specifications when run at a clock rate of 200 MHz.

A list of the performance tables for the various speeds can be found below

- [Table 1 “Performance for DDR2–800” on Page 4](#)
- [Table 2 “Performance for DDR2–667” on Page 4](#)
- [Table 3 “Performance for DDR2–533C” on Page 4](#)
- [Table 4 “Performance for DDR2–400B” on Page 5](#)

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



Table 1 Performance for DDR2-800

Product Type Speed Code			-2.5F	-2.5	Unit
Speed Grade			DDR2-800D 5-5-5	DDR2-800E 6-6-6	—
max. Clock Frequency	@CL6	f_{CK6}	400	400	MHz
	@CL5	f_{CK5}	400	333	MHz
	@CL4	f_{CK4}	266	266	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	12.5	15	ns
min. Row Precharge Time		t_{RP}	12.5	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	57.5	60	ns

Table 2 Performance for DDR2-667

Product Type Speed Code			-3	-3S	Unit
Speed Grade			DDR2-667C 4-4-4	DDR2-667D 5-5-5	—
max. Clock Frequency	@CL5	f_{CK5}	333	333	MHz
	@CL4	f_{CK4}	333	266	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	12	15	ns
min. Row Precharge Time		t_{RP}	12	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	57	60	ns

Table 3 Performance for DDR2-533C

Product Type Speed Code			-3.7	Unit
Speed Grade			DDR2-533C 4-4-4	—
max. Clock Frequency	@CL5	f_{CK5}	266	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns



Table 4 Performance for DDR2-400B

Product Type Speed Code			-5	Units
Speed Grade			DDR2-400B 3-3-3	—
max. Clock Frequency	@CL5	f_{CK5}	200	MHz
	@CL4	f_{CK4}	200	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	40	ns
min. Row Cycle Time		t_{RC}	55	ns

1.2 Description

The 512-Mb DDR2 DRAM is a high-speed Double-Data-Rate-Two CMOS DRAM device containing 536,870,912 bits and internally configured as a quad-bank DRAM. The 512-Mb device is organized as either 32 Mbit \times 4 I/O \times 4 banks, 16 Mbit \times 8 I/O \times 4 banks or 8 Mbit \times 16 I/O \times 4 banks chip. These devices achieve high speed transfer rates starting at 400 Mb/sec/pin for general applications. See [Table 1](#) to [Table 4](#) for performance figures.

The device is designed to comply with all DDR2 DRAM key features:

1. Posted \overline{CAS} with additive latency,
2. Write latency = read latency - 1,
3. Normal and weak strength data-output driver,
4. Off-Chip Driver (OCD) impedance adjustment
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks.

Inputs are latched at the cross point of differential clocks (CK rising and \overline{CK} falling). All I/Os are synchronized with a single ended DQS or differential DQS-DQS pair in a source synchronous fashion.

A 16-bit address bus for $\times 4$ and $\times 8$ organized components and a 15-bit address bus for $\times 16$ components is used to convey row, column and bank address information in a $\overline{RAS-CAS}$ multiplexing style.

The DDR2 device operates with a 1.8 V \pm 0.1 V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in PG-TFBGA package.



Table 5 Ordering Information for RoHS compliant products

Product Type	Org.	Speed	CAS-RCD-RP Latencies ¹⁾²⁾³⁾	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Package
HYB18T512160BF-25F	×16	DDR2-800D	5-5-5	400	4-4-4	266	PG-TFBGA-84-8
HYB18T512800BF-25F	×8	DDR2-800D	5-5-5	400	4-4-4	266	PG-TFBGA-60-24
HYB18T512400BF-25F	×4	DDR2-800D	5-5-5	400	4-4-4	266	PG-TFBGA-60-24
HYB18T512160BF-2.5	×16	DDR2-800E	6-6-6	400	5-5-5	333	PG-TFBGA-84-8
HYB18T512800BF-2.5	×8	DDR2-800E	6-6-6	400	5-5-5	333	PG-TFBGA-60-24
HYB18T512400BF-2.5	×4	DDR2-800E	6-6-6	400	5-5-5	333	PG-TFBGA-60-24
HYB18T512160BF-3	×16	DDR2-667C	4-4-4	333	3-3-3	200	PG-TFBGA-84-8
HYB18T512400BF-3	×4	DDR2-667C	4-4-4	333	3-3-3	200	PG-TFBGA-60-24
HYB18T512800BF-3	×8	DDR2-667C	4-4-4	333	3-3-3	200	PG-TFBGA-60-24
HYB18T512160BF-3S	×16	DDR2-667D	5-5-5	333	4-4-4	266	PG-TFBGA-84-8
HYB18T512400BF-3S	×4	DDR2-667D	5-5-5	333	4-4-4	266	PG-TFBGA-60-24
HYB18T512800BF-3S	×8	DDR2-667D	5-5-5	333	4-4-4	266	PG-TFBGA-60-24
HYB18T512160BF-3.7	×16	DDR2-533C	4-4-4	266	3-3-3	200	PG-TFBGA-84-8
HYB18T512400BF-3.7	×4	DDR2-533C	4-4-4	266	3-3-3	200	PG-TFBGA-60-24
HYB18T512800BF-3.7	×8	DDR2-533C	4-4-4	266	3-3-3	200	PG-TFBGA-60-24
HYB18T512160BF-5	×16	DDR2-400B	3-3-3	200	—	—	PG-TFBGA-84-8
HYB18T512400BF-5	×4	DDR2-400B	3-3-3	200	—	—	PG-TFBGA-60-24
HYB18T512800BF-5	×8	DDR2-400B	3-3-3	200	—	—	PG-TFBGA-60-24

- 1) CAS: Column Address Strobe
- 2) RCD: Row Column Delay
- 3) RP: Row Precharge

Note: For product nomenclature see [Chapter 9](#) of this data sheet



2 Pin Configuration

2.1 Pin Configuration

The pin configuration of a DDR2 SDRAM is listed by function in [Table 6](#). The abbreviations used in the Pin# and Buffer Type columns are explained in [Table 7](#) and [Table 8](#) respectively. The pin numbering for the FBGA package is depicted in Figure 1 for $\times 4$, Figure 2 for $\times 8$ and Figure 3 for $\times 16$.

Table 6 Pin Configuration of DDR2 SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals $\times 4/\times 8$ organizations				
E8	CK	I	SSTL	Clock Signal CK, Complementary Clock Signal $\overline{\text{CK}}$
F8	$\overline{\text{CK}}$	I	SSTL	
F2	CKE	I	SSTL	Clock Enable
Clock Signals $\times 16$ organization				
J8	CK	I	SSTL	Clock Signal CK, Complementary Clock Signal $\overline{\text{CK}}$ <i>Note: See functional description in $\times 4/\times 8$ organization</i>
K8	$\overline{\text{CK}}$	I	SSTL	
K2	CKE	I	SSTL	Clock Enable <i>Note: See functional description in $\times 4/\times 8$ organization</i>
Control Signals $\times 4/\times 8$ organizations				
F7	$\overline{\text{RAS}}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
G7	$\overline{\text{CAS}}$	I	SSTL	
F3	$\overline{\text{WE}}$	I	SSTL	
G8	CS	I	SSTL	Chip Select
Control Signals $\times 16$ organization				
K7	$\overline{\text{RAS}}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
L7	$\overline{\text{CAS}}$	I	SSTL	
K3	$\overline{\text{WE}}$	I	SSTL	
L8	CS	I	SSTL	Chip Select
Address Signals $\times 4/\times 8$ organizations				
G2	BA0	I	SSTL	Bank Address Bus 1:0
G3	BA1	I	SSTL	



Table 6 Pin Configuration of DDR2 SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
H8	A0	I	SSTL	Address Signal 12:0, Address Signal 10/Autoprecharge
H3	A1	I	SSTL	
H7	A2	I	SSTL	
J2	A3	I	SSTL	
J8	A4	I	SSTL	
J3	A5	I	SSTL	
J7	A6	I	SSTL	
K2	A7	I	SSTL	
K8	A8	I	SSTL	
K3	A9	I	SSTL	
H2	A10	I	SSTL	
	AP	I	SSTL	
K7	A11	I	SSTL	
L2	A12	I	SSTL	
L8	A13	I	SSTL	Address Signal 13
				<i>Note: x4/x8 512 Mbit components</i>
	NC	–	–	<i>Note: and x16 512 Mbit components</i>
Address Signals ×16 organization				
L2	BA0	I	SSTL	Bank Address Bus 1:0
L3	BA1	I	SSTL	
L1	NC	–	–	
M8	A0	I	SSTL	Address Signal 12:0, Address Signal 10/Autoprecharge
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
Data Signals ×4 organizations				
C8	DQ0	I/O	SSTL	Data Signal 3:0
C2	DQ1	I/O	SSTL	
D7	DQ2	I/O	SSTL	
D3	DQ3	I/O	SSTL	



Table 6 Pin Configuration of DDR2 SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Data Signals ×8 organization				
C8	DQ0	I/O	SSTL	Data Signal 7:0
C2	DQ1	I/O	SSTL	
D7	DQ2	I/O	SSTL	
D3	DQ3	I/O	SSTL	
D1	DQ4	I/O	SSTL	
D9	DQ5	I/O	SSTL	
B1	DQ6	I/O	SSTL	
B9	DQ7	I/O	SSTL	
Data Signals ×16 organization				
G8	DQ0	I/O	SSTL	Data Signal 15:0
G2	DQ1	I/O	SSTL	
H7	DQ2	I/O	SSTL	
H3	DQ3	I/O	SSTL	
H1	DQ4	I/O	SSTL	
H9	DQ5	I/O	SSTL	
F1	DQ6	I/O	SSTL	
F9	DQ7	I/O	SSTL	
C8	DQ8	I/O	SSTL	
C2	DQ9	I/O	SSTL	
D7	DQ10	I/O	SSTL	
D3	DQ11	I/O	SSTL	
D1	DQ12	I/O	SSTL	
D9	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
B9	DQ15	I/O	SSTL	
Data Strobe ×4/×8 organisations				
B7	DQS	I/O	SSTL	Data Strobe
A8	$\overline{\text{DQS}}$	I/O	SSTL	
Data Strobe ×8 organisations				
B3	RDQS	O	SSTL	Read Data Strobe
A2	$\overline{\text{RDQS}}$	O	SSTL	
Data Strobe ×16 organization				
B7	UDQS	I/O	SSTL	Data Strobe Upper Byte
A8	$\overline{\text{UDQS}}$	I/O	SSTL	
F7	LDQS	I/O	SSTL	Data Strobe Lower Byte
E8	$\overline{\text{LDQS}}$	I/O	SSTL	
Data Mask ×4/×8 organizations				
B3	DM	I	SSTL	Data Mask
Data Mask ×16 organization				



Table 6 Pin Configuration of DDR2 SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
B3	UDM	I	SSTL	Data Mask Upper/Lower Byte
F3	LDM	I	SSTL	
Power Supplies ×4/×8/×16 organizations				
A9,C1,C3,C7, C9	V _{DDQ}	PWR	–	I/O Driver Power Supply
A1	V _{DD}	PWR	–	Power Supply
A7,B2,B8,D2, D8	V _{SSQ}	PWR	–	I/O Driver Power Supply
A3,E3	V _{SS}	PWR	–	Power Supply
Power Supplies ×4/×8 organizations				
E2	V _{REF}	AI	–	I/O Reference Voltage
E1	V _{DDL}	PWR	–	Power Supply
E9,H9,L1	V _{DD}	PWR	–	Power Supply
E7	V _{SSDL}	PWR	–	Power Supply
J1,K9	V _{SS}	PWR	–	Power Supply
Power Supplies ×16 organization				
J2	V _{REF}	AI	–	I/O Reference Voltage
E9, G1, G3, G7, G9	V _{DDQ}	PWR	–	I/O Driver Power Supply
J1	V _{DDL}	PWR	–	Power Supply
E1, J9, M9, R1	V _{DD}	PWR	–	Power Supply
E7, F2, F8, H2, H8	V _{SSQ}	PWR	–	I/O Driver Power Supply
J7	V _{SSDL}	PWR	–	Power Supply
J3,N1,P9	V _{SS}	PWR	–	Power Supply
Not Connected ×4 organizations				
A2, B1, B9, D1, D9, G1, L3,L7, L8	NC	NC	–	Not Connected
Not Connected ×8 organization				
G1, L3,L7, L8	NC	NC	–	Not Connected
Not Connected ×16 organization				
A2, E2, L1, R3, R7, R8	NC	NC	–	Not Connected
Other Pins ×4/×8 organizations				
F9	ODT	I	SSTL	On-Die Termination Control
Other Pins ×16 organization				
K9	ODT	I	SSTL	On-Die Termination Control



Table 7 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 8 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.



1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	\overline{DQS}	V_{DDQ}
NC	V_{SSQ}	DM		B		DQS	V_{SSQ}	NC
V_{DDQ}	DQ1	V_{DDQ}		C		V_{DDQ}	DQ0	V_{DDQ}
NC	V_{SSQ}	DQ3		D		DQ2	V_{SSQ}	NC
V_{DDL}	V_{REF}	V_{SS}		E		V_{SSDL}	CK	V_{DD}
	CKE	\overline{WE}		F		\overline{RAS}	\overline{CK}	ODT
NC	BA0	BA1		G		\overline{CAS}	\overline{CS}	
	A10/AP	A1		H		A2	A0	V_{DD}
V_{SS}	A3	A5		J		A6	A4	
	A7	A9		K		A11	A8	V_{SS}
V_{DD}	A12	NC		L		NC	NC,A13	

MPPT0020

Figure 1 Pin Configuration for $\times 4$ components, PG-TFBGA-60-24

Notes

1. V_{DDL} and V_{SSDL} are power and ground for the DLL. They are isolated on the device from V_{DD} , V_{DDQ} , V_{SS} , and V_{SSQ}

2. Ball position L8 is A13 for 512-Mbit and is Not Connected on 256-Mbit



1	2	3	4	5	6	7	8	9
V_{DD}	NC, \overline{RDQS}	V_{SS}		A		V_{SSQ}	\overline{DQS}	V_{DDQ}
DQ6	V_{SSQ}	DM/ \overline{RDQS}		B		DQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		C		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		D		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		E		V_{SSDL}	CK	V_{DD}
	CKE	WE		F		\overline{RAS}	\overline{CK}	ODT
NC	BA0	BA1		G		\overline{CAS}	\overline{CS}	
	A10/AP	A1		H		A2	A0	V_{DD}
V_{SS}	A3	A5		J		A6	A4	
	A7	A9		K		A11	A8	V_{SS}
V_{DD}	A12	NC		L		NC	NC,A13	

MPPT0090

Figure 2 Pin Configuration for ×8 components, PG-TFBGA-60-24

Notes

1. $\overline{RDQS} / \overline{RDQS}$ are enabled by EMRS(1) command.
2. If $\overline{RDQS} / \overline{RDQS}$ is enabled, the DM function is disabled
3. When enabled, \overline{RDQS} & \overline{RDQS} are used as strobe signals during reads.
4. V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{DD} , V_{DDQ} , V_{SSDL} , V_{SS} , and V_{SSQ} are isolated on the device.
5. Ball position L8 is A13 for 512-Mbit and is Not Connected on 256-Mbit.



1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	\overline{UDQS}	V_{DDQ}
DQ14	V_{SSQ}	UDM		B		UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}		C		V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11		D		DQ10	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}		E		V_{SSQ}	\overline{LDQS}	V_{DDQ}
DQ6	V_{SSQ}	LDM		F		LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		G		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		H		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		J		VSSDL	CK	V_{DD}
	CKE	\overline{WE}		K		\overline{RAS}	\overline{CK}	ODT
NC	BA0	BA1		L		\overline{CAS}	\overline{CS}	
	A10/AP	A1		M		A2	A0	V_{DD}
V_{SS}	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	V_{SS}
V_{DD}	A12	NC		R		NC	NC	

MPPT0120

Figure 3 Pin Configuration for $\times 16$ components, PG-TFBGA-84-8

Notes

1. $\overline{UDQS}/UDQS$ is data strobe for DQ[15:8],
 $\overline{LDQS}/LDQS$ is data strobe for DQ[7:0]

2. LDM is the data mask signal for DQ[7:0], UDM is the data mask signal for DQ[15:8]

3. V_{DDL} and V_{SSDL} are power and ground for the DLL.
 V_{DDL} is connected to V_{DD} on the device. V_{DD} , V_{DDQ} ,
 V_{SSDL} , V_{SS} , and V_{SSQ} are isolated on the device.



2.2 512 Mbit DDR2 Addressing

Table 9 512-Mbit DDR2 Addressing

Configuration	128Mb x 4 ¹⁾	64Mb x 8	32Mb x 16	Note
Bank Address	BA[1:0]	BA[1:0]	BA[1:0]	—
Number of Banks	4	4	4	—
Auto-Precharge	A10 / AP	A10 / AP	A10 / AP	—
Row Address	A[13:0]	A[13:0]	A[12:0]	—
Column Address	A11, A[9:0]	A[9:0]	A[9:0]	—
Number of Column Address Bits	11	10	10	2)
Number of I/Os	4	8	16	—
Page Size [Bytes]	1024 (1K)	1024 (1K)	2048(2K)	3)

1) Referred to as 'org'

2) Referred to as 'colbits'

3) PageSize = $2^{\text{colbits}} \times \text{org}/8$ [Bytes]



3 Functional Description

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	PD		WR		DLL	TM		CL		BT		BL	
eg. addr				w		w		w	w		w		w		w	

MPBT0410

Table 10 Mode Register Definition (BA[2:0] = 000B)

Field	Bits	Type ¹⁾	Description
BA2	16	reg. addr.	Bank Address [2] <i>Note: BA2 not available on 256 Mbit and 512 Mbit components</i> 0 _B BA2 , Bank Address
BA1	15		Bank Address [1] 0 _B BA1 , Bank Address
BA0	14		Bank Address [0] 0 _B BA0 , Bank Address
A13	13		Address Bus[13] <i>Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration</i> 0 _B A13 , Address bit 13
PD	12	w	Active Power-Down Mode Select 0 _B PD , Fast exit 1 _B PD , Slow exit
WR	[11:9]	w	Write Recovery²⁾ <i>Note: All other bit combinations are illegal.</i> 001 _B WR , 2 010 _B WR , 3 011 _B WR , 4 100 _B WR , 5 101 _B WR , 6
DLL	8	w	DLL Reset 0 _B DLL , No 1 _B DLL , Yes
TM	7	w	Test Mode 0 _B TM , Normal Mode 1 _B TM , Vendor specific test mode
CL	[6:4]	w	CAS Latency <i>Note: All other bit combinations are illegal.</i> 010 _B CL , 2 011 _B CL , 3 100 _B CL , 4 101 _B CL , 5 110 _B CL , 6



Table 10 Mode Register Definition (BA[2:0] = 000B)

Field	Bits	Type ¹⁾	Description
BT	3	w	Burst Type 0 _B BT, Sequential 1 _B BT, Interleaved
BL	[2:0]	w	Burst Length <i>Note: All other bit combinations are illegal.</i> 010 _B BL, 4 011 _B BL, 8

- 1) w = write only register bits
 2) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: $WR [cycles] \geq t_{WR} (ns) / t_{CK} (ns)$. The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing WR_{MIN} is determined by $t_{CK,MAX}$ and WR_{MAX} is determined by $t_{CK,MIN}$.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	Q _{ff}	RDQS	\overline{DQS}	OCD P og am			R _{tt}		AL		R _{tt}	DIC	DLL
eg. add					w	w	w	w		w		w		w	w	w

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Table 11 Extended Mode Register Definition (BA[2:0] = 001B)

Field	Bits	Type ¹⁾	Description
BA2	16	reg. addr.	Bank Address [2] <i>Note: BA2 not available on 256 Mbit and 512 Mbit components</i> 0 _B BA2, Bank Address
BA1	15		Bank Address [1] 0 _B BA1, Bank Address
BA0	14		Bank Address [0] 0 _B BA0, Bank Address



Table 11 Extended Mode Register Definition (BA[2:0] = 001B)

Field	Bits	Type ¹⁾	Description
A13	13	w	Address Bus[13] <i>Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration</i> 0 _B A13 , Address bit 13
Qoff	12		Output Disable 0 _B QOff , Output buffers enabled 1 _B QOff , Output buffers disabled
RDQS	11		Read Data Strobe Output (RDQS, RDQS) 0 _B RDQS , Disable 1 _B RDQS , Enable
DQS	10		Complement Data Strobe (DQS Output) 0 _B DQS , Enable 1 _B DQS , Disable
OCD Program	[9:7]		Off-Chip Driver Calibration Program 000 _B OCD , OCD calibration mode exit, maintain setting 001 _B OCD , Drive (1) 010 _B OCD , Drive (0) 100 _B OCD , Adjust mode 111 _B OCD , OCD calibration default
AL	[5:3]		Additive Latency <i>Note: All other bit combinations are illegal.</i> 000 _B AL , 0 001 _B AL , 1 010 _B AL , 2 011 _B AL , 3 100 _B AL , 4 101 _B AL , 5
R _{TT}	2,6		Nominal Termination Resistance of ODT 00 _B RTT , ∞ (ODT disabled) 01 _B RTT , 75 Ohm 10 _B RTT , 150 Ohm 11 _B RTT , 50 Ohm ²⁾
DIC	1		Off-chip Driver Impedance Control 0 _B DIC , Full (Driver Size = 100%) 1 _B DIC , Reduced
DLL	0		DLL Enable 0 _B DLL , Enable 1 _B DLL , Disable

1) w = write only register bits

2) optional for DDR2-400/533 & 667

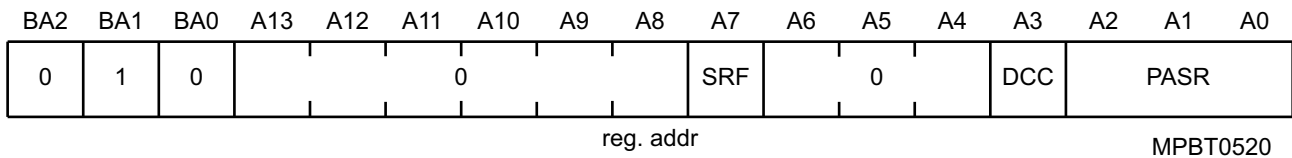
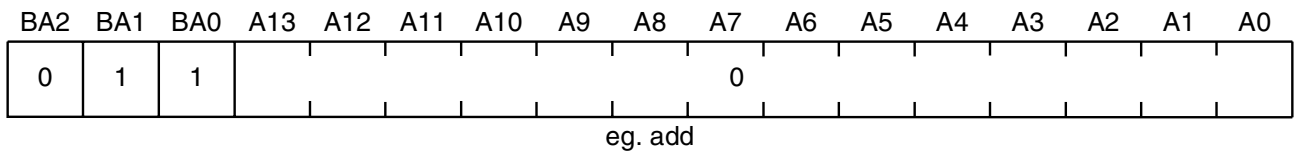


Table 12 EMRS(2) Programming Extended Mode register Definition (BA[2:0]=010_B)

Field	Bits	Type ¹⁾	Description
BA2	16	w	Bank Address[2] <i>Note: BA2 is not available on 256Mbit and 512Mbit components</i> 0 _B BA2 , Bank Address
BA	[15:14]	w	Bank Address[15:14] 00 _B BA , MRS 01 _B BA , EMRS(1) 10 _B BA , EMRS(2) 11 _B BA , EMRS(3): Reserved
A	[13:8]	w	Address Bus[13:8] <i>Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration</i> 0 _B A[13:8] , Address bits
A	7	w	Address Bus[7], adapted self refresh rate for TCase > 85°C 0 _B A7 , disable 1 _B A7 , enable ²⁾
A	[6:4]	w	Address Bus[6:4] 0 _B A[6:4] , Address bits
A	3	w	Address Bus[3], Duty Cycle Correction (DCC) 0 _B A[3] , DCC disabled 1 _B A[3] , DCC enabled
Partial Self Refresh for 4 banks			
A	[2:0]	w	Address Bus[2:0], Partial Array Self Refresh for 4 Banks³⁾ 000 _B PASR0 , Full Array 001 _B PASR1 , Half Array (BA[1:0]=00, 01) 010 _B PASR2 , Quarter Array (BA[1:0]=00) 011 _B PASR3 , Not defined 100 _B PASR4 , 3/4 array (BA[1:0]=01, 10, 11) 101 _B PASR5 , Half array (BA[1:0]=10, 11) 110 _B PASR6 , Quarter array (BA[1:0]=11) 111 _B PASR7 , Not defined

- 1) w = write only
- 2) When DRAM is operated at 85°C ≤ T_{Case} ≤ 95°C the extended self refresh rate must be enabled by setting bit A7 to "1" before the self refresh mode can be entered.
- 3) If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be lost if self refresh is entered. Data integrity will be maintained if t_{REF} conditions are met and no Self Refresh command is issued



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Table 13 EMR(3) Programming Extended Mode Register Definition (BA[2:0]=010_B)

Field	Bits	Type ¹⁾	Description
BA2	16	reg.addr	Bank Address[2] <i>Note: BA2 is not available on 256Mbit and 512Mbit components</i> 0 _B BA2 , Bank Address
BA1	15		Bank Address[1] 1 _B BA1 , Bank Address
BA0	14		Bank Address[0] 1 _B BA0 , Bank Address
A	[13:0]	w	Address Bus[13:0] <i>Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration</i> 0 _B A[13:0] , Address bits

1) w = write only



ODT Truth Tables

The ODT Truth Table shows which of the input pins are terminated depending on the state of address bit A10 and A11 in the EMRS(1) for all three device

organisations (×4, ×8 and ×16). To activate termination of any of these pins, the ODT function has to be enabled in the EMRS(1) by address bits A6 and A2.

Table 14 ODT Truth Table

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
x4 components		
DQ[3:0]	X	
DQS	X	
$\overline{\text{DQS}}$	0	X
DM	X	
x8 components		
DQ[7:0]	X	
DQS	X	
$\overline{\text{DQS}}$	0	X
RDQS	X	1
$\overline{\text{RDQS}}$	0	1
DM	X	0
x16 components		
DQ[7:0]	X	
DQ[15:8]	X	
LDQS	X	
$\overline{\text{LDQS}}$	0	X
UDQS	X	
$\overline{\text{UDQS}}$	0	X
LDM	X	
UDM	X	

Note: X = don't care; 0 = bit set to low; 1 = bit set to high



Table 15 Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Notes

1. Page Size and Length is a function of I/O organization:
128Mb x 4 organization (CA[9:0], CA11); Page Size = 1 KByte; Page Length = 2048
64Mb x 8 organization (CA[9:0]); Page Size = 1

KByte; Page Length = 1024

32Mb x 16 organization (CA[9:0]); Page Size = 2 KByte; Page Length = 1024

2. Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components



4 Truth Tables

Table 16 Command Truth Table

Function	CKE		CS	RAS	CAS	WE	BA0 BA1	A[13:11]	A10	A[9:0]	Note ¹⁾²⁾³⁾
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			4)5)
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	—
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	6)
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	7)
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	—
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	—
Bank Activate	H	H	L	L	H	H	BA	Row Address			—
Write	H	H	L	H	L	L	BA	Column	L	Column	8)
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	—
Read	H	H	L	H	L	H	BA	Column	L	Column	—
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	—
No Operation	H	X	L	H	H	H	X	X	X	X	—
Device Deselect	H	X	H	X	X	X	X	X	X	X	—
Power Down Entry	H	L	H	X	X	X	X	X	X	X	9)
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	—
			L	H	H	H					

- 1) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 2) "X" means "H or L (but a defined logic level)".
- 3) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) All DDR2 SDRAM commands are defined by states of \overline{CS} , \overline{WE} , \overline{RAS} , \overline{CAS} , and CKE at the rising edge of the clock.
- 5) Bank addresses BA[1:0] determine which bank is to be operated upon. For (E)MRS BA[1:0] selects an (Extended) Mode Register.
- 6) V_{REF} must be maintained during Self Refresh operation.
- 7) Self Refresh Exit is asynchronous.
- 8) Burst reads or writes at BL = 4 cannot be terminated.
- 9) The Power Down Mode does not perform any refresh operations.



Table 17 Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State ¹⁾	CKE		Command (N) ²⁾³⁾ RAS, CAS, WE, CS	Action (N)	Note ⁴⁾⁵⁾
	Previous Cycle ⁶⁾ (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	7)8)
	L	H	DESELECT or NOP	Power-Down Exit	9)10)11)
Self Refresh	L	L	X	Maintain Self Refresh	12)
	L	H	DESELECT or NOP	Self Refresh Exit	13)14)
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	15)
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	—
	H	L	AUTOREFRESH	Self Refresh Entry	16)
Any State other than listed above	H	H	Refer to the Command Truth Table		17)

- 1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
- 2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
- 3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 4) CKE must be maintained HIGH while the device is in OCD calibration mode.
- 5) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- 7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
- 8) "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).
- 9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
- 11) $t_{CKE,MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CKE} + t_{IH}$.
- 12) V_{REF} must be maintained during Self Refresh operation.
- 13) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
- 14) Valid commands for Self Refresh Exit are NOP and DESELCT only.
- 15) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress.
- 16) Self Refresh mode can only be entered from the All Banks Idle state.
- 17) Must be a legal command as defined in the Command Truth Table.

Table 18 Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	—

- 1) Used to mask write data; provided coincident with the corresponding data.



5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 19 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0 to +2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5 to +2.3	V	—
V_{DDL}	Voltage on VDDL pin relative to V_{SS}	-0.5 to +2.3	V	—
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5 to +2.3	V	—
T_{STG}	Storage Temperature	-55 to +100	°C	2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV; Vref may be equal to or less than 300mV.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 20 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Operating Temperature	0 to 95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.

2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.

3) Above 85 °C case temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$.

4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%



5.2 DC Characteristics

Table 21 Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	—
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	—
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4)

- 1) V_{DDQ} tracks with V_{DD} , V_{DDDL} tracks with V_{DD} . AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDDL} tied together.
- 2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
- 3) Peak to peak ac noise on V_{REF} may not exceed $\pm 2\% V_{REF}$ (dc)
- 4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in die dc level of V_{REF} .

Table 22 ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2] =[1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	—
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	—
Deviation of V_M with respect to $V_{DDQ} / 2$	delta V_M	-6.00	—	+ 6.00	%	2)

- 1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IH(ac)})$ and $I(V_{IL(ac)})$ respectively. $Rtt(eff) = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IH(ac)}) - I(V_{IL(ac)}))$.
- 2) Measurement Definition for V_M : Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: $delta V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$

Table 23 Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current; any input $0 V < V_{IN} < V_{DD}$	-2	+2	μA	1)
I_{OL}	Output Leakage Current; $0 V < V_{OUT} < V_{DDQ}$	-5	+5	μA	2)

- 1) All other pins not under test = 0 V
- 2) DQ's, LDQS, \overline{LDQS} , UDQS, \overline{UDQS} , DQS, \overline{DQS} , RDQS, \overline{RDQS} are disabled and ODT is turned off



5.3 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) “Enable \overline{DQS} ” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured

relative to the rising or falling edges of DQS crossing at V_{REF} . In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, \overline{DQS} . This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the \overline{DQS} (and \overline{RDQS}) signals are internally disabled and don't care.

Table 24 DC & AC Logic Input Levels for DDR2-667 and DDR2-800

Symbol	Parameter	DDR2-667, DDR2-800		Units
		Min.	Max.	
$V_{IH(dc)}$	DC input logic high	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V
$V_{IL(dc)}$	DC input low	-0.3	$V_{REF} - 0.125$	V
$V_{IH(ac)}$	AC input logic high	$V_{REF} + 0.200$	—	V
$V_{IL(ac)}$	AC input low	—	$V_{REF} - 0.200$	V

Table 25 DC & AC Logic Input Levels for DDR2-533 and DDR2-400

Symbol	Parameter	DDR2-533, DDR2-400		Units
		Min.	Max.	
$V_{IH(dc)}$	DC input logic high	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V
$V_{IL(dc)}$	DC input low	-0.3	$V_{REF} - 0.125$	V
$V_{IH(ac)}$	AC input logic high	$V_{REF} + 0.250$	—	V
$V_{IL(ac)}$	AC input low	—	$V_{REF} - 0.250$	V

Table 26 Single-ended AC Input Test Conditions

Symbol	Condition	Value	Unit	Note
V_{REF}	Input reference voltage	$0.5 \times V_{DDQ}$	V	1)
$V_{SWING.MAX}$	Input signal maximum peak to peak swing	1.0	V	—
SLEW	Input signal minimum Slew Rate	1.0	V / ns	2)3)

- 1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
- 2) The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac).MIN}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac).MAX}$ for falling edges as shown in [Figure 4](#)
- 3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

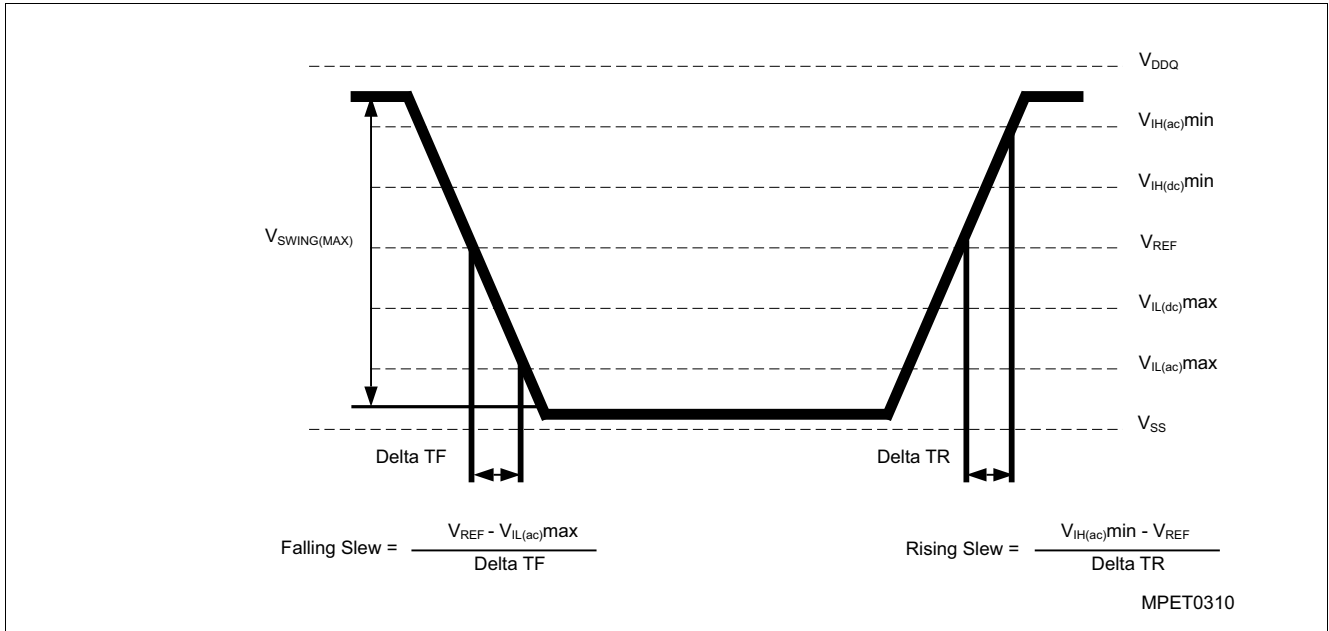


Figure 4 Single-ended AC Input Test Conditions Diagram

Table 27 Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{IN(dc)}$	DC input signal voltage	-0.3	$V_{DDQ} + 0.3$	—	1)
$V_{ID(dc)}$	DC differential input voltage	0.25	$V_{DDQ} + 0.6$	—	2)
$V_{ID(ac)}$	AC differential input voltage	0.5	$V_{DDQ} + 0.6$	V	3)
$V_{IX(ac)}$	AC differential cross point input voltage	$0.5 \times V_{DDQ} - 0.175$	$0.5 \times V_{DDQ} + 0.175$	V	4)
$V_{OX(ac)}$	AC differential cross point output voltage	$0.5 \times V_{DDQ} - 0.125$	$0.5 \times V_{DDQ} + 0.125$	V	5)

- 1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, \overline{CK} , DQS, \overline{DQS} etc.
- 2) $V_{ID(dc)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.
- 3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.
- 4) The value of $V_{IX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ} . $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
- 5) The value of $V_{OX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ} . $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

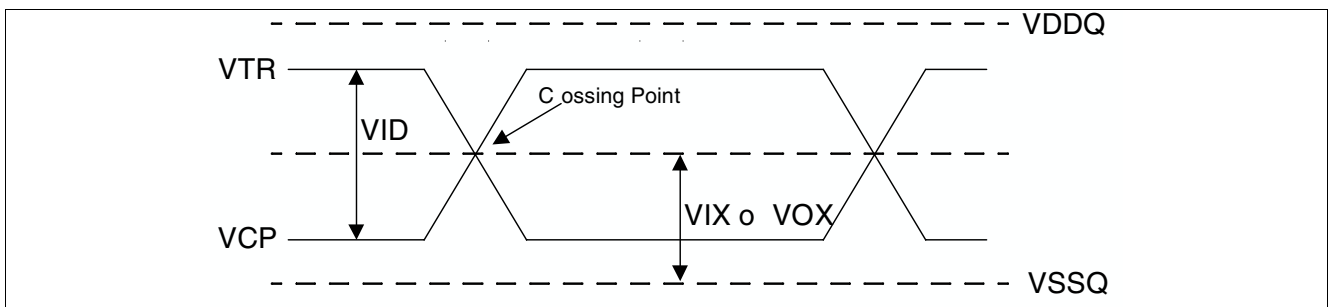


Figure 5 Differential DC and AC Input and Output Logic Levels Diagram



5.4 Output Buffer Characteristics

Table 28 SSTL_18 Output DC Current Drive

Symbol	Parameter	SSTL_18	Unit	Note
I_{OH}	Output Minimum Source DC Current	-13.4	mA	1)2)
I_{OL}	Output Minimum Sink DC Current	13.4	mA	3)

- 1) $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 1.42\text{ V}$. $(V_{OUT} - V_{DDQ}) / I_{OH}$ must be less than 21 Ohm for values of V_{OUT} between V_{DDQ} and $V_{DDQ} - 280\text{ mV}$.
- 2) The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in and . They are used to test drive current capability to ensure $V_{IH,MIN}$ plus a noise margin and $V_{IL,MAX}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 Ohm load line to define a convenient current for measurement.
- 3) $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 280\text{ mV}$. V_{OUT} / I_{OL} must be less than 21 Ohm for values of V_{OUT} between 0 V and 280 mV.

Table 29 SSTL_18 Output AC Test Conditions

Symbol	Parameter	SSTL_18	Unit	Note
V_{OH}	Minimum Required Output Pull-up	$V_{TT} + 0.603$	V	1)
V_{OL}	Maximum Required Output Pull-down	$V_{TT} - 0.603$	V	—
V_{OTR}	Output Timing Measurement Reference Level	$0.5 \times V_{DDQ}$	V	—

- 1) SSTL_18 test load for V_{OH} and V_{OL} is different from the referenced load. The SSTL_18 test load has a 20 Ohm series resistor additionally to the 25 Ohm termination resistor into V_{TT} . The SSTL_18 definition assumes that $\pm 335\text{ mV}$ must be developed across the effectively 25 Ohm termination resistor ($13.4\text{ mA} \times 25\text{ Ohm} = 335\text{ mV}$). With an additional series resistor of 20 Ohm this translates into a minimum requirement of 603 mV swing relative to V_{TT} , at the output device ($13.4\text{ mA} \times 45\text{ Ohm} = 603\text{ mV}$).

Table 30 OCD Default Characteristics

Symbol	Description	Min.	Nominal	Max.	Unit	Note
—	Output Impedance	—	—	—	Ohms	1)2)
—	Pull-up / Pull down mismatch	0	—	4	Ohms	3)
—	Output Impedance step size for OCD calibration	0	—	1.5	Ohms	4)
S_{OUT}	Output Slew Rate	1.5	—	5.0	V / ns	5)6)7)

- 1) $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$; $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$
- 2) Impedance measurement condition for output source dc current: $V_{DDQ} = 1.7\text{ V}$, $V_{OUT} = 1420\text{ mV}$; $(V_{OUT} - V_{DDQ}) / I_{OH}$ must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and $V_{DDQ} - 280\text{ mV}$. Impedance measurement condition for output sink dc current: $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = -280\text{ mV}$; V_{OUT} / I_{OL} must be less than 23.4 Ohms for values of V_{OUT} between 0 V and 280 mV.
- 3) Mismatch is absolute value between pull-up and pull-down, both measured at same temperature and voltage.
- 4) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is $18 \pm 0.75\text{ Ohms}$ under nominal conditions.
- 5) The absolute value of the Slew Rate as measured from DC to DC is equal to or greater than the Slew Rate as measured from AC to AC. This is verified by design and characterization but not subject to production test.
- 6) Timing skew due to DRAM output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ's is included in t_{DQSQ} and t_{QHS} specification.
- 7) DRAM output Slew Rate specification applies to 400, 533 and 667 MT/s speed bins.



5.5 Input / Output Capacitance

Table 31 Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Unit
CCK	Input capacitance, CK and \overline{CK}	1.0	2.0	pF
CDCK	Input capacitance delta, CK and \overline{CK}	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS}	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS}	—	0.5	pF



5.6 Overshoot and Undershoot Specification

Table 32 AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above V_{DD}	1.33	1.00	0.80	0.80	V.ns
Maximum undershoot area below V_{SS}	1.33	1.00	0.80	0.80	V.ns

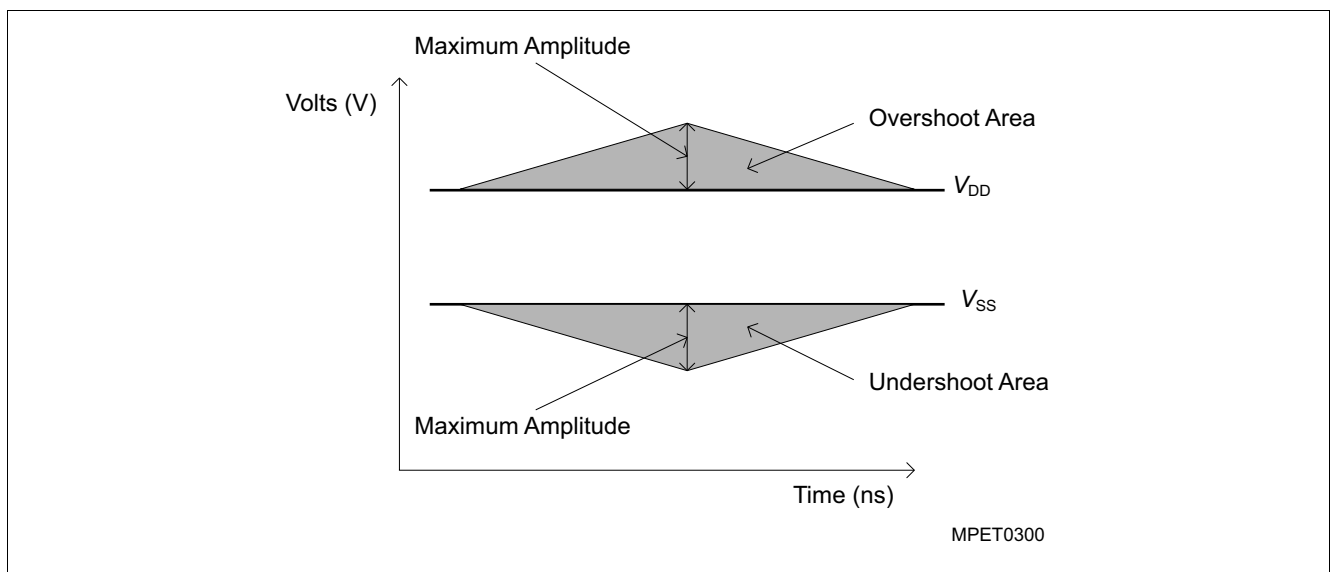


Figure 6 AC Overshoot / Undershoot Diagram for Address and Control Pins

Table 33 AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above V_{DDQ}	0.38	0.28	0.23	0.23	V.ns
Maximum undershoot area below V_{SSQ}	0.38	0.28	0.23	0.23	V.ns

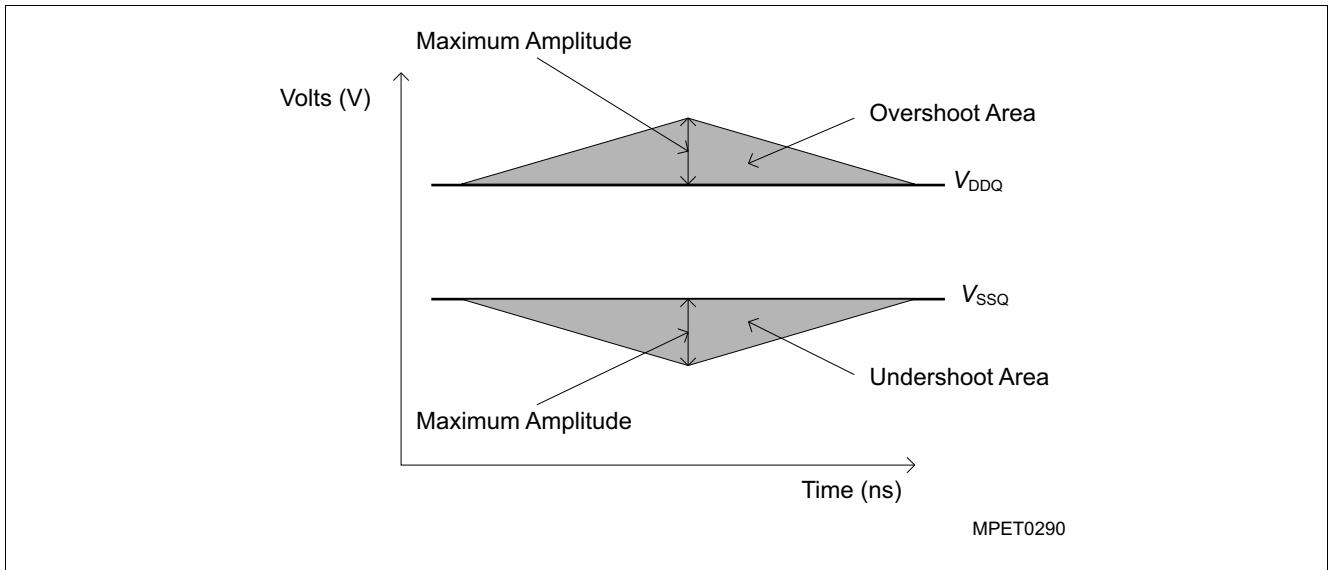


Figure 7 AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins



6 Specifications and Conditions

Table 34 I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD0}	1)2)3)4) 5)6)
Operating Current - One bank Active - Read - Precharge $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, AL = 0, CL = CL(IDD); CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD1}	
Precharge Power-Down Current All banks idle; CKE is LOW; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable; Data bus inputs are floating.	I_{DD2P}	
Precharge Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching.	I_{DD2N}	
Precharge Quiet Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating.	I_{DD2Q}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to "0" (Fast Power-down Exit).	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to 1 (Slow Power-down Exit);	$I_{DD3P(1)}$	
Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD3N}	
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL(IDD); $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching; $I_{OUT} = 0$ mA.	I_{DD4R}	
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL(IDD); $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, CKE is HIGH, \overline{CS} is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5B}	
Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{REFI} = 7.8$ μ s interval, CKE is LOW and \overline{CS} is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5D}	



Table 34 I_{DD} Measurement Conditions

Parameter	Symbol	Note
Self-Refresh Current CKE \leq 0.2 V; external clock off, CK and \overline{CK} at 0 V; Other control and address inputs are floating, Data bus inputs are floating.	I_{DD6}	
Operating Bank Interleave Read Current 1. All banks interleaving reads, $I_{OUT} = 0$ mA; BL = 4, CL = $CL_{(IDD)}$, AL = $t_{RCD(IDD)} - 1 \times t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching. 2. Timing pattern:	I_{DD7}	7)
DDR2-400-333: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D (11 clocks)		
DDR2-533-333: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D (15 clocks)		
DDR2-667-444: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D (19 clocks)		
DDR2-667-555: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D (20 clocks)		
DDR2-800-555: A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D (22 clocks)		
DDR2-800-666: A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D (23 clocks)		

- 1) $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$
- 2) I_{DD} specifications are tested after the device is properly initialized.
- 3) I_{DD} parameter are specified with ODT disabled.
- 4) Data Bus consists of DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS} , LDQS, \overline{LDQS} , UDQS and \overline{UDQS} .
- 5) Definitions for I_{DD} : see [Table 35](#)
- 6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in chapter 7..
- 7) A = Activate, RA = Read with Auto-Precharge, D=DESELECT

Table 35 Definition for I_{DD}

Parameter	Description
LOW	defined as $V_{IN} \leq V_{IL(ac).MAX}$
HIGH	defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	defined as inputs are stable at a HIGH or LOW level
FLOATING	defined as inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or strobes



Table 36 I_{DD} Specification for HYB18T512xxxBF

Symbol	-2.5F	-2.5	-3	-3S	-3.7	-5	Unit	Note
	DDR2-800D	DDR2-800E	DDR2-667C	DDR2-667D	DDR2-533C	DDR2-400B		
	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	84	80	75	71	65	61	mA	×4/×8
	105	100	95	90	80	75	mA	×16
I_{DD1}	100	95	90	85	75	70	mA	×4/×8
	120	115	105	100	90	83	mA	×16
I_{DD2P}	7	7	7	7	7	7	mA	—
I_{DD2N}	51	51	45	45	38	34	mA	—
I_{DD2Q}	45	45	40	40	35	32	mA	—
I_{DD3P}	39	39	33	33	28	24	mA	1)
	9	9	9	9	9	9	mA	2)
I_{DD3N}	60	60	50	50	43	39	mA	—
I_{DD4R}	155	155	130	130	110	95	mA	×4/×8
	180	180	155	155	130	115	mA	×16
I_{DD4W}	155	155	130	130	110	95	mA	×4/×8
	200	200	170	170	145	130	mA	×16
I_{DD5B}	145	145	140	140	130	125	mA	—
I_{DD5D}	9	9	9	9	9	9	mA	3)
I_{DD6}	7	7	7	7	7	7	mA	—
I_{DD7}	170	160	160	152	145	141	mA	×4/×8
	265	255	252	240	230	220	mA	×16

1) MRS(12)=0

2) MRS(12)=1

3) $0^{\circ} \leq T_{CASE} \leq 85^{\circ}C$.



7 Timing Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

7.1 Speed Grade Definitions

All Speed grades faster than DDR2-DDR400B comply with DDR2-DDR400B timing specifications ($t_{CK} = 5\text{ns}$ with $t_{RAS} = 40\text{ns}$).

List of Speed Grade Definition tables:

- [Table 37 “Speed Grade Definition Speed Bins DDR2–800” on Page 36](#)
- [Table 38 “Speed Grade Definition Speed Bins for DDR2–667” on Page 37](#)
- [Table 39 “Speed Grade Definition Speed Bins for DDR2–533C” on Page 37](#)
- [Table 40 “Speed Grade Definition Speed Bins for DDR2–400B” on Page 38](#)

Table 37 Speed Grade Definition Speed Bins DDR2–800

Speed Grade			DDR2–800D		DDR2–800E		Unit	Note
IFX Sort Name			–2.5F		–2.5			
CAS-RCD-RP latencies			5–5–5		6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	—
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	—
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	—
Row Active Time		t_{RAS}	45	70000	45	70000	ns	5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	—
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	—
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	—

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS / \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.



Table 38 Speed Grade Definition Speed Bins for DDR2-667

Speed Grade		DDR2-667		DDR2-667		Unit	Note	
IFX Sort Name		-3		-3S				
CAS-RCD-RP latencies		4-4-4		5-5-5		t_{CK}		
Parameter	Symbol	Min.	Max.	Min.	Max.	—		
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	ns	—
	@ CL = 5	t_{CK}	3	8	3	8	ns	—
Row Active Time	t_{RAS}	45	70000	45	70000	ns	5)	
Row Cycle Time	t_{RC}	57	—	60	—	ns	—	
RAS-CAS-Delay	t_{RCD}	12	—	15	—	ns	—	
Row Precharge Time	t_{RP}	12	—	15	—	ns	—	

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS/ \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.

Table 39 Speed Grade Definition Speed Bins for DDR2-533C

Speed Grade		DDR2-533		Unit	Note	
IFX Sort Name		-3.7				
CAS-RCD-RP latencies		4-4-4		t_{CK}		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	—
	@ CL = 5	t_{CK}	3.75	8	ns	—
Row Active Time	t_{RAS}	45	70000	ns	5)	
Row Cycle Time	t_{RC}	60	—	ns	—	
RAS-CAS-Delay	t_{RCD}	15	—	ns	—	
Row Precharge Time	t_{RP}	15	—	ns	—	

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS / \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.



Table 40 Speed Grade Definition Speed Bins for DDR2-400B

Speed Grade		DDR2-400		Unit	Note	
IFX Sort Name		-5				
CAS-RCD-RP latencies		3-3-3		t_{CK}		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	—
	@ CL = 5	t_{CK}	5	8	ns	—
Row Active Time	t_{RAS}	40	70000	ns	5)	
Row Cycle Time	t_{RC}	55	—	ns	—	
RAS-CAS-Delay	t_{RCD}	15	—	ns	—	
Row Precharge Time	t_{RP}	15	—	ns	—	

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS/ \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.



7.2 AC Timing Parameters

List of Timing Parameters Tables.

- [Table 41 “Timing Parameter by Speed Grade - DDR2-800” on Page 39](#)
- [Table 42 “Timing Parameter by Speed Grade - DDR2-667” on Page 41](#)
- [Table 43 “Timing Parameter by Speed Grade - DDR2-533” on Page 44](#)
- [Table 44 “Timing Parameter by Speed Grade - DDR2-400” on Page 47](#)

Table 41 Timing Parameter by Speed Grade - DDR2-800

Parameter	Symbol	DDR2-800		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	-400	+400	ps	—
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	7)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	125	—	ps	—
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	—	—	ps	—
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}	-350	+350	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	200	ps	9)
Write command to 1st DQS latching transition	t_{DQSS}	-0.25	+0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	50	—	ps	—
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	—	—	ps	—
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. (t_{CL} , t_{CH})		—	10)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC.MAX}$	ps	11)
Address and control input hold time	$t_{IH}(\text{base})$	250	—	ps	—
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—



Table 41 Timing Parameter by Speed Grade - DDR2-800 (cont'd)

Parameter	Symbol	DDR2-800		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
Address and control input setup time	$t_{IS}(\text{base})$	175	—	ps	—
DQ low-impedance time from CK / \overline{CK}	$t_{LZ}(\text{DQ})$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	—
DQS low-impedance from CK / \overline{CK}	$t_{LZ}(\text{DQS})$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	—
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	—	—
Data hold skew factor	t_{QHS}	—	300	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	μs	12)13)
		—	3.9	μs	14)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	15)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	—
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	—
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	17)
		10	—	ns	—
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	$0.35 \times t_{CK}$	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	19)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	t_{CK}	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

- 1) $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$. See notes
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = $0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} .



- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 10) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 11) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 12) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 13) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 14) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 15) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 16) $t_{RP(A)}$ for a Precharge-All command for an 8 bank device is equal to $t_{RP} + 1t_{CK}$, where t_{RP} are the values for a single bank precharge.
- 17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See [Chapter 1](#)
- 18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 19) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 = "1") a slow power-down exit timing t_{XARDS} has to be satisfied.

Table 42 Timing Parameter by Speed Grade - DDR2-667

Parameter	Symbol	DDR2-667		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
DQ output access time from CK / \overline{CK}	t_{AC}	-450	+450	ps	—
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	—
CK, \overline{CK} high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, \overline{CK} low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	$WR + t_{RP}$	—	t_{CK}	7)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	175	—	ps	—
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	—	—	ps	—
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / \overline{CK}	t_{DQSCK}	-400	+400	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—



Table 42 Timing Parameter by Speed Grade - DDR2-667 (cont'd)

Parameter	Symbol	DDR2-667		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	240	ps	9)
Write command to 1st DQS latching transition	t_{DQSS}	- 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	ps	—
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	—	—	ps	—
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. (t_{CL} , t_{CH})		—	10)
Data-out high-impedance time from CK / \overline{CK}	t_{HZ}	—	$t_{AC.MAX}$	ps	11)
Address and control input hold time	$t_{IH}(\text{base})$	275	—	ps	—
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	$t_{IS}(\text{base})$	200	—	ps	—
DQ low-impedance time from CK / \overline{CK}	$t_{LZ}(\text{DQ})$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	—
DQS low-impedance from CK / \overline{CK}	$t_{LZ}(\text{DQS})$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	—
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HPQ} - t_{QHS}$	—	—	—
Data hold skew factor	t_{QHS}	—	340	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	μs	12)13)
		—	3.9	μs	14)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	15)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	—
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	—
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	17)
		10	—	ns	—
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	$0.35 \times t_{CK}$	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	19)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)



Table 42 Timing Parameter by Speed Grade - DDR2-667 (cont'd)

Parameter	Symbol	DDR2-667		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	t_{CK}	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

- 1) $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$. See notes
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} .
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 10) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 11) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 12) The Auto-Refresh command interval has been reduced to 3.9 μs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 13) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 14) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 15) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 16) $t_{RP(A)}$ for a Precharge-All command for an 8 bank device is equal to $t_{RP} + 1t_{CK}$, where t_{RP} are the values for a single bank precharge.
- 17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See [Chapter 1](#)
- 18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 19) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing t_{XARDS} has to be satisfied.



Table 43 Timing Parameter by Speed Grade - DDR2-533

Parameter	Symbol	DDR2-533		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	-500	+500	ps	—
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	7)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	ps	—
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	—
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSK}	-450	+450	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	9)
Write command to 1st DQS latching transition	t_{DQSS}	- 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	ps	—
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	—
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		—	10)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC,MAX}$	ps	11)
Address and control input hold time	$t_{IH}(\text{base})$	375	—	ps	—
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	$t_{IS}(\text{base})$	250	—	ps	—
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQ})$	$2 \times t_{AC,MIN}$	$t_{AC,MAX}$	ps	—
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQS})$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	—
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	—	—



Table 43 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2-533		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	400	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	μ s	12)13)
		—	3.9	μ s	14)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	15)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	—
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	—
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	17)
		10	—	ns	—
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	$0.25 \times t_{CK}$	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	19)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

- 1) $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$. See notes
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} .
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 10) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).



- 11) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 12) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 13) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 14) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 15) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 16) $t_{RP(A)}$ for a Precharge-All command for an 8 bank device is equal to $t_{RP} + 1t_{CK}$, where t_{RP} are the values for a single bank precharge.
- 17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See [Chapter 1](#)
- 18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 19) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 = "1") a slow power-down exit timing t_{XARDS} has to be satisfied.



Table 44 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	-600	+600	ps	—
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	7)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	275	—	ps	—
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	—
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}	-500	+500	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	9)
Write command to 1st DQS latching transition	t_{DQSS}	- 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	150	—	ps	—
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	—
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		—	10)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC,MAX}$	ps	11)
Address and control input hold time	$t_{IH}(\text{base})$	475	—	ps	—
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	$t_{IS}(\text{base})$	350	—	ps	—
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQ})$	$2 \times t_{AC,MIN}$	$t_{AC,MAX}$	ps	—
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ}(\text{DQS})$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	—
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	—	—



Table 44 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	450	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	μ s	12)13)
		—	3.9	μ s	14)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	15)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	—
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	—
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	17)
		10	—	ns	—
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	$0.25 \times t_{CK}$	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	19)
Internal Write to Read command delay	t_{WTR}	10	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

- 1) $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$. See notes
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS/ \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} .
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 10) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).



- 11) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 12) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 13) $0\text{ }^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85\text{ }^{\circ}\text{C}$
- 14) $85\text{ }^{\circ}\text{C} < T_{\text{CASE}} \leq 95\text{ }^{\circ}\text{C}$
- 15) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 16) $t_{RP(A)}$ for a Precharge-All command for an 8 bank device is equal to $t_{RP} + 1t_{CK}$, where t_{RP} are the values for a single bank precharge.
- 17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See [Chapter 1](#)
- 18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 19) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{\text{MIN}}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 = "1") a slow power-down exit timing t_{XARDS} has to be satisfied.



7.3 ODT AC Electrical Characteristics

Table 45 ODT AC Electrical Characteristics and Operating Conditions for DDR2-667

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	—
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 0.7 \text{ ns}$	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	—
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	—
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	—
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	—
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	—

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .

Table 46 ODT AC Electrical Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	—
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	—
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	—
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	—
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	—
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	—

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .

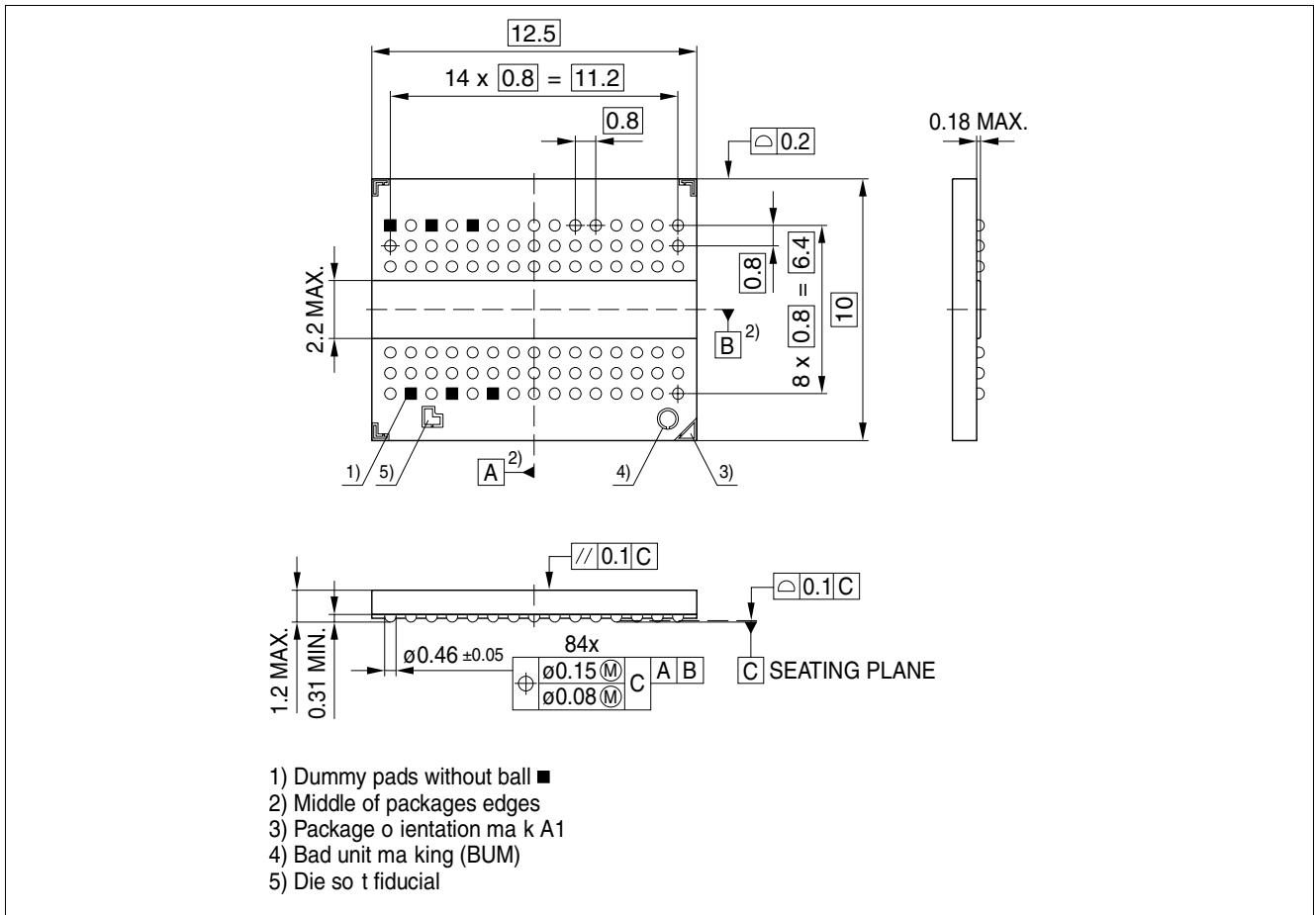


Figure 9 Package Outline P-TFBGA-84



9 Product Nomenclature

For reference the Qimonda SDRAM component nomenclature is enclosed in this chapter.

Table 47 Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
DDR2 DRAM	HYB	18	T	512	16		0	A	C	-3.7	

Table 48 DDR2 Memory Components

Field	Description	Values	Coding
1	QIMONDA Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 M
		512	512 M
		1G	1 Gb
5+6	Number of I/Os	40	×4
		80	×8
		160	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	-3	DDR2-667 4-4-4
		-3S	DDR2-667 5-5-5
		-3.7	DDR2-533 4-4-4
		-5	DDR2-400 3-3-3
11	N/A for Components		



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