National Semiconductor Corporation

PRELIMINARY

DP83BC04 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

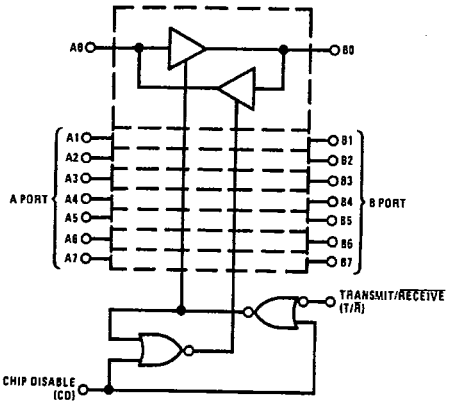
General Description

The DP83BC04 is a Bipolar-CMOS 8-bit TRI-STATE bidirectional transceiver (non-inverting), designed to provide bidirectional drive for bus oriented microprocessor and digital communication systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP transistors are used for low input currents and an increased output high (V_{OH}) level allows compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capability. In addition it features glitch free power up/down on the B port, preventing erroneous glitches on the system bus.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- 5 mA maximum ICC in TRI-STATE mode
- 40 mA maximum ICC in active mode
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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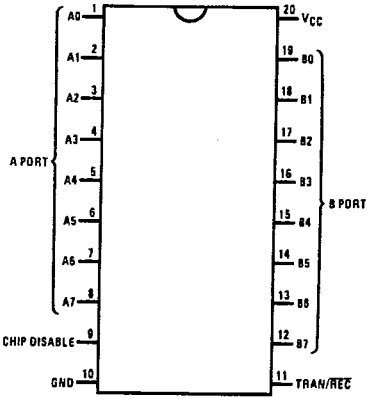
Dual-In-Line Package



Top View

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Order Number DP83BC04BJ or DP83BC04BN
See NS Package Number J20A or N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 seconds)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max
Supply Voltage (V_{CC})		
DP83BC04	4.75	5.25
Temperature (T_A)		
DP83BC04	0	70

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP83BC04			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max. (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP83BC04			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP83BC04			0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = Max			5		mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = Max			40		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DP83BC04B and across the 0°C to +70°C range for the DP73BC04B. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min or absolute value basis.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A Port Data/Mode Specification (*Figure A*)						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 0, S5 = 2		8.5		ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 0, S2 = X, S3 = 0, S4 = 0, S5 = 2		10		ns
t_{PCDLZA}	Propagation Delay from "0" to TRI-STATE from CD to A Port	B0–B7 = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 1, S4 = 0, S5 = 0		15.5		ns
t_{PCDHZA}	Propagation Delay from "1" to TRI-STATE from CD to A Port	B0–B7 = 2.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 0, S5 = 1		14		ns
t_{PCDZLA}	Propagation Delay from TRI-STATE to "0" from CD to A Port	B0–B7 = 0.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 1, S4 = 0, S5 = 0		26		ns
t_{PCDZHA}	Propagation Delay from TRI-STATE to "1" from CD to A Port	B0–B7 = 2.4V, T/$\overline{R}$ = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 1, S4 = 0, S5 = 1		32		ns
t_{PTRLZA}	Propagation Delay from "0" to TRI-STATE from T/$\overline{R}$ to A Port	B0–B7 = 0.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 0, S4 = 1, S5 = 0		16.5		ns
t_{PTRHZA}	Propagation Delay from "1" to TRI-STATE from T/$\overline{R}$ to A Port	B0–B7 = 2.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 0, S4 = 1, S5 = 1		15		ns
t_{PTRZLA}	Propagation Delay from TRI-STATE to "0" from T/$\overline{R}$ to A Port	B0–B7 = 0.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 1, S3 = 0, S4 = 1, S5 = 0		27		ns
t_{TPRZHA}	Propagation Delay from TRI-STATE to "1" from T/$\overline{R}$ to A Port	B0–B7 = 2.4V, CD = 0.4V, R1 = 1k, C1 = 50 pF S1 = 1, S2 = 0, S3 = 0, S4 = 1, S5 = 1		33		ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATION (*FIGURE B*)						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V T/$\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 0, S9 = 2		11		ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4, T/$\overline{R}$ = 2.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 0, S9 = 2		18.5		ns
t_{PCDLZB}	Propagation Delay from "0" to TRI-STATE from CD to B Port	A0–A7 = 0.4V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 1, S9 = 0		15.5		ns
t_{PCDHZB}	Propagation Delay from "1" to TRI-STATE from CD to B Port	A0–A7 = 2.4V; T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1, S9 = 1		13.5		ns
t_{PCDZLB}	Propagation Delay from TRI-STATE "0" from CD to B Port	A0–A7 = 0.4V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 1, S8 = 1, S9 = 0		25		ns
t_{PCDZHB}	Propagation Delay from TRI-STATE to "1" from CD to B Port	A0–A7 = 2.5V, T/$\overline{R}$ = 2.5V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 1, S8 = 1, S9 = 1		36		ns
t_{PTRLZB}	Propagation Delay from "0" to TRI-STATE from T/$\overline{R}$ to B Port	A0–A7 = 0.4V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 0, S8 = 0, S9 = 0		22		ns
t_{PTRHZB}	Propagation Delay from "1" to TRI-STATE from T/$\overline{R}$ to B Port	A0–A7 = 2.5V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 0, S9 = 1		23		ns
t_{PTRZLB}	Propagation Delay from TRI-STATE to "0" from T/$\overline{R}$ to B Port	A0–A7 = 0.4V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 1, S7 = 0, S8 = 0, S9 = 0		48		ns
t_{PTRZHB}	Propagation Delay from TRI-STATE to "1" from T/$\overline{R}$ to B Port	A0–A7 = 2.5V, CD = 0.4V, R2 = 150Ω, R3 = 100Ω, C2 = 300 pF, S6 = 0, S7 = 0, S8 = 0, S9 = 1		53		ns

Test Circuit

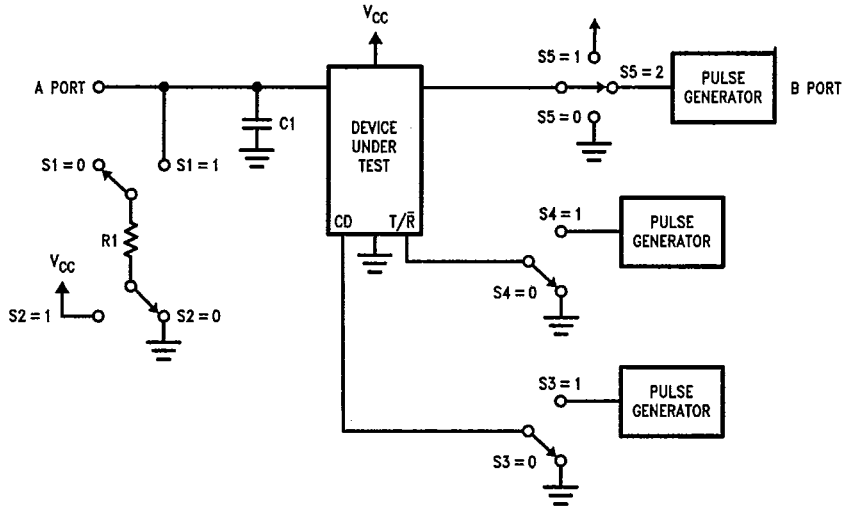

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FIGURE A. A Port Test Load

Test Circuit (Continued)

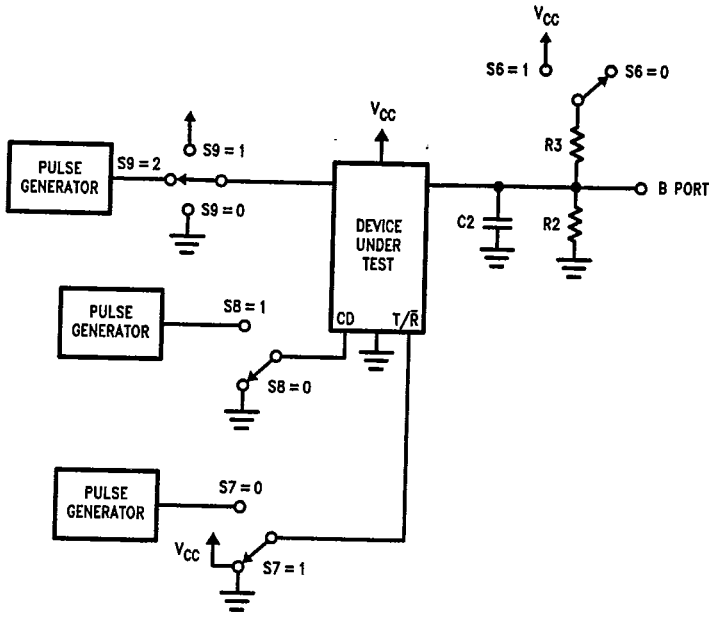

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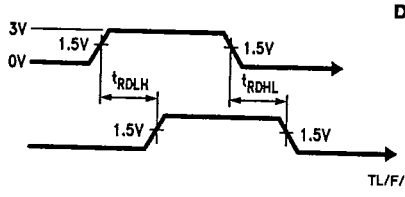
FIGURE B. B Port Test Load

Timing Waveforms

Data Path Delays:



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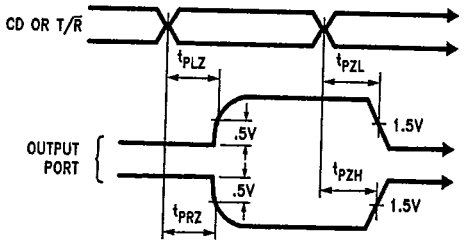

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FIGURE C