

74BCT573

Octal D Latch with TRI-STATE® Outputs

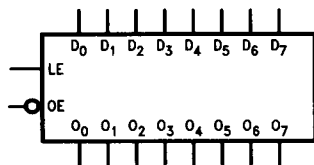
General Description

The 'BCT573 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. This device is functionally identical to the 'BCT373 but has a broadside pinout.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to the 'BCT373
- TRI-STATE outputs for bus interfacing
- Guaranteed 2000V minimum ESD protection
- Guaranteed multiple output switching specifications
- Guaranteed 500 mA minimum latchup protection
- Low I_{CCZ} through BiCMOS techniques
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

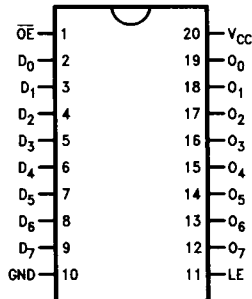
Logic Symbol



TL/F/10879-1

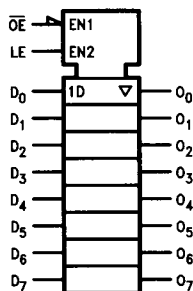
Connection Diagram

Pin Assignment for
DIP and SOIC



TL/F/10879-2

IEEE/IEC



TL/F/10879-3

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Functional Description

The 'BCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

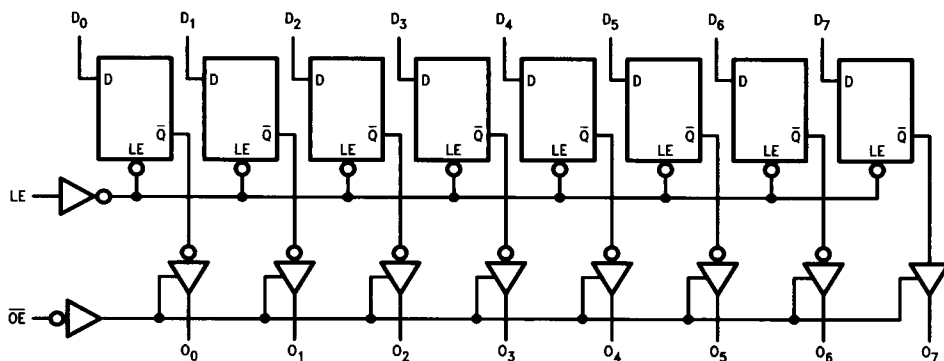
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

O_0 = Value stored from previous clock cycle

Logic Diagram



TL/F/10879-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Plastic	-55°C to +150°C

V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
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Input Voltage (Note 2)	-0.5V to +7.0V
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Input Current (Note 2)	-30 mA to +5.0 mA
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Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in the Disable or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	2000V
Over Voltage Latchup	V _{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I _{OH} = -3 mA I _{OH} = -15 mA
V _{OL}	Output LOW Voltage		0.55		V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		-250		μA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current		20		μA	0V-5.5V	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current		-20		μA	0V-5.5V	V _{OUT} = 0.5V
I _{OZ}	Output Leakage Current		±20		μA	0V-2.0V 1.8V-0V	OE = 2.0V, V _{OUT} = 0.5V or 2.7V (Power Up) OE = 2.0V, V _{OUT} = 0.5V or 2.7V (Power Down)
I _{OS}	Output Short-Circuit Current	-100	-225		mA	Max	V _{OUT} = 0V
I _{CEX}	Output HIGH Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{ZZ}	Bus Drainage Test		100		μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current	8	12		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current	29	48		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current	6	8		mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74BCT			74BCT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	4.0 7.4	8.4 10.5	2.0 3.5	8.4 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	3.0 3.0	6.8 5.7	8.9 8.3	3.0 3.0	8.9 8.3	ns
t_{PZH} t_{PZL}	Output Enable Time	3.7 3.7	6.1 6.5	10.0 10.0	3.7 3.7	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.2 2.2	4.8 4.8	7.0 7.0	2.2 2.2	7.0 7.0	ns

AC Operating Requirements

Symbol	Parameter	74BCT		74BCT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_n to LE	1.0 1.0		1.0 1.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_n to LE	4.0 4.0		4.0 4.0		ns
$t_w(\text{H})$	LE Pulse Width, HIGH	4.0		4.0		ns

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT		74BCT		74BCT		Units
		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 50 \text{ pF}$ 8 Outputs Switching (Note 1)		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 250 \text{ pF}$ 1 Output Switching (Note 2)		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 250 \text{ pF}$ 8 Outputs Switching (Notes 1, 2)		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 3.5	10.0 13.0	3.0 4.0	9.5 13.0	4.0 6.0	12.0 16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	4.0 4.0	10.0 9.5	4.0 4.0	12.0 10.0	6.0 6.0	14.5 13.0	ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc).

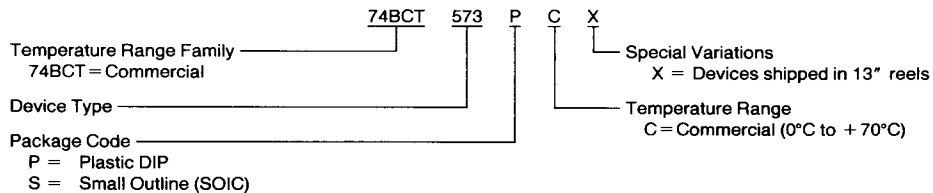
Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

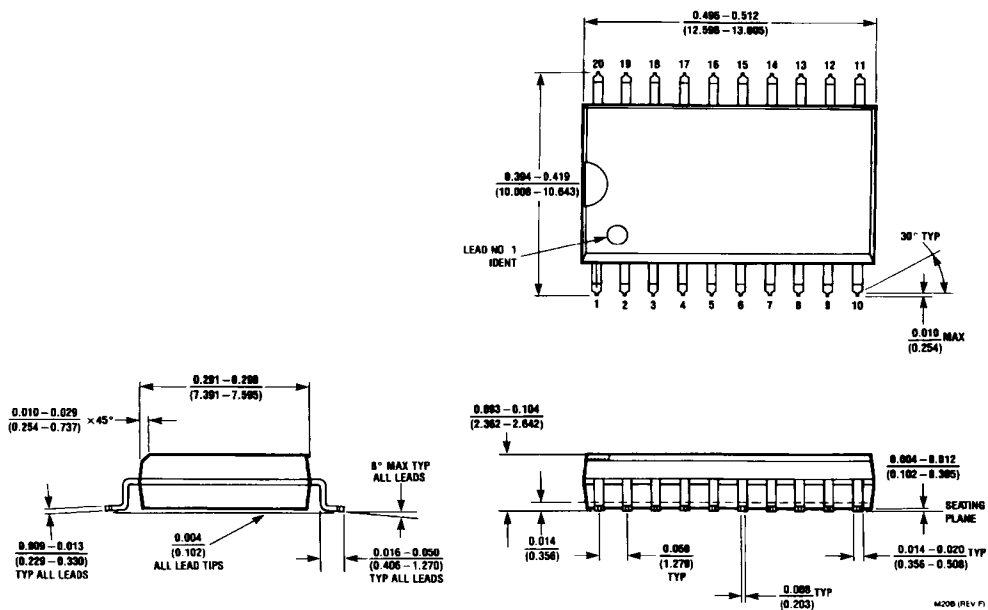
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	10.0	pF	$V_{CC} = 5.0V$

Ordering Information

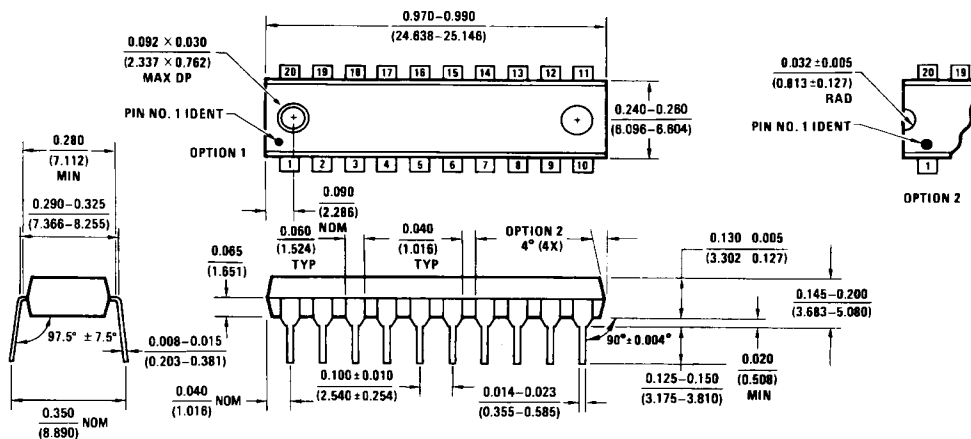
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



**20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B**

Physical Dimensions inches (millimeters) (Continued)

20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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