DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD750004, 750006, 750008

4 BIT SINGLE-CHIP MICROCOMPUTER

The μPD750008 is one of the 75XL series 4-bit single-chip microcomputers, which provide data processing capability equal to that of an 8-bit microcomputer.

The μPD750008 is an advanced model of the μPD75008. It features an enhanced CPU function and enables high-speed operation at a low voltage of 2.2 V. It can be substituted for the μPD75008. In addition, it is best suited to applications using batteries.

A built-in one-time PROM product, μPD75P0016[Note], is also available. It is suitable for small-scale production and evaluation of application systems.

Note Under development

The following user's manual describes the details of the functions of the μPD750008. Be sure to read it before designing application systems.

μPD750008 User's Manual: IEU-1421

FEATURES

- Capable of low-voltage operation: V_{DD} = 2.2 to 5.5 V
- Mk I mode/Mk II mode switch function contained
- Internal memory
  Program memory (ROM)
  : 4096 × 8 bits (μPD750004)
  : 6144 × 8 bits (μPD750006)
  : 8192 × 8 bits (μPD750008)
  Data memory (RAM)
  : 512 × 4 bits
- Function for specifying the instruction execution time (useful for high-speed operation and saving power) ★
  0.95 μs, 1.91 μs, 3.81 μs, 15.3 μs (when operating at 4.19 MHz)
  0.67 μs, 1.33 μs, 2.67 μs, 10.7 μs (when operating at 6.0 MHz)
  122 μs (when operating at 32.768 kHz)
- Enhanced timer function (4 channels)
- Can be easily substituted for the μPD75008 because this product succeeds to the functions and instructions of the μPD75008.

APPLICATIONS

Cordless telephones, radio devices, audio products, and home electric appliances

ORDERING INFORMATION

Part number	Package
μPD750004CU-×××	42-pin plastic shrink DIP (600 mil)
μPD750004GB-×××-3B4	44-pin plastic QFP (10 × 10 mm)
μPD750006CU-×××	42-pin plastic shrink DIP (600 mil)
μPD750006GB-×××-3B4	44-pin plastic QFP (10 × 10 mm)
μPD750008CU-×××	42-pin plastic shrink DIP (600 mil)
μPD750008GB-×××-3B4	44-pin plastic QFP (10 × 10 mm)

Remark ××× is a mask ROM code number.

In this manual, the product described is the μPD750008 unless otherwise specified.

The information in this document is subject to change without notice.

Document No. IC-3647
(O. D. No. IC-8960)
Date Published April 1995 P
Printed in Japan

Major changes in this revision are indicated by starts (★) in the margins.

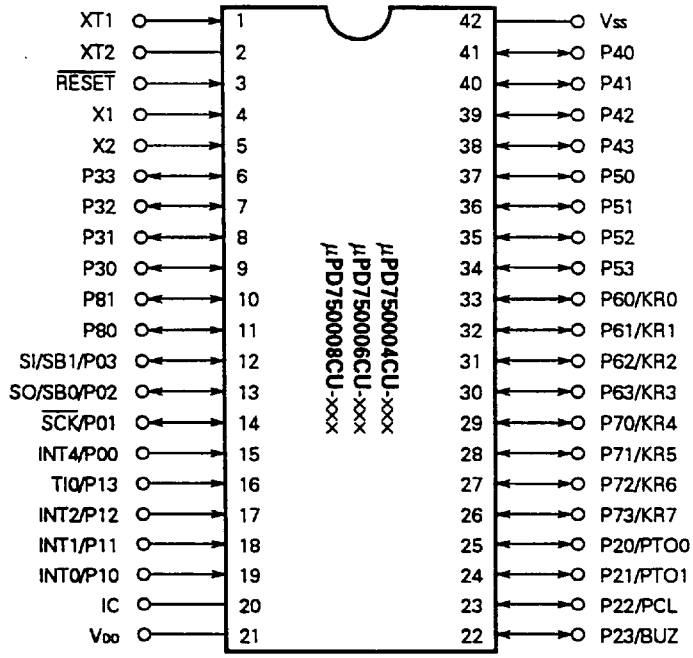
FUNCTIONS

Item		Function			
Command execution time		• 0.95, 1.91, 3.81, 15.3 μs (when the main system clock operates at 4.19 MHz) • 0.67, 1.33, 2.67, 10.7 μs (when the main system clock operates at 6.0 MHz) • 122 μs (when the subsystem clock operates at 32.768 kHz)			
Internal memory	ROM	4096 × 8 bits (μPD750004)			
		6144 × 8 bits (μPD750006)			
		8192 × 8 bits (μPD750008)			
	RAM	512 × 4 bits			
General-purpose register		• When operating in 4 bits: 8 × 4 banks • When operating in 8 bits: 4 × 4 banks			
I/O port		34	8	CMOS I/O pins	Can incorporate 25 pull-up resistors that are specified with the software.
			18	CMOS input-output pins Four pins can directly drive the LED.	
			8	N-ch open-drain I/O pins Eight pins can directly drive the LED.	Can withstand 10 V. Can incorporate pull-up resistors that are specified with the mask option.
Timer		4	• Timer/event counter • Timer counter • Basic interval timer: Can be used as a watchdog timer. • Clock timer: Can output a buzzer sound.		
Serial interface		• Three-wire serial I/O mode (switchable between the start LSB and the start MSB) • Two-wire serial I/O mode • SBI mode			
Bit sequential buffer		16 bits			
Clock output		• Φ, 524 kHz, 262 kHz, 65.5 kHz (when the main system clock operates at 4.19 MHz) • Φ, 750 kHz, 375 kHz, 93.7 kHz (when the main system clock operates at 6.0 MHz)			
Vectored interrupt		External: 3 Internal : 4			
Test input		External: 1 Internal : 1			
System clock oscillator		• Ceramic or crystal oscillator for main system clock • Crystal oscillator for subsystem clock			
Standby		STOP/HALT mode			
Operating ambient temperature range		−40 to +85 °C			
★ Operating supply voltage		2.2 to 5.5 V			
Package		42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 × 10 mm)			

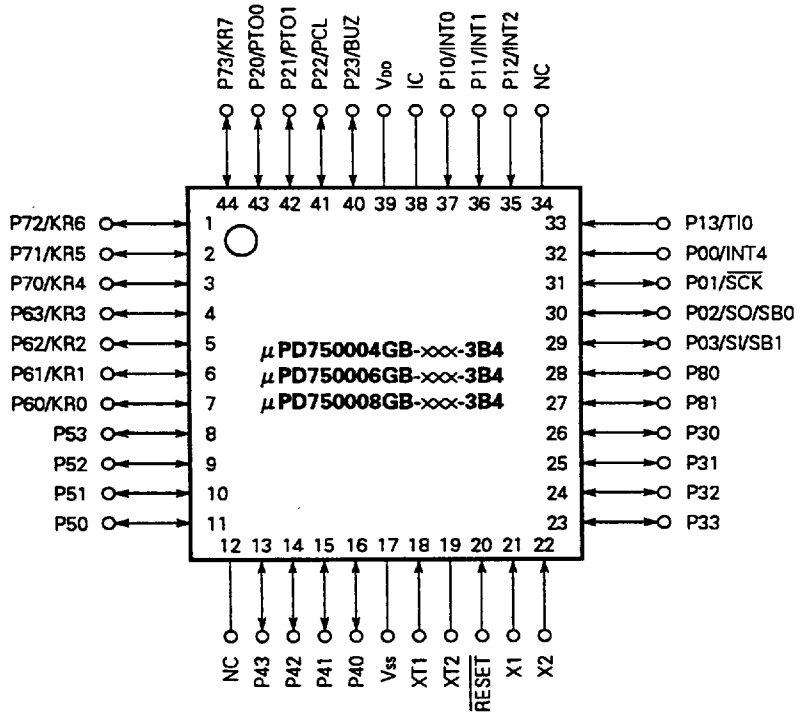
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **42-pin plastic shrink DIP (600 mil)**



- **44-pin plastic QFP (10 × 10 mm)**

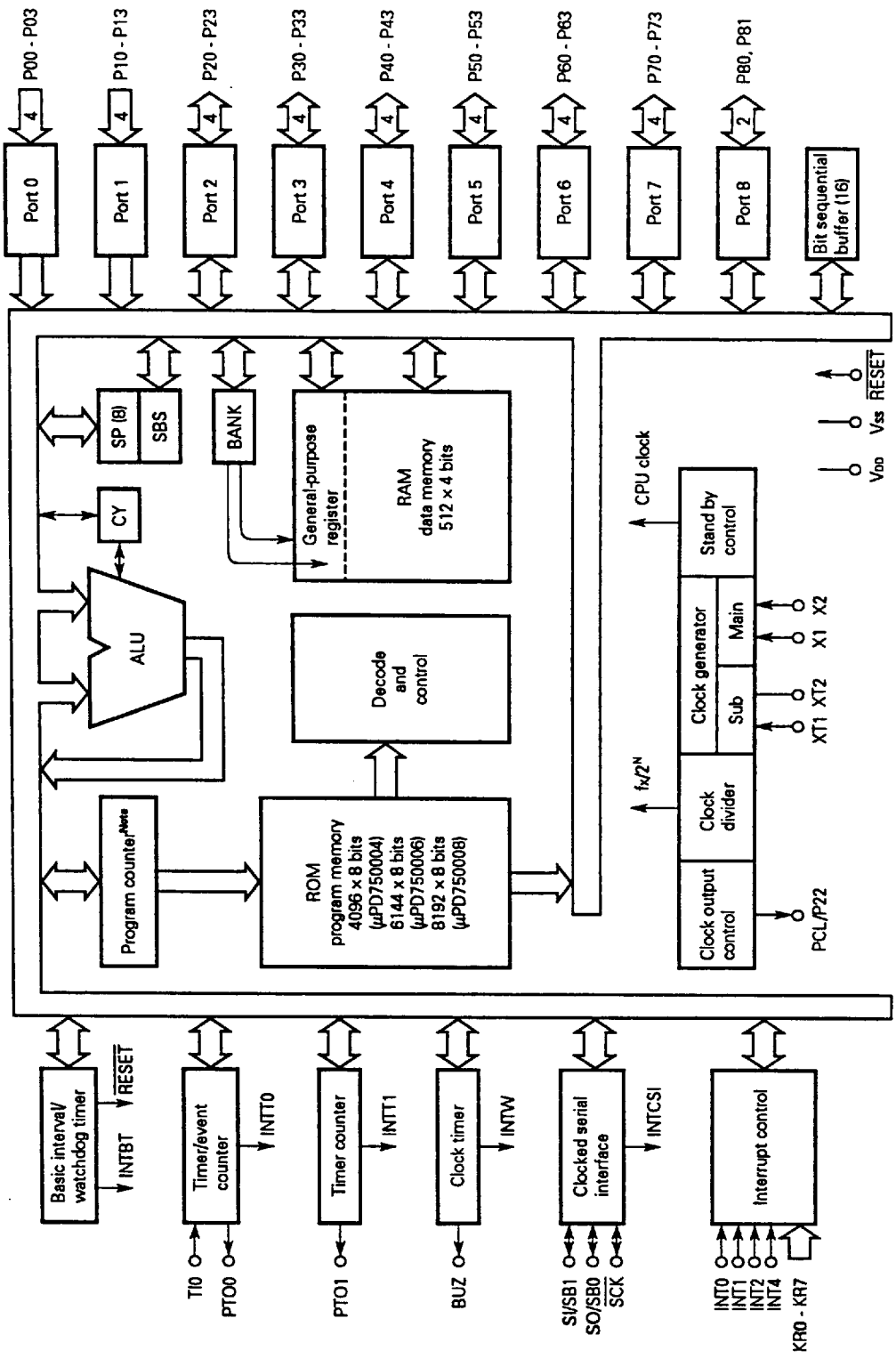


IC : Internally connected (Connect directly to VDD.)

PIN NAMES

P00 - 03	:	Port 0
P10 - 13	:	Port 1
P20 - 23	:	Port 2
P30 - 33	:	Port 3
P40 - 43	:	Port 4
P50 - 53	:	Port 5
P60 - 63	:	Port 6
P70 - 73	:	Port 7
P80, 81	:	Port 8
KR0 - 7	:	Key Return
$\overline{SCK}$	:	Serial Clock
SI	:	Serial Input
SO	:	Serial Output
SB0, 1	:	Serial Bus 0, 1
$\overline{RESET}$	:	Reset Input
TI0	:	Timer Input 0
PTO0, 1	:	Programmable Timer Output 0, 1
BUZ	:	Buzzer Clock
PCL	:	Programmable Clock
INT0, 1, 4	:	External Test Interrupt 0, 1, 4
INT2	:	External Test Input 2
X1, 2	:	Main System Clock Oscillation 1, 2
XT1, 2	:	Subsystem Clock Oscillation 1, 2
NC	:	No Connection
IC	:	Internally Connected

2. BLOCK DIAGRAM



Note The program counter consists of 12 bits in the μPD750004 and 13 bits in the μPD750006 and μPD750008.

3. PIN FUNCTIONS

3.1 PORT PINS

Pin name	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01 - P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30[Note 2]	I/O	–	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31[Note 2]		–				
P32[Note 2]		–				
P33[Note 2]		–				
P40 - P43[Notes 2, 3]	I/O	–	N-ch open-drain 4-bit I/O port (PORT4). A pull-up resistor can be provided for each bit (mask option). Withstand voltage is 10 V in open-drain mode.	○	High level (when pull-up resistors are provided) or high impedance	M-D
P50 - P53[Notes 2, 3]	I/O	–	N-ch open-drain 4-bit I/O port (PORT5). A pull-up resistor can be provided for each bit (mask option). Withstand voltage is 10 V in open-drain mode.		High level (when pull-up resistors are provided) or high impedance	M-D
P60	I/O	KR0	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit I/O port (PORT7). Pull-up resistors can be provided by software in units of 4 bits.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	—	2-bit I/O port (PORT8). Pull-up resistors can be provided by software in units of 2 bits.	×	Input	E-B
P81		—				

Notes 1. The circle (○) indicates the Schmitt trigger input.

2. Can directly drive the LED.

3. When pull-up resistors that can be specified with the mask option are not incorporated (when pins are used as N-ch open-drain input ports), the input leak low current increases when an input instruction or bit operation instruction is executed.

3.2 NON-PORT PINS

Pin name	Input/ output	Shared pin	Function	When reset	I/O circuit type[Note 1]
TI0	Input	P13	Input pin for receiving external event pulse signal for timer/event counter	–	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output pin	Input	E-B
PTO1		P21			
PCL	I/O	P22	Clock output pin	Input	E-B
BUZ	I/O	P23	Fixed frequency output pin (for buzzer output or system clock trimming)	Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O pin	Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output pin Serial bus I/O pin	Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input pin Serial bus I/O pin	Input	Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input pin (both rising and falling edges are detected)	–	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input pin (detection edge selectable) Note 2	–	Ⓑ-C
INT1		P11	Note 3		
INT2	Input	P12	Test input pin for detecting the first rising edge from the test input Note 3	–	Ⓑ-C
KR0 - KR3	I/O	P60 - P63	Test input pins for detecting the first falling edges from the test inputs	Input	Ⓕ-A
KR4 - KR7	I/O	P70 - P73	Test input pins for detecting the first falling edges from the test inputs	Input	Ⓕ-A
X1, X2	Input	–	Crystal/ceramic connection pin for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.	–	–
XT1	Input	–	Crystal connection pin for subsystem clock generation. When external clock signal is used, connect it to XT1. Leave XT2 open.	–	–
XT2	–				
$\overline{RESET}$	Input	–	System reset input pin	–	Ⓑ
IC	–	–	Internally connected. (To be connected directly to V_{DD})	–	–
V_{DD}	–	–	Positive power supply pin	–	–
V_{SS}	–	–	GND potential pin	–	–

Notes 1. The circle (◯) indicates the Schmitt trigger input.

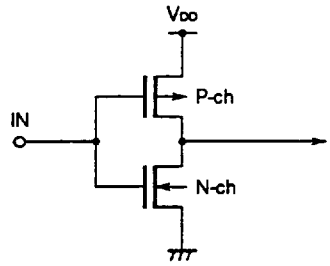
2. Clock synchronous

3. Asynchronous

3.3 PIN INPUT/OUTPUT CIRCUITS

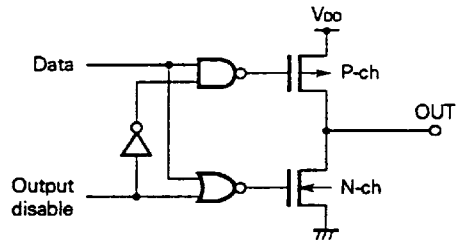
The input/output circuit of each μPD750008 pin is shown below in a simplified manner.

Type A (For type E-B)



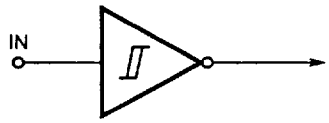
CMOS input buffer

Type D (For type E-B, F-A)



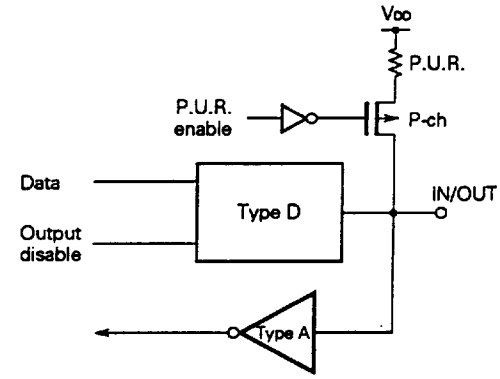
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



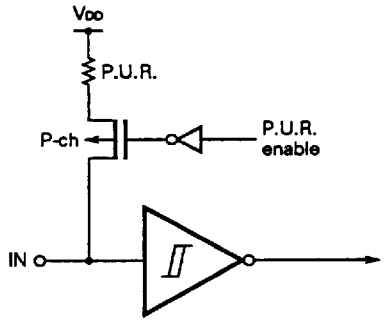
Schmitt trigger input with hysteresis

Type E-B



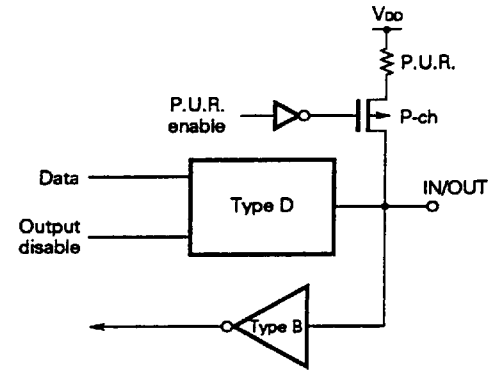
P.U.R.: Pull-Up Resistor

Type B-C

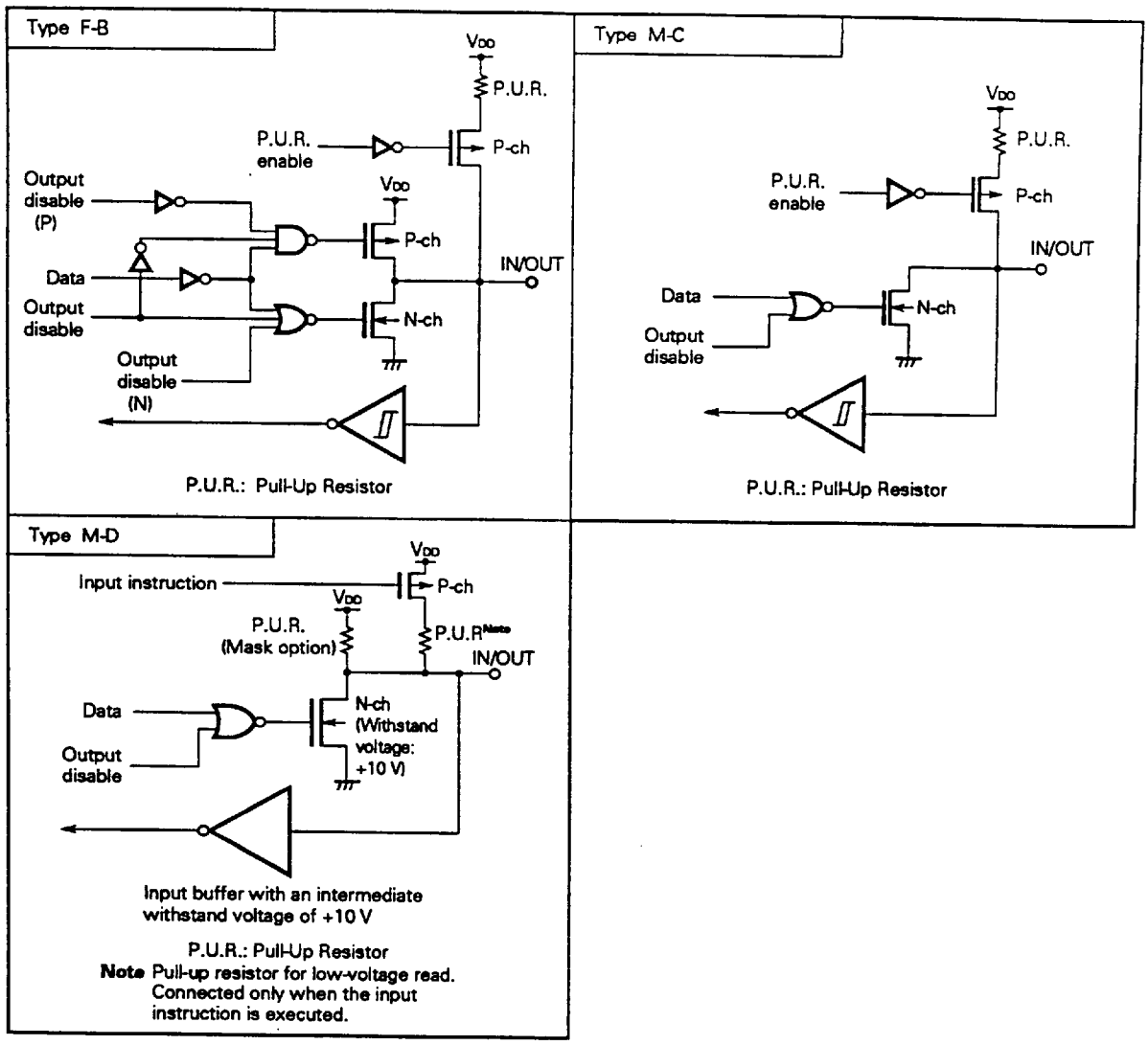


P.U.R.: Pull-Up Resistor

Type F-A



P.U.R.: Pull-Up Resistor



3.4 MASK OPTION SELECTION

The following mask options are available for selection for each pin.

Table 3-1 Mask Option Selection

Pin name	Mask option	
P40 - P43, P50 - P53	Pull-up resistor provided	Pull-up resistor not provided

Remark A mask option can be specified for each bit.

3.5 CONNECTION OF UNUSED PINS

Table 3-2 Connection of Unused Pins

Pin name	Recommended connection
P00/INT4	To be connected to V_{SS}
P01/$\overline{SCK}$	To be connected to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	To be connected to V_{SS}
P13/TI0	
P20/PTO0	Input state : To be connected to V_{SS} or V_{DD} through a separate resistor Output state: To be left open
P21/PTO1	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60-P63	
P70-P73	
P80, P81	
XT1	To be connected to V_{SS} or V_{DD}
XT2	To be left open
IC	To be connected directly to V_{DD}

4. Mk I MODE/Mk II MODE SWITCH FUNCTION

4.1 DIFFERENCES BETWEEN Mk I MODE AND Mk II MODE

The CPU of the μPD750008 subseries has two modes (Mk I mode and Mk II mode) and which mode is used is selectable. Bit 3 of the stack bank selection register (SBS) determines the mode.

- Mk I mode: This mode has the upward compatibility with the μPD75008 subseries. It can be used in the 75XL CPUs having a ROM of up to 16KB.
- Mk II mode: This mode is not compatible with the μPD75008 subseries. It can be used in all 75XL CPUs, including those having a ROM of 16KB or more.

Table 4-1 shows the differences between Mk I mode and Mk II mode.

Table 4-1 Differences between Mk I Mode and Mk II Mode

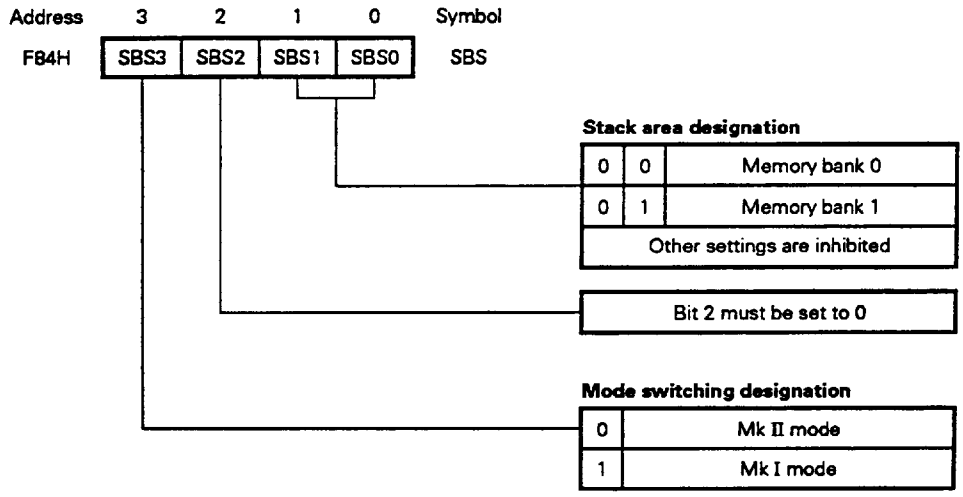
	Mk I mode	Mk II mode
Number of stack bytes in a subroutine instruction	2 bytes	3 bytes
BRA !addr instruction CALLA !addr instruction	Undefined operation	Normal operation
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

4.2 SETTING OF THE STACK BANK SELECTION REGISTER (SBS)

The Mk I mode and Mk II mode are switched by stack bank selection register. Fig. 4-1 shows the register configuration.

The stack bank selection register is set with a 4-bit memory operation instruction. To use the CPU in Mk I mode, initialize the register to 10××B[Note] at the beginning of the program. To use the CPU in Mk II mode, initialize it to 00××B[Note].

Fig. 4-1 Stack Bank Selection Register Format



Note Specify the desired value in ××.

Caution The CPU operates in Mk I mode after the $\overline{\text{RESET}}$ signal is issued, because bit 3 of SBS is set to 1. Set bit 3 of SBS to 0 (Mk II mode) to use the CPU in Mk II mode.

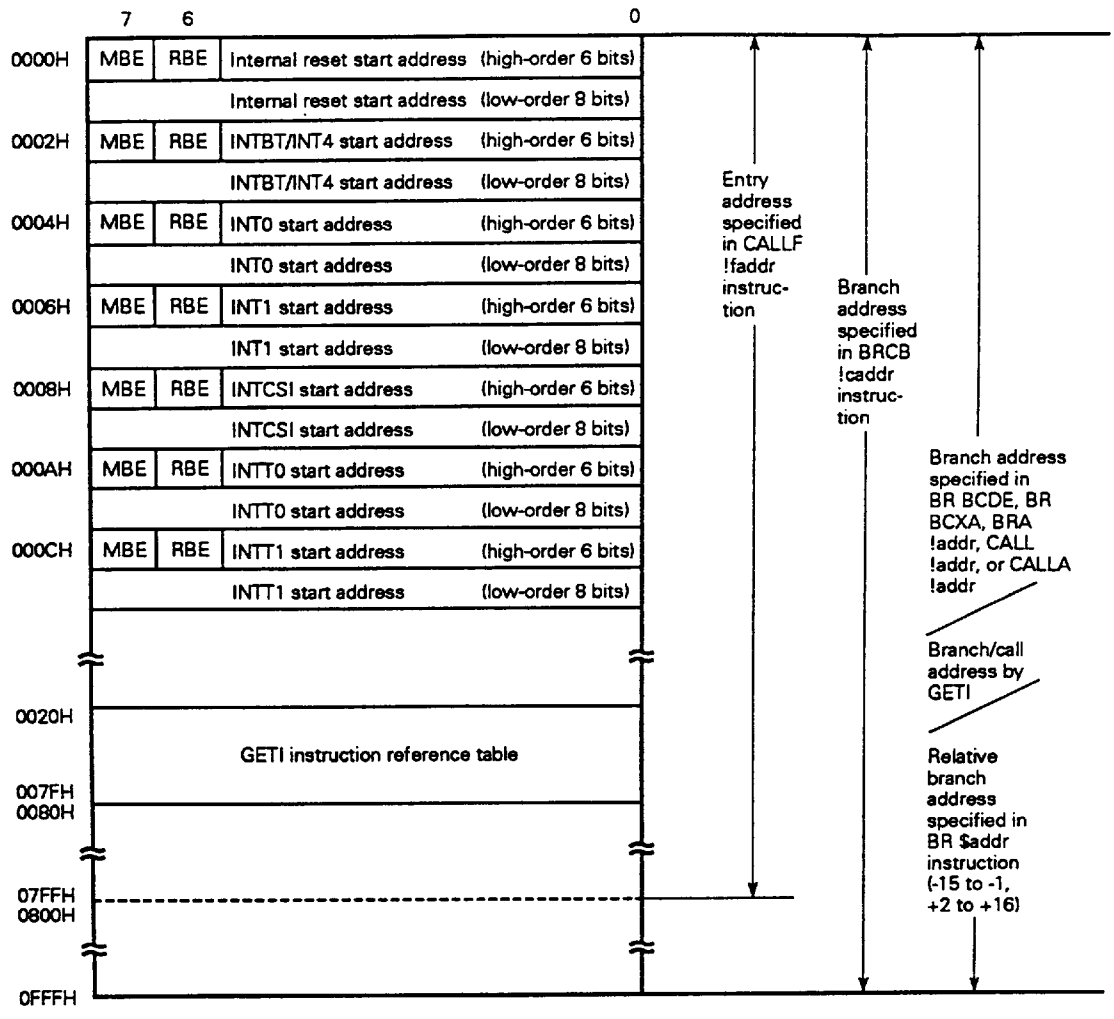
5. MEMORY CONFIGURATION

- Program memory (ROM) ....4096 × 8 bits (0000H-0FFFH): μPD750004
  6144 × 8 bits (0000H-17FFH): μPD750006
  8192 × 8 bits (0000H-1FFFH): μPD750008

- 0000H to 0001H
  Vector address table for holding the RBE and MBE values and program start address when a $\overline{\text{RESET}}$ signal is issued (allowing a reset start at an arbitrary address)
- 0002H to 000DH
  Vector address table for holding the RBE and MBE values and program start address for each vectored interrupt (allowing interrupt processing to be started at an arbitrary address)
- 0020H to 007FH
  Table area referenced by the GETI instruction

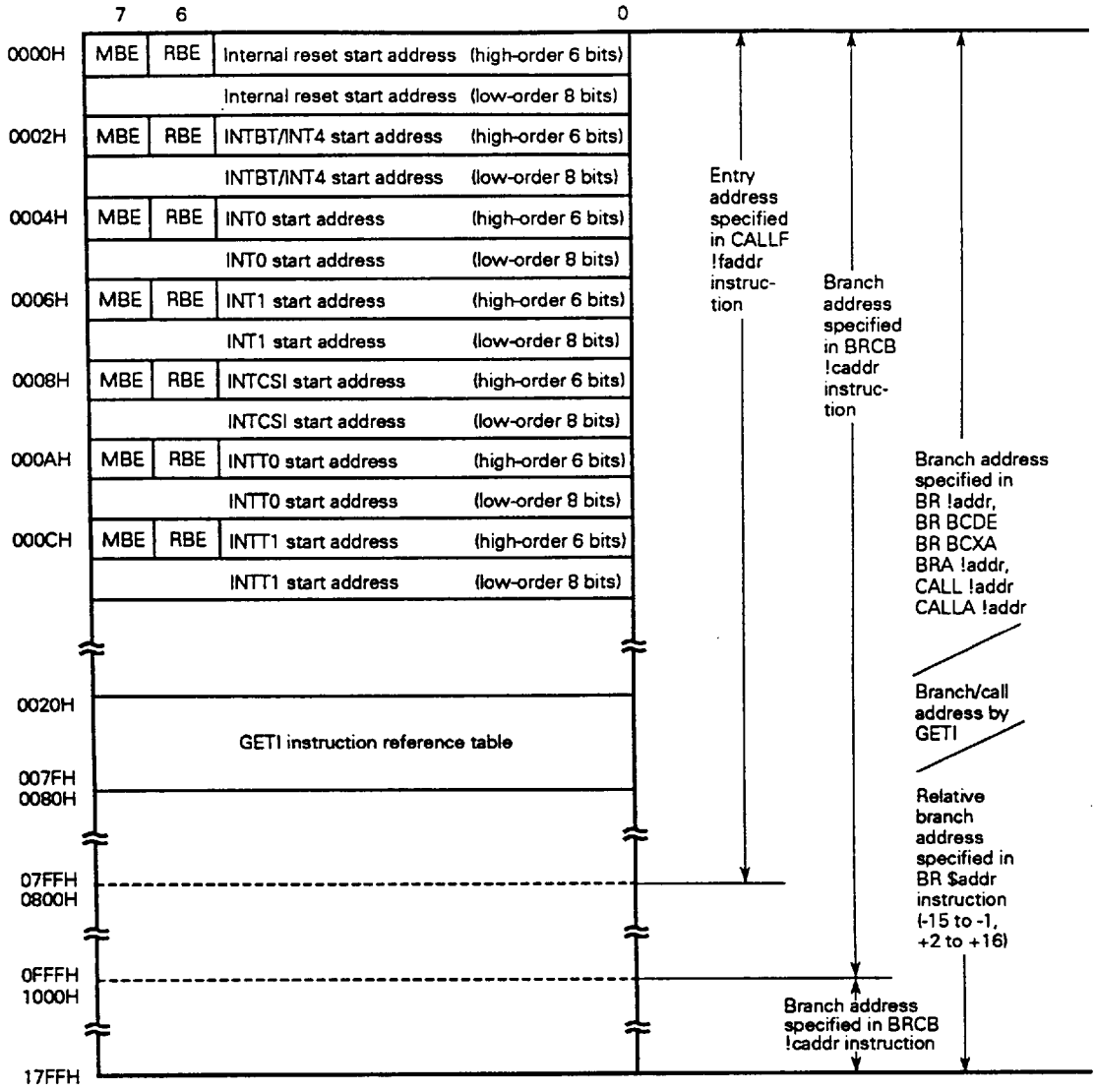
- Data memory (RAM)
  - Data area : 512 × 4 bits (000H to 1FFH)
  - Peripheral hardware area : 128 × 4 bits (F80H to FFFH)

Fig. 5-1 Program Memory Map (in μPD750004)



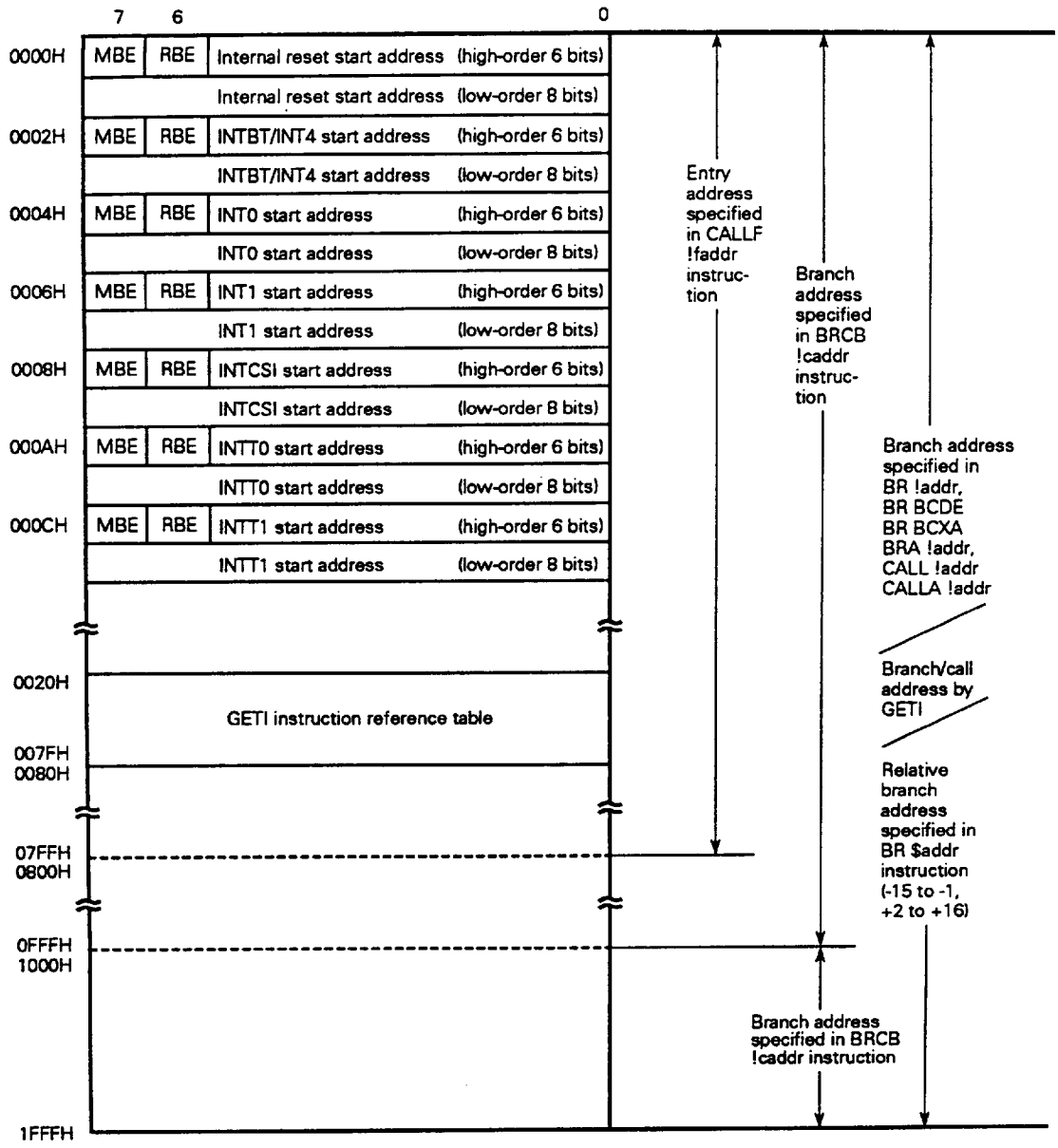
Remark In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.

Fig. 5-2 Program Memory Map (in μPD750006)



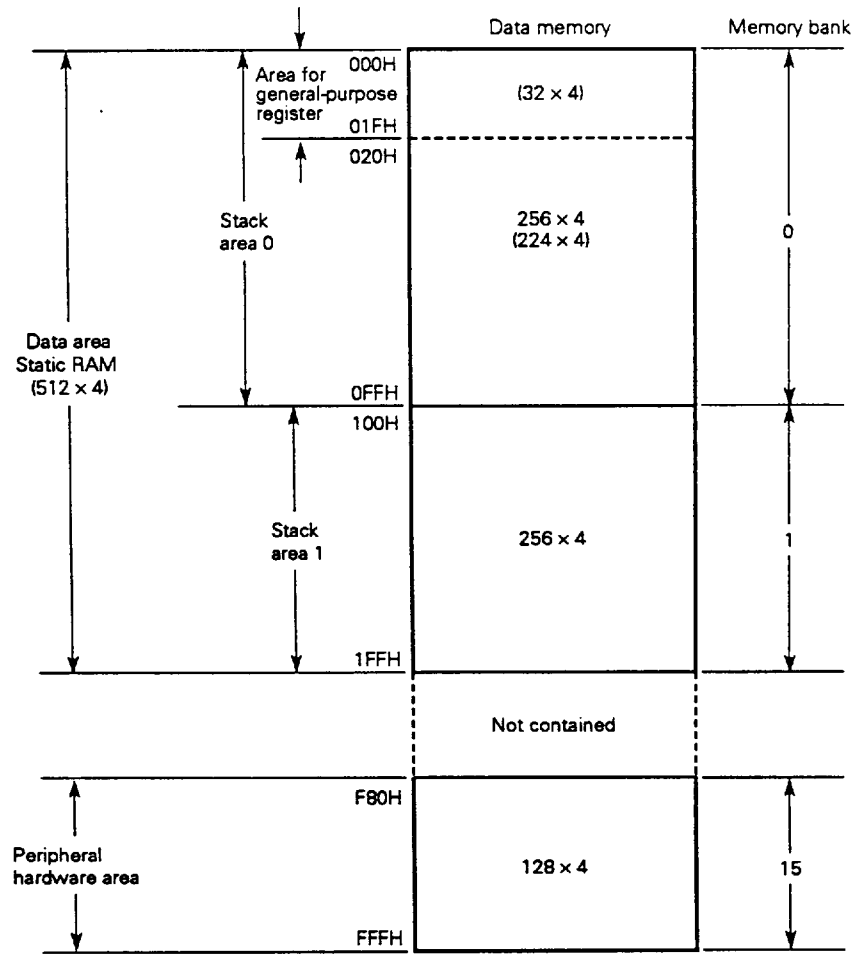
Remark **In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.**

Fig. 5-3 Program Memory Map (in μPD750008)



Remark **In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.**

Fig. 5-4 Data Memory Map



6. PERIPHERAL HARDWARE FUNCTIONS

6.1 PORTS

The μPD750008 has the following three types of I/O port:

- 8 CMOS input pins (PORT0 and PORT1)
- 18 CMOS I/O pins (PORT2, PORT3, and PORT6 to PORT8)
- 8 N-ch open-drain I/O pins (PORT4 and PORT5)

Total: 34 pins

Table 6-1 Digital Ports and Their Features

Port name (symbol)	Function	Operation and feature	Remarks
PORT0	4-bit I/O	Allows read and test at any time regardless of the operation modes of another functions assigned to these pins.	Also used as INT4, $\overline{SCK}$, SO/SB0, and SI/SB1.
PORT1			Also used as INT0 to INT2 and TI0.
PORT3[Note]	4-bit I/O	Allows input or output mode setting bit by bit.	PORT6 is also used as KR0 to KR3.
PORT6			
PORT2		Allows input or output mode setting in units of 4 bits. Ports 6 and 7 can be paired, allowing data I/O in units of 8 bits.	Also used as PTO0, PTO1, PCL, and BUZ.
PORT7			Also used as KR4 to KR7.
PORT4[Note] PORT5[Note]	4-bit I/O (N-ch open-drain; can withstand 10 V)	Allows input or output mode setting in units of 4 bits. Ports 4 and 5 can be paired, allowing data I/O in units of 8 bits.	Whether to use pull-up resistors can be specified bit by bit with a mask option.
PORT8	2-bit I/O	Allows input or output mode setting in units of 2 bits.	–

Note Can directly drive the LED.

P10 is also used as an external vectored interrupt input pin. This input is provided with a noise eliminator.

6.2 CLOCK GENERATOR

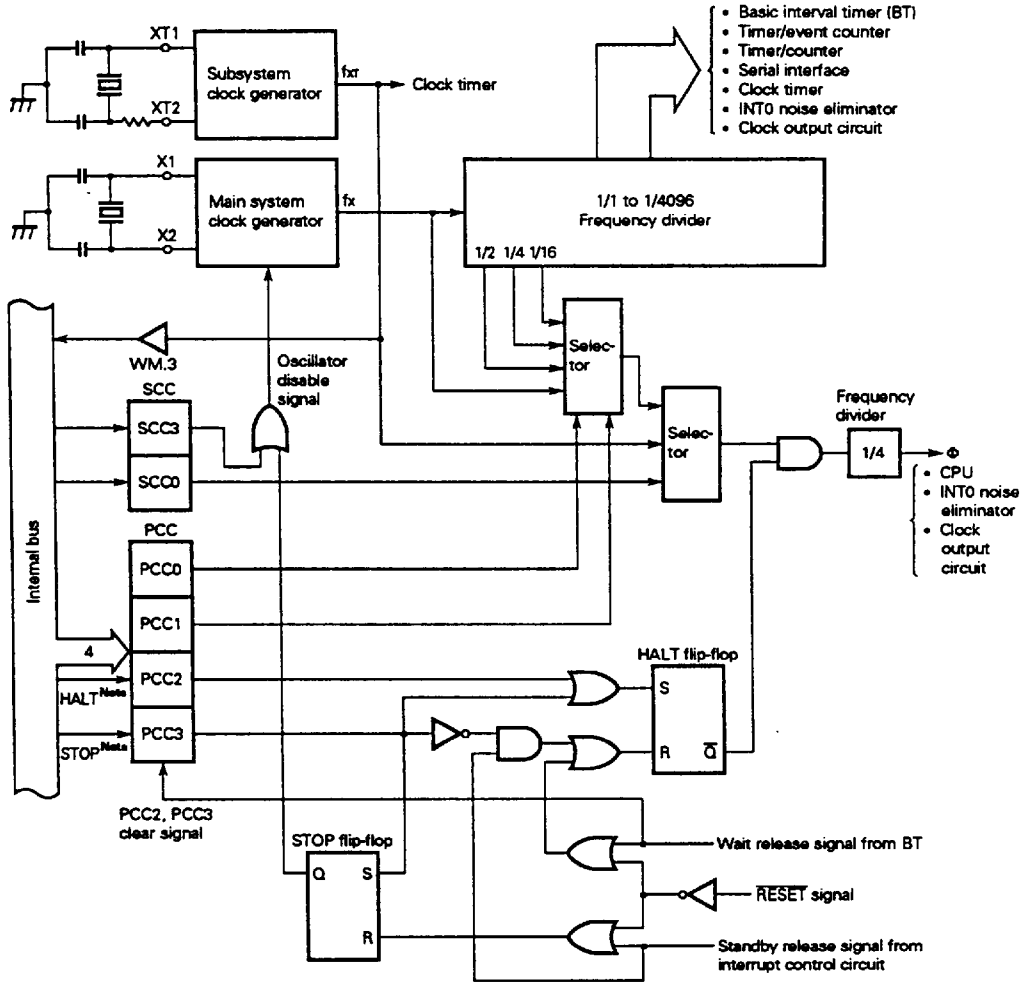
Operation of the clock generator is specified by the processor clock control register (PCC) and system clock control register (SCC).

The main system clock and subsystem clock are used.

The instruction execution time can be made variable.

- 0.95 μs, 1.91 μs, 3.82 μs, 15.3 μs (when the main system clock is at 4.19 MHz)
- 0.67 μs, 1.33 μs, 2.67 μs, 10.7 μs (when the main system clock is at 6.00 MHz)
- 122 μs (when the subsystem clock is at 32.768 kHz)

Fig. 6-1 Clock Generator Block Diagram



Note Instruction execution

Remarks 1. fx = Main system clock frequency

2. fXT = Subsystem clock frequency

3. Φ = CPU clock

4. PCC: Processor clock control register

5. SCC: System clock control register

6. One clock cycle (tCY) of the CPU clock (Φ) is equal to one machine cycle of an instruction.

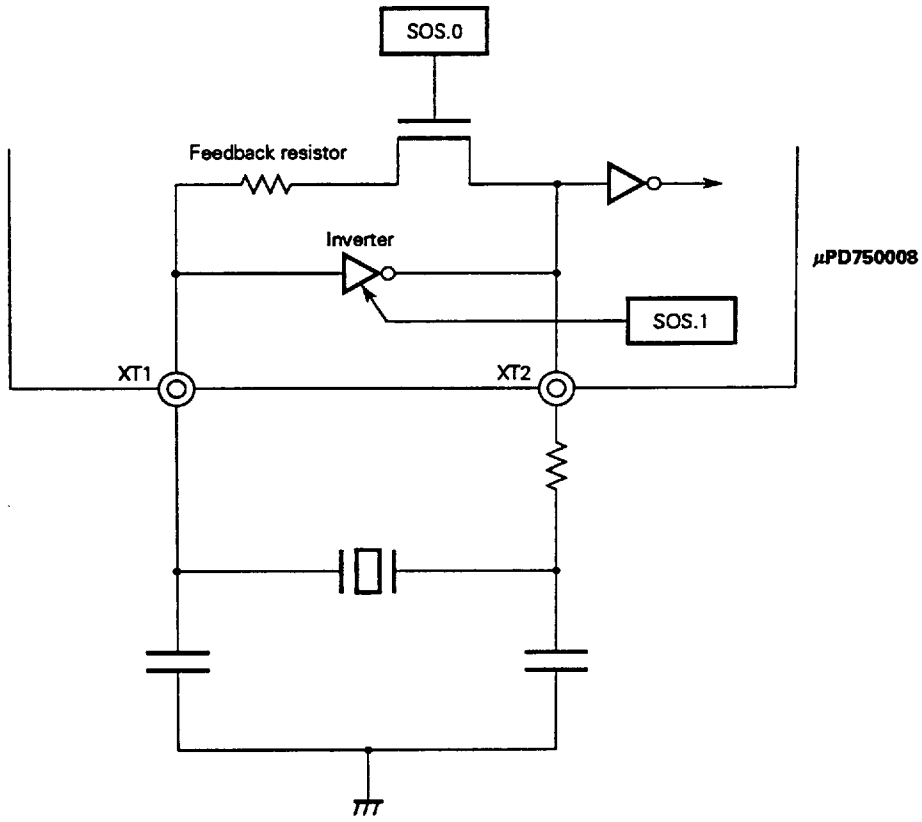
6.3 CONTROL FUNCTIONS OF SUBSYSTEM CLOCK OSCILLATOR

The subsystem clock oscillator of the μPD750008 subseries has two control functions to decrease the supply current.

- The function to select with the software whether to use the built-in feedback resistor
- The function to suppress the supply current by reducing the drive current of the built-in inverter when the operating supply voltage is high ($V_{DD} \geq 2.7$ V)

Each function can be used by switching bits 0 and 1 in the sub-oscillator control register (SOS). (See Fig. 6-2.)

Fig. 6-2 Subsystem Clock Oscillator

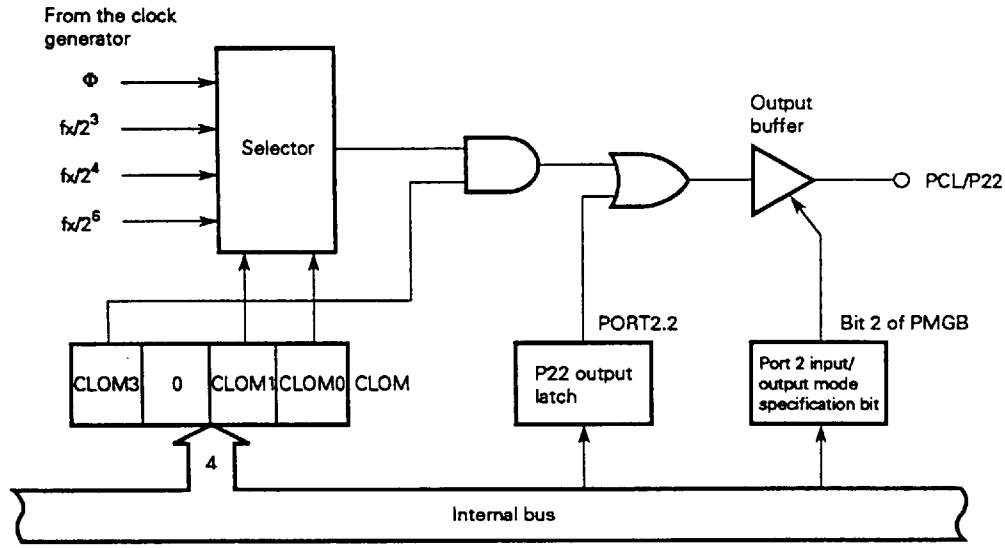


6.4 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs a clock pulse from the P22/PCL pin. This clock pulse is used for remote control output, peripheral LSIs, etc.

- Clock output (PCL): Φ, 524, 262, or 65.5 kHz (at 4.19 MHz)
  Φ, 750, 375, or 93.8 kHz (at 6.00 MHz)

Fig. 6-3 Clock Output Circuit Configuration



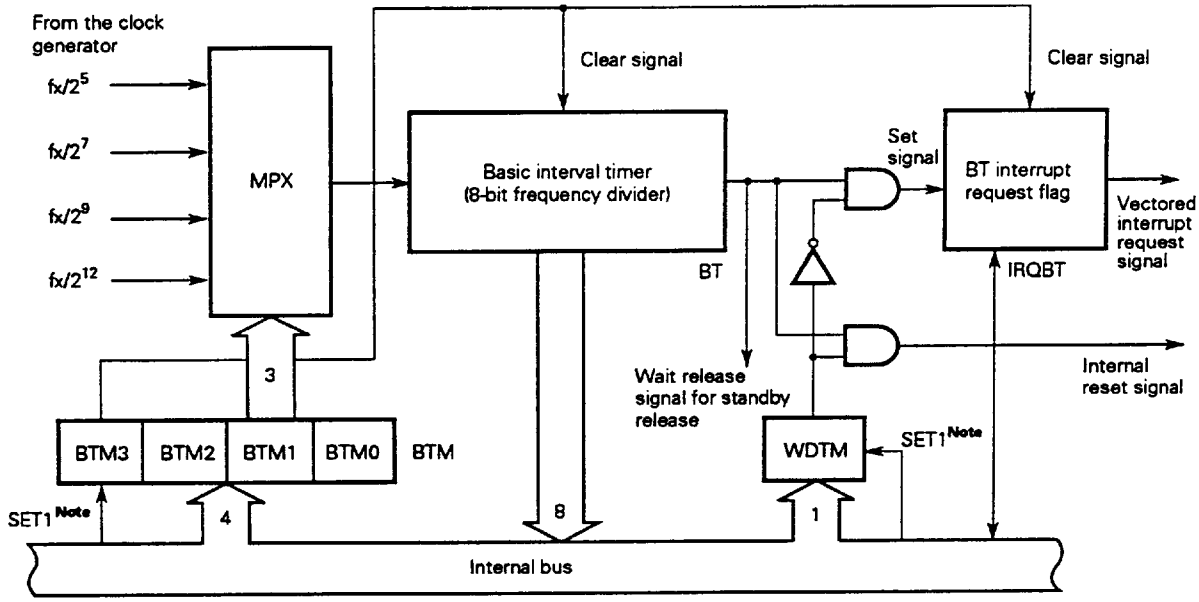
Remark Measures are taken to prevent outputting a narrow pulse when selecting clock output enable/disable.

6.5 BASIC INTERVAL/WATCHDOG TIMER

The basic interval/watchdog timer has these functions:

- Interval timer operation which generates a reference timer interrupt
- Operation as a watchdog timer for detecting program crashes and resetting the CPU
- Selection of wait time for releasing the standby mode and counting the wait time
- Reading out the count value

Fig. 6-4 Block Diagram of the Basic Interval/Watchdog Timer



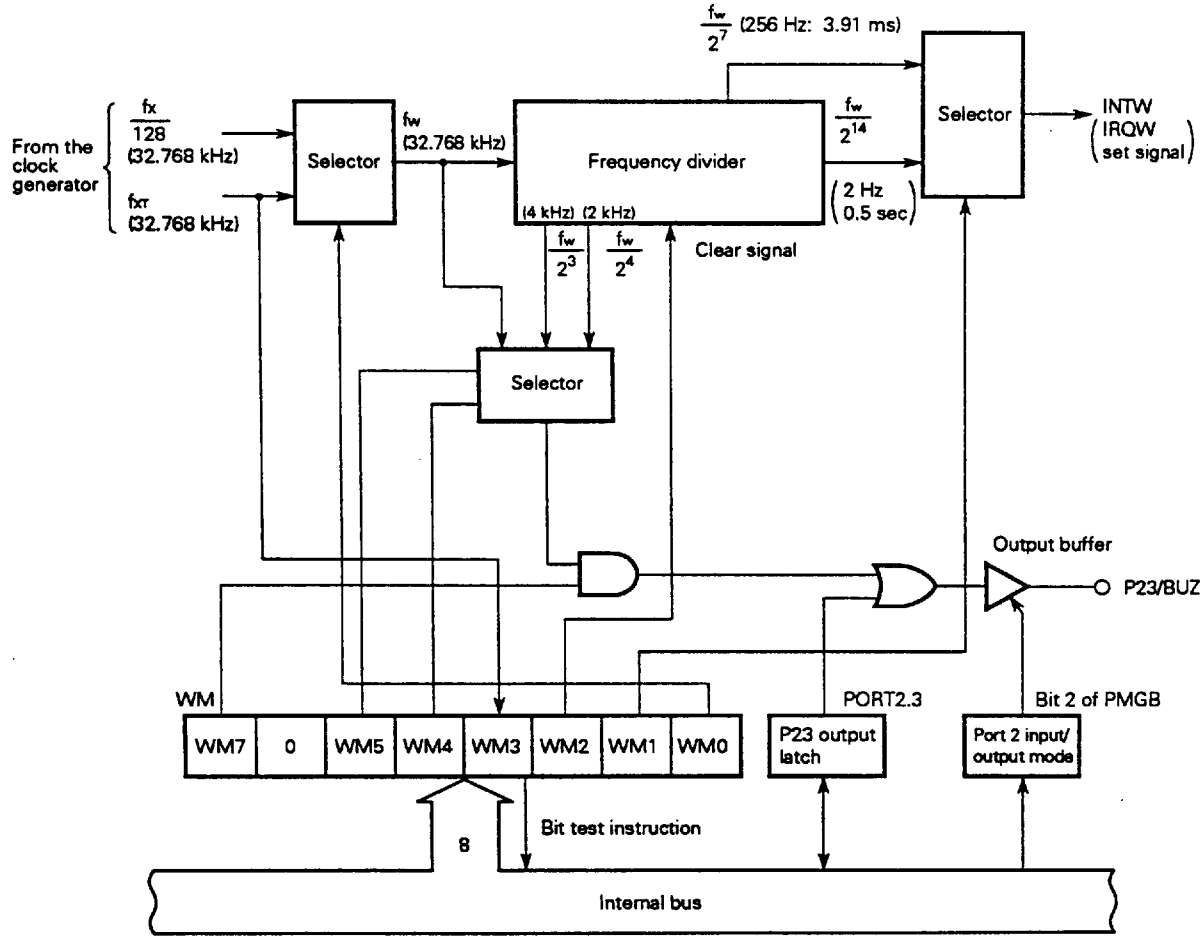
Note Instruction execution

6.6 CLOCK TIMER

The μPD750008 contains one channel for a clock timer. The clock timer provides the following functions:

- Sets the test flag (IRQW) with a 0.5 sec interval. The standby mode can be released by IRQW.
- The 0.5 second interval can be generated from either the main system clock or subsystem clock. Use a main system clock of 4.194304 MHz.
- The time interval can be made 128 times faster (3.91 ms) by selecting the fast mode. This is convenient for program debugging, testing, etc.
- Any of the frequencies 2.048 kHz, 4.096 kHz, and 32.768 kHz can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that a zero-second start of the clock can be made.

Fig. 6-5 Clock Timer Block Diagram



( ) is for fx = 4.194304 MHz, fxT = 32.768 kHz.

6.7 TIMER/EVENT COUNTER

The μPD750008 contains one channel for a timer/event counter. The timer/event counter provides the following functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin
- Event counter operation
- Divides the TI0 pin input by N and outputs to the PTO0 pin (frequency divider operation)
- Supplies serial shift clock to the serial interface circuit
- Count condition read out function.

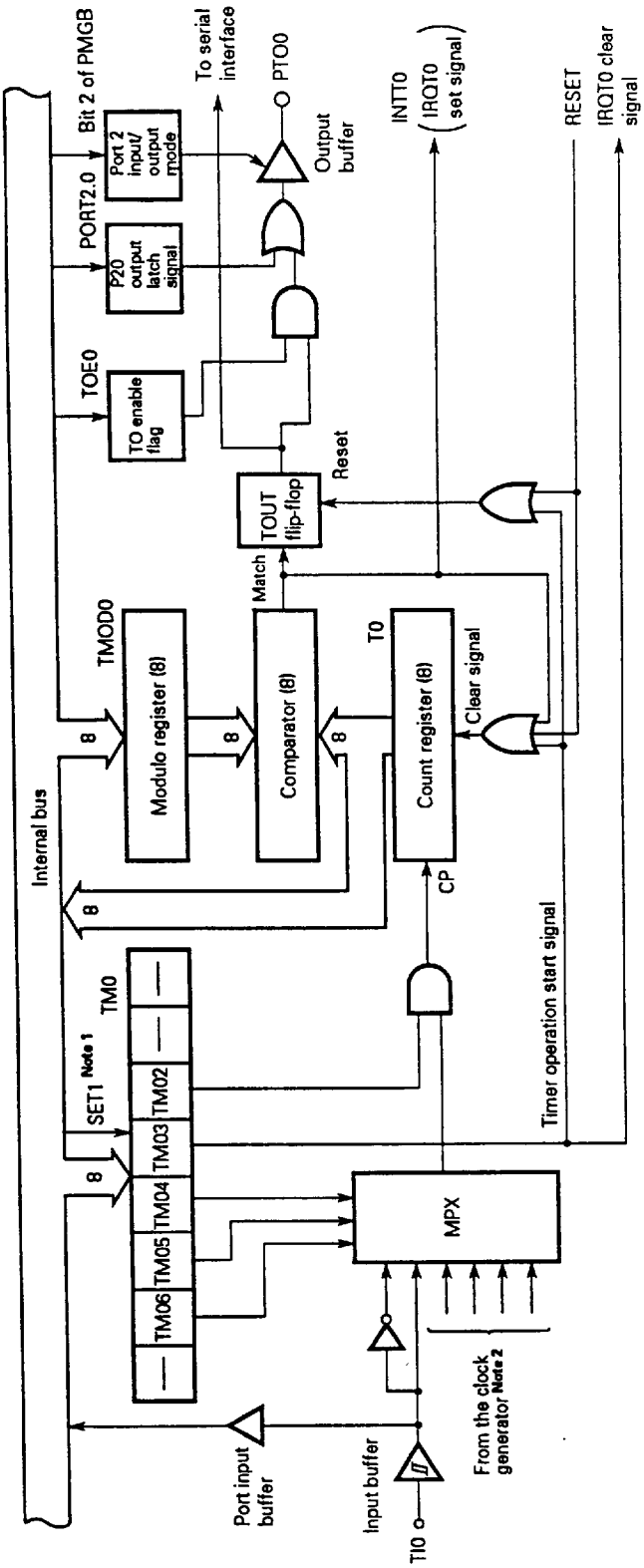


Fig. 6-6 Timer/Event Counter Block Diagram

Notes 1. Instruction execution
2. See Fig. 6-1.

6.8 TIMER/COUNTER

The μPD750008 contains one channel for a timer/counter. The timer/counter provides the following functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO1 pin
- Count condition read out function.

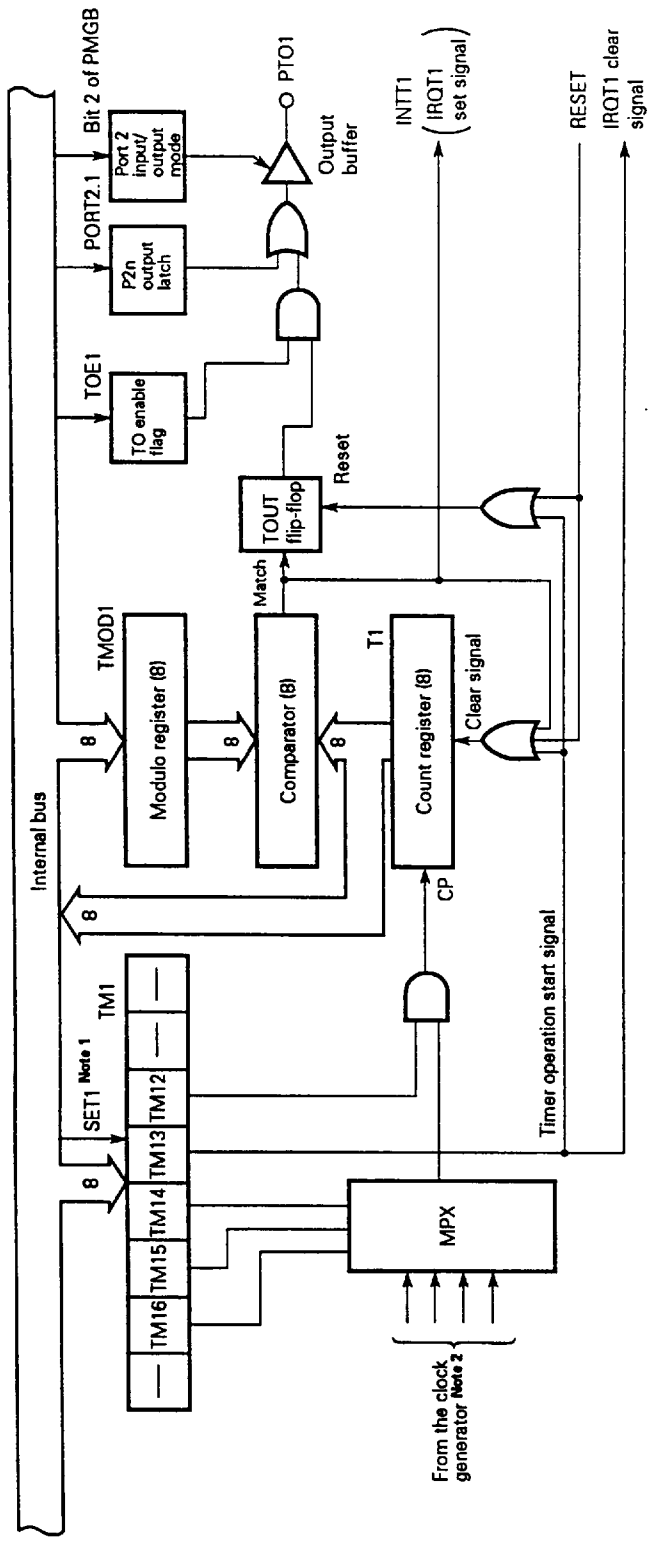


Fig. 6-7 Timer/Counter Block Diagram

Notes 1. Instruction execution
2. See Fig. 6-1.

6.9 SERIAL INTERFACE

The μPD750008 has three modes.

- Three-wire serial I/O mode (The first bit is switchable between MSB and LSB.)
- Two-wire serial I/O mode (The first bit is MSB.)
- SBI mode (The first bit is MSB.)

The three-wire serial I/O mode enables connections to be made with the 75X series, 78K series, and many other types of I/O devices.

The two-wire serial I/O mode and SBI mode enable communication with two or more devices.

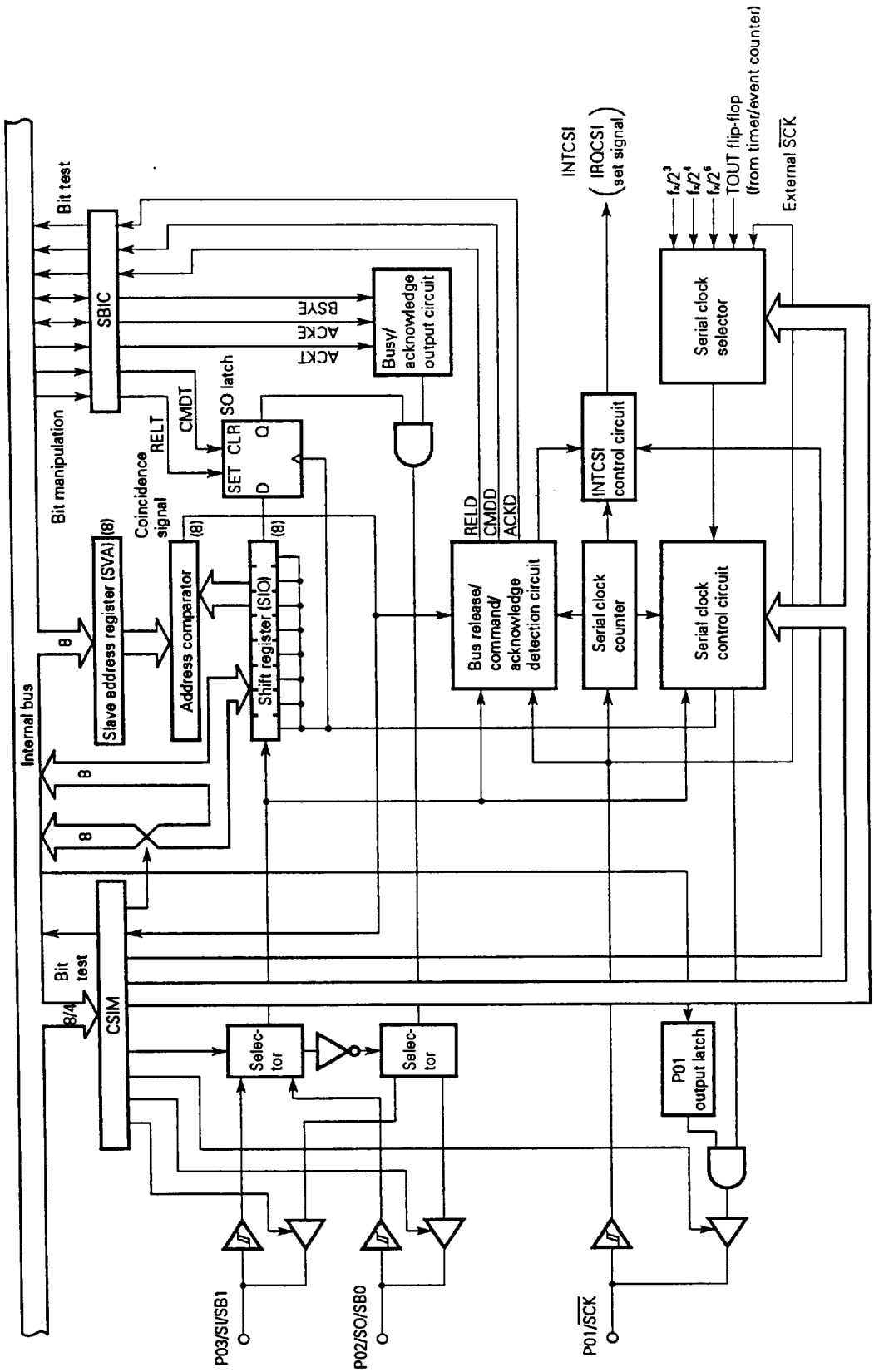


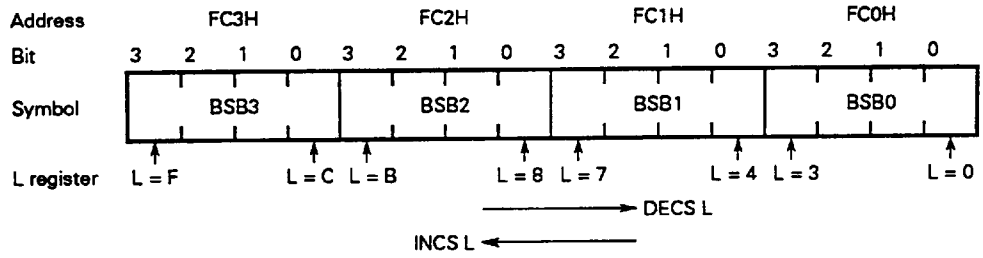
Fig. 6-8 Serial Interface Block Diagram

6.10 BIT SEQUENTIAL BUFFER: 16 BITS

The bit sequential buffer (BSB) is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially updated by bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.

This data memory consists of 16 bits so that pmem.@L addressing of the bit manipulation instruction is possible. Therefore, indirect bit specification is possible using the L register. In this case, processing can be continued by sequentially moving the specification bit through incrementing or decrementing the value of the L register within the program loop.

Fig. 6-9 Bit Sequential Buffer Format



Remarks 1. In pmem.@L addressing, bit specification is shifted according to the L register.

2. In pmem.@L addressing, the bit sequential buffer can be manipulated at any time regardless of MBE/MBS specification.

7. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

The μPD750008 has seven interrupt sources and two test sources. One test source, INT2, has two types of edge detection testable input pins.

The interrupt control circuit of the μPD750008 has the following functions.

(1) Interrupt functions

- Hardware controlled vectored interrupt function which can control whether or not to accept an interrupt using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be set arbitrarily.
- Multiple interrupt function which can specify the priority by the interrupt priority specification register (IPS)
- Test function of an interrupt request flag (IRQxxx)
  (The software can confirm that an interrupt occurred.)
- Release of the standby mode (Interrupts released by an interrupt enable flag can be selected.)

(2) Test functions

- Whether test request flags (IRQxxx) are issued can be checked with software.
- Release of the standby mode (A test source to be released can be selected with test enable flags.)

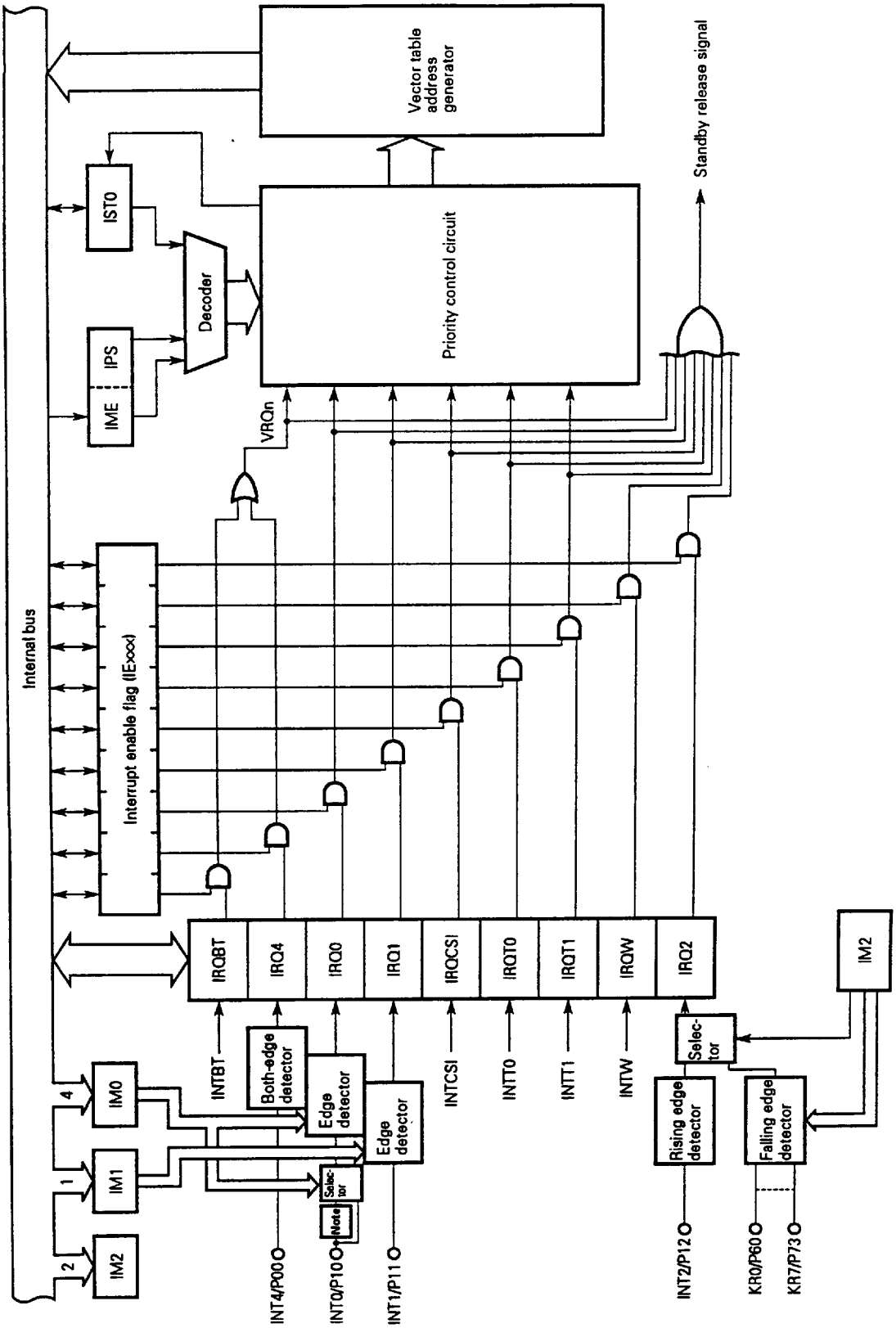


Fig. 7-1 Interrupt Control Circuit Block Diagram

Note Noise eliminator (Standby release is not possible when the noise eliminator is selected.)

8. STANDBY FUNCTION

The μPD750008 has two different standby modes (STOP mode and HALT mode) to reduce power dissipation while waiting for program execution.

Table 8-1 Standby Mode Statuses

Item \ Mode		STOP mode	HALT mode
Instruction for setting		STOP instruction	HALT instruction
System clock for setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation status	Clock oscillator	Only the main system clock stops its operation	Only the CPU clock Φ stops its operation (oscillation continues)
	Basic interval/ watchdog timer	Does not operate	Can operate only at main system clock oscillation. (IRQBT is set at reference time intervals.)
	Serial interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Can operate only when external $\overline{SCK}$ input is selected as the serial clock or at main system clock oscillation.
	Timer/event counter	Can operate only when the TI0 pin input is selected for the count clock	Can operate only when TI0 pin input is specified as the count clock or at main system clock oscillation.
	Timer/counter	Does not operate	Can operate[Note 1]
	Clock timer	Can operate when f_{XT} is selected as the count clock	Can operate
	External interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate. [Note 2]	
	CPU	Does not operate	
Release signal		An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the generation of a $\overline{RESET}$ signal	

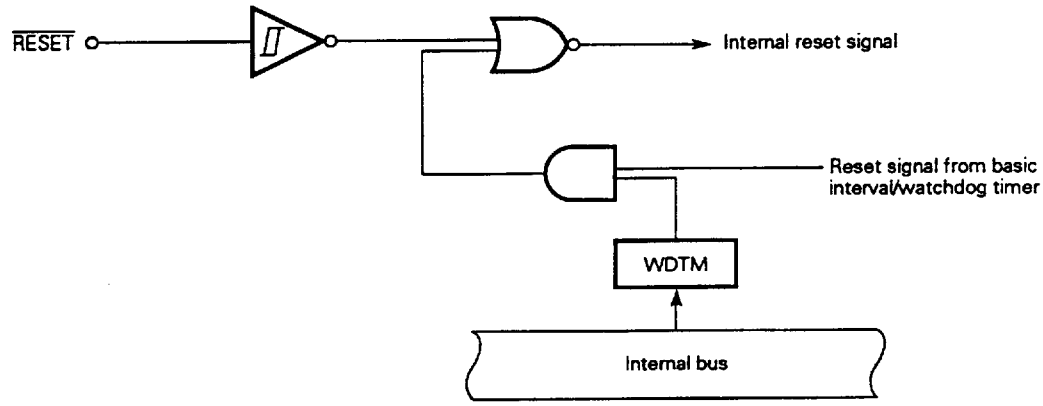
Notes 1. Operation is possible only when the main system clock operates.

2. Operation is possible only when the noise eliminator is not selected by bit 2 of the edge detection mode register (IM0) (when IM02 = 1).

9. RESET FUNCTION

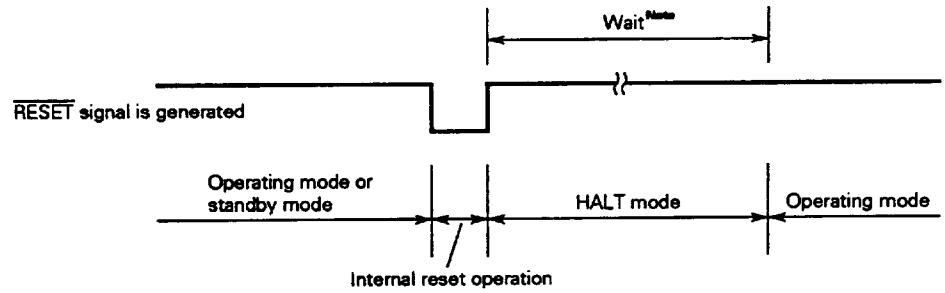
The μPD750008 is reset with the external reset signal ($\overline{\text{RESET}}$) or the reset signal received from the interval/watchdog timer. When either reset signal is input, the internal reset signal is generated. Fig. 9-1 shows the configuration of the reset circuit.

Fig. 9-1 Configuration of Reset Functions



When the $\overline{\text{RESET}}$ signal is generated, the μPD750008 is reset and all hardware is initialized as indicated in Table 9-1. Fig. 9-2 shows the reset operation timing.

Fig. 9-2 Reset Operation by Generation of $\overline{\text{RESET}}$ Signal



Note Either of the following two values can be selected by a mask option:
2^{17}/fx (21.8 ms at 6.00 MHz)
2^{15}/fx (5.46 ms at 6.00 MHz)

Table 9-1 Status of the Hardware after a Reset (1/2)

Hardware			Generation of a $\overline{\text{RESET}}$ signal in a standby mode	Generation of a $\overline{\text{RESET}}$ signal during operation
Program counter (PC)		μPD750004	4 low-order bits at address 0000H in program memory are set in PC bits 11 to 8, and the data at address 0001H are set in PC bits 7 to 0.	4 low-order bits at address 0000H in program memory are set in PC bits 11 to 8, and the data at address 0001H are set in PC bits 7 to 0.
		μPD750006, 750008	5 low-order bits at address 0000H in program memory are set in PC bits 12 to 8, and the data at address 0001H are set in PC bits 7 to 0.	5 low-order bits at address 0000H in program memory are set in PC bits 12 to 8, and the data at address 0001H are set in PC bits 7 to 0.
PSW	Carry flag (CY)		Held	Undefined
	Skip flags (SK0 to SK2)		0	0
	Interrupt status flags (IST0, IST1)		0	0
	Bank enable flags (MBE, RBE)		Bit 6 at address 0000H in program memory is set in RBE, and bit 7 is set in MBE.	Bit 6 at address 0000H in program memory is set in RBE, and bit 7 is set in MBE.
Stack pointer (SP)			Undefined	Undefined
Stack bank selection register (SBS)			1000	1000
Data memory (RAM)			Held[Note]	Undefined
General-purpose registers (X, A, H, L, D, E, B, C)			Held	Undefined
Bank selection register (MBS, RBS)			0, 0	0, 0
Basic interval/ watchdog timer	Counter (BT)		Undefined	Undefined
	Mode register (BTM)		0	0
	Watchdog timer enable flag (WDTM)		0	0
Timer/event counter	Counter (T0)		0	0
	Modulo register (TMOD0)		FFH	FFH
	Mode register (TM0)		0	0
	TOE0, TOUT flip-flop		0, 0	0, 0
Timer/counter	Counter (T1)		0	0
	Modulo registers (TMOD1)		FFH	FFH
	Mode register (TM1)		0	0
	TOE1, TOUT flip-flop		0, 0	0, 0
Clock timer	Mode register (WM)		0	0
Serial interface	Shift register (SIO)		Held	Undefined
	Operation mode register (CSIM)		0	0
	SBI control register (SBIC)		0	0
	Slave address register (SVA)		Held	Undefined

Note Data of address 0F8H to 0FDH of the data memory becomes undefined when the $\overline{\text{RESET}}$ signal is generated.

Table 9-1 Status of the Hardware after a Reset (2/2)

Hardware		Generation of a $\overline{\text{RESET}}$ signal in a standby mode	Generation of a $\overline{\text{RESET}}$ signal during operation
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Sub-oscillator control register (SOS)		0	0
Interrupt	Interrupt request flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt enable flag (IExxx)	0	0
	Priority selection register (IPS)	0	0
	INT0, INT1 and INT2 mode registers (IM0, IM1, IM2)	0, 0, 0	0, 0, 0
Digital ports	Output buffer	Off	Off
	Output latch	Clear (0)	Clear (0)
	I/O mode registers (PMGA, PMGB, PMGC)	0	0
	Pull-up resistor specification register (POGA, POGB)	0	0
Bit sequential buffers (BSB0 to BSB3)		Held	Undefined

10. INSTRUCTION SET

(1) Operand identifier and its descriptive method

The operands are described in the operand column of each instruction according to the descriptive method for the operand format of the appropriate instructions. (For details, refer to *RA75X Assembler Package User's Manual: Language* (EEU-1343).) For descriptions in which alternatives exist, one element should be selected. Capital letters and plus and minus signs are keywords; therefore, they should be described as they are.

For immediate data, the appropriate numerical values or labels should be described.

The symbols of register flags can be used as a label instead of mem, fmem, pmem, and bit. (For details, refer to *μPD750008 User's Manual* (IEU-1421).) However, there are some restrictions on usable labels for fmem and pmem.

Representation format	Description method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label[Note] 2-bit immediate data or label
fmem pmem	FB0H - FBFH, FF0H - FFFH immediate data or label FC0H - FFFH immediate data or label
addr	0000H - 0FFFH immediate data or label (μPD750004) 0000H - 17FFH immediate data or label (μPD750006) 0000H - 1FFFH immediate data or label (μPD750008)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H-7FH immediate data (however, bit 0 = 0) or label
PORTn IExxx RBn MBn	PORT0 - PORT8 IEBT, IET0, IET1, IE0 - IE2, IE4, IECSI, IEW RB0 - RB3 MB0, MB1, MB15

Note Only even address can be specified for 8-bit data processing.

(2) Symbol definitions in operation description

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Pair register (XA); 8-bit accumulator
BC	:	Pair register (BC)
DE	:	Pair register (DE)
HL	:	Pair register (HL)
XA'	:	Extended register pair (XA')
BC'	:	Extended register pair (BC')
DE'	:	Extended register pair (DE')
HL'	:	Extended register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; Bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 8)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority specification register
IExxx	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Address bit delimiter
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols used for the addressing area column

*1	MB = MBE • MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H - 7FH) MB = 15 (F80H - FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H - FBFH, FF0H - FFFH	
*5	MB = 15, pmem = FC0H - FFFH	
*6	addr = 0000H - 0FFFH (μPD750004) 0000H - 17FFH (μPD750006) 0000H - 1FFFH (μPD750008)	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H - 0FFFH (μPD750004) 0000H - 0FFFH (PC_{12} = 0 : μPD750006, 750008) 1000H - 17FFH (PC_{12} = 1 : μPD750006) 1000H - 1FFFH (PC_{12} = 1 : μPD750008)	
*9	faddr = 0000H - 07FFH	
*10	taddr = 0020H - 007FH	

Remarks 1. MB indicates the memory bank that can be accessed.
2. For *2, MB = 0 regardless of MBE and MBS settings.
3. For *4 and *5, MB = 15 regardless of MBE and MBS.
4. For *6 to *10, each addressable area is indicated.

(4) Description of machine cycle column

S indicates the number of machine cycles necessary for skipping any skip instruction. The value of S changes as follows:

- When no skip is performed ..... S = 0
- When a 1-byte or 2-byte instruction is skipped ..... S = 1
- When a 3-byte instruction[Note] is skipped ..... S = 2

Note 3-byte instruction: BR !addr, BRA !addr, CALL !addr, and CALLA !addr instructions.

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle (= t_{CY}) of the CPU clock (F), and four types of times are available for selection according to the PCC setting.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ↔ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table reference	MOVT	XA, @PCDE	1	3	• μPD750004 XA ← $(PC_{11-8} + DE)_{ROM}$		
					• μPD750006, 750008 XA ← $(PC_{12-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	• μPD750004 XA ← $(PC_{11-8} + XA)_{ROM}$		
					• μPD750006, 750008 XA ← $(PC_{12-8} + XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ Note	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ Note	*6	

Note Set register B to 0 in the μPD750004. Only the LSB is valid in register B in the μPD750006 and μPD750008.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← (H + mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← CY	*5	
		@H+mem.bit, CY	2	2	(H + mem$_{3-0}$.bit) ← CY	*1	
Arithmetic	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1 ← rp'1 – XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY ← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
		XA, rp'	2	2	XA ← XA ⊻ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ⊻ XA		
Accumulator manipulation	RORC	A	1	1	CY ← A$_0$, A$_3$ ← CY, A$_{n-1}$ ← A$_n$		
	NOT	A	2	2	A ← $\overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp'	2	2 + S	rp' ← rp' – 1		rp' = FFH

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∧ (H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ⊻ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ⊻ (H + mem$_{3-0}$.bit)	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Branch	BR	addr	—	—	• μPD750004 $PC_{11-0} \leftarrow$ addr The assembler selects the most adequate instruction from BRCB !caddr or BR $addr. • μPD750006, 750008 $PC_{12-0} \leftarrow$ addr The assembler selects the most adequate instruction from BR !addr, BRCB !caddr, or BR $addr.	*6	
		!addr	3	3	• μPD750006, 750008 $PC_{12-0} \leftarrow$ addr	*6	
		$addr	1	2	• μPD750004 $PC_{11-0} \leftarrow$ addr • μPD750006, 750008 $PC_{12-0} \leftarrow$ addr	*7	
		PCDE	2	3	• μPD750004 $PC_{11-0} \leftarrow PC_{11-8} + DE$ • μPD750006, 750008 $PC_{12-0} \leftarrow PC_{12-8} + DE$		
		PCXA	2	3	• μPD750004 $PC_{11-0} \leftarrow PC_{11-8} + XA$ • μPD750006, 750008 $PC_{12-0} \leftarrow PC_{12-8} + XA$		
		BCDE	2	3	• μPD750004 $PC_{11-0} \leftarrow$ BCDE[Note 1] • μPD750006, 750008 $PC_{12-0} \leftarrow$ BCDE[Note 2]	*6	
		BCXA	2	3	• μPD750004 $PC_{11-0} \leftarrow$ BCXA[Note 1] • μPD750006, 750008 $PC_{12-0} \leftarrow$ BCXA[Note 2]	*6	
	BRA[Note 3]	!addr	3	3	• μPD750004 $PC_{11-0} \leftarrow$ addr • μPD750006, 750008 $PC_{12-0} \leftarrow$ addr	*6	

Notes 1. Set register B to 0.

2. Only the LSB is valid in register B.

3. The shaded portion is supported in Mk II mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Branch	BRCB	!caddr	2	2	• μPD750004 $PC_{11-0} \leftarrow caddr_{11-0}$	*8	
					• μPD750006, 750008 $PC_{12-0} \leftarrow PC_{12} + caddr_{11-0}$		
Subroutine stack control	CALLA[Note]	!addr	3	3	• μPD750004 (SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, 0 PC_{11-0} ← addr, SP ← SP – 6	*6	
					• μPD750006, 750008 (SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 6		
	CALL[Note]	!addr	3	3	• μPD750004 (SP – 3) ← MBE, RBE, 0, 0 (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} PC_{11-0} ← addr, SP ← SP – 4	*6	
					• μPD750006, 750008 (SP – 3) ← MBE, RBE, 0, PC_{12} (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} PC_{12-0} ← addr, SP ← SP – 4		
				4	• μPD750004 (SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, 0 PC_{11-0} ← addr, SP ← SP – 6		
					• μPD750006, 750008 (SP – 2) ← ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP – 6		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLF[Note]	!faddr	2	2	• μPD750004 (SP – 3) ← MBE, RBE, 0, 0 (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} PC_{11-0} ← 0 + faddr, SP ← SP – 4	*9	
					• μPD750006, 750008 (SP – 3) ← MBE, RBE, 0, PC_{12} (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} PC_{12-0} ← 00 + faddr, SP ← SP – 4		
				3	• μPD750004 (SP – 2) → ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, 0 PC_{11-0} ← 0 + faddr, SP ← SP – 6		
					• μPD750006, 750008 (SP – 2) → ×, ×, MBE, RBE (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, PC_{12} PC_{12-0} ← 00 + faddr, SP ← SP – 6		
	RET[Note]		1	3	• μPD750004 PC_{11-0} ← (SP) (SP + 3) (SP + 2) MBE, RBE, 0, 0 ← (SP + 1), SP ← SP + 4		
					• μPD750006, 750008 PC_{11-0} ← (SP) (SP + 3) (SP + 2) MBE, RBE, 0, PC_{12} ← (SP + 1), SP ← SP + 4		
				3	• μPD750004 ×, ×, MBE, RBE ← (SP + 4) 0, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2), SP ← SP + 6		
					• μPD750006, 750008 ×, ×, MBE, RBE ← (SP + 4) MBE, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2), SP ← SP + 6		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	RETS[Note]		1	3 + S	• μPD750004 MBE, RBE, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 then skip unconditionally		Uncondition
					• μPD750006, 750008 MBE, 0, 0 ← PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 then skip unconditionally		
				3 + S	• μPD750004 0, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) ×, ×, MBE, RBE ← (SP + 4) SP ← SP + 6 then skip unconditionally		
					• μPD750006, 750008 0, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) ×, ×, MBE, RBE ← (SP + 4) SP ← SP + 4 then skip unconditionally		
	RETI[Note]		1	3	• μPD750004 MBE, RBE, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		Uncondition
					• μPD750006, 750008 MBE, RBE, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					• μPD750004 0, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					• μPD750006, 750008 0, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
Input/output	IN[Note]	A, PORTn	2	2	A ← PORTn (n = 0 - 8)		
		XA, PORTn	2	2	XA ← PORTn+1,PORTn (n = 4, 6)		
	OUT[Note]	PORTn, A	2	2	PORTn ← A (n = 2 - 8)		
		PORTn, XA	2	2	PORTn+1,PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		

Note When executing the IN/OUT instruction, MBE must be set to 0 or MBE and MBS must be set to 1 and 15, respectively.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	SEL	RBn	2	2	RBS ← n (n = 0 - 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI[Note]	taddr	1	3	• μPD750004 When the TBR instruction is used PC_{11-0} ← (taddr)$_{3-0}$ + (taddr + 1)	*10	
					When the TCALL instruction is used (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, 0, 0 PC_{11-0} ← (taddr)$_{3-0}$ + (taddr + 1) SP ← SP – 4		
					When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.
					• μPD750006, 750008 When the TBR instruction is used PC_{12-0} ← (taddr)$_{4-0}$ + (taddr + 1)		
					When the TCALL instruction is used (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, 0, PC12 PC_{12-0} ← (taddr)$_{4-0}$ + (taddr + 1) SP ← SP – 4		
					When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.
				3	• μPD750004 When the TBR instruction is used PC_{11-0} ← (taddr)$_{3-0}$ + (taddr + 1)	*10	
				4	When the TCALL instruction is used (SP – 6) (SP – 3) (SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, 0, 0 (SP – 2) ← ×, ×, MBE, RBE PC_{11-0} ← (taddr)$_{3-0}$ + (taddr + 1) SP ← SP – 6		
				3	When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only. TBR and TCALL instructions are assembler pseudo instructions to define tables used for GETI instructions.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	GETI[Note]	taddr	1	3	• μPD750006, 750008 When the TBR instruction is used $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$	*10	
				4	When the TCALL instruction is used $(SP - 6)\ (SP - 3)\ (SP - 4) \leftarrow PC_{11-0}$ $(SP - 5) \leftarrow 0, 0, 0, PC_{12}$ $(SP - 2) \leftarrow \times, \times, MBE, RBE$ $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ $SP \leftarrow SP - 6$		
				3	When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only. TBR and TCALL instructions are assembler pseudo instructions to define tables used for GETI instructions.

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions			Rated value	Unit
Supply voltage	V_{DD}				−0.3 to +7.0	V
Input voltage	V_{I1}	Other than ports			−0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports	Built-in pull-up resistor		−0.3 to V_{DD} + 0.3	V
			Open drain		−0.3 to +14	V
Output voltage	V_O				−0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Each pin			−10	mA
		All pins			−30	mA
Low-level output current	I_{OL} Note	Each pin		Peak value	30	mA
				rms	15	mA
		All pins		Peak value	220	mA
				rms	150	mA
Operating ambient temperature	T_A				−40 to +85	°C
Storage temperature	T_{stg}				−65 to +150	°C

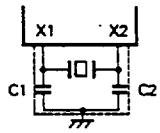
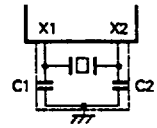
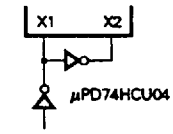
Note Calculate rms with [rms] = [peak value] $\times\sqrt{\text{duty}}$.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATOR (T_A = −40 °C to +85 °C)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator	V_{DD} = 2.2 to 5.5 V 	Oscillator frequency (f_{XX}) Note 1	V_{DD} = 2.7 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 2.2 to 2.7 V	1.0		5.0	MHz
		Oscillation settling time Note 2	After V_{DD} reaches Min. of the oscillation voltage range			4	ms
Crystal	V_{DD} = 2.7 to 5.5 V 	Oscillator frequency (f_{XX}) Note 1	2.7 V < V_{DD} ≤ 5.5 V	1.0		6.0	MHz
			V_{DD} = 2.7 V	1.0	4.19	5.0	MHz
		Oscillation settling time Note 2	V_{DD} = 5.0 V ±10%			10	ms
						30	ms
External clock	V_{DD} = 1.8 to 5.5 V 	X1 input frequency (f_X) Note 1		1.0		6.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		83.3		500	ns

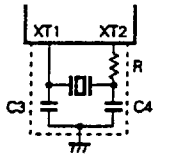
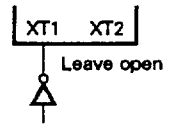
Notes 1. The oscillator frequency and X1 input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is applied or after the STOP mode is released.

Caution When the main system clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of Vss. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATOR (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation settling time Note 2	V_{DD} = 5.0 V ± 10%		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is applied.

Caution When the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions of surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of Vss. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring; the subsystem clock oscillator has low amplification to minimize current consumption and is more likely to malfunction due to noise than the main system clock oscillator.

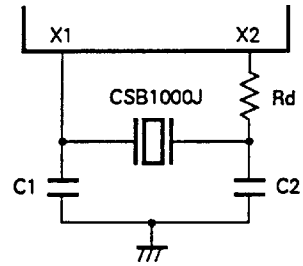
RECOMMENDED PARAMETERS FOR THE OSCILLATION CIRCUIT

When a ceramic resonator is used for the main system clock (T_A = −40 to +85 °C)

Manufacturer	Product name	Oscillation frequency (MHz)	Recommended circuit constant		Oscillation voltage range		Remarks
			C1 (pF)	C2 (pF)	Min. (V)	Max. (V)	
Murata Mfg.	CSB1000J[Note]	1.00	100	100	2.8	5.5	Rd = 4.7 kΩ
	CSA2.00MG040	2.00	100	100	2.8		
	CST2.00MG040		Incorporated	Incorporated	2.8		
	CSA4.00MG	4.00	30	30	2.8		
	CST4.00MGW		Incorporated	Incorporated	2.8		
	CSA4.00MGU		30	30	2.6		
	CST4.00MGWU		Incorporated	Incorporated	2.6		
	CSA4.19MG	4.19	30	30	2.8		
	CST4.19MGW		Incorporated	Incorporated	2.8		
	CSA4.19MGU		30	30	2.8		
	CST4.19MGWU		Incorporated	Incorporated	2.8		
	CSA6.00MGU	6.00	30	30	2.9		
	CST6.00MGWU		Incorporated	Incorporated	2.9		
	CSA6.00MG		30	30	2.7		
	CST6.00MGW		Incorporated	Incorporated	2.7		
Kyocera	KBR-1000F/Y	1.00	220	220	2.45	5.5	
	KBR-2.0MS	2.00	82	82	2.5		
	PBRC 2.00A		82	82	2.5		
	KBR-4.0MSA	4.00	33	33	2.5		
	KBR-4.0MKS		Incorporated	Incorporated	2.5		
	PBRC4.00A		33	33	2.5		
	PBRC4.00B		Incorporated	Incorporated	2.5		
	KBR-6.0MSA	6.00	33	33	2.5		
	KBR-6.0MKS		Incorporated	Incorporated	2.5		
	PBRC6.00A		33	33	2.5		
	PBRC6.00B		Incorporated	Incorporated	2.5		
TDK	FCR2.0M3	2.00	33	33	2.2	5.5	
	FCR4.0M5	4.00	15	15	2.0		
	FCR4.19M5	4.19	15	15	2.2		
	FCR6.0M5	6.00	15	15	2.5		

Note When the CSB1000J (1.00 MHz) manufactured by Murata Mfg. is used, a limiting resistor (Rd = 4.7 kΩ) is necessary (see the figure below). When one of other resonators is used, no limiting resistor is required.

Recommended sample circuit for the main system clock when the CSB1000J manufactured by Murata Mfg. is used



When a crystal is used for the subsystem clock

Manufacturer	Product name	Oscillation frequency (kHz)	Recommended circuit constant			Oscillation voltage range		Remarks	
			C3(pF)	C4(pF)	R(kΩ)	Min. (V)	Max. (V)		
Kyocera	KF-38G	32.768	10	33	220	2.7	5.5	Low-current-drain mode	T_A = -40 to +85 °C
						1.8	5.5	Low-voltage mode	
Daishinku	DT-38	32.768	10	10	220	2.7	5.5	Low-current-drain mode	T_A = -10 to +60 °C
						2.2	5.5	Low-voltage mode	

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Low-level output current	I_{OL}	Each pin					15	mA
		All pins					150	mA
High-level input voltage	V_{IH1}	Ports 2, 3, and 8		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, and 7 and $\overline{RESET}$		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	Built-in pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0.9V_{DD}		V_{DD}	V
			N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		13	V
				V_{DD} = 1.8 to 2.7 V	0.9V_{DD}		13	V
	V_{IH4}	X1, XT1			V_{DD}-0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2, 5, and 8		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, and 7 and $\overline{RESET}$		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	X1, XT1			0		0.1	V
High-level output voltage	V_{OH}	Ports 0, 2, 3, and 6 to 8 I_{OH} = −1 mA			V_{DD}-0.5			V
Low-level output voltage	V_{OL1}	Ports 0 and 2 to 8		I_{OL} = 15 mA, V_{DD} = 5.0 V ±10%		0.2	2.0	V
				I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	N-ch open drain Pull-up resistor ≥ 1 kΩ				0.2V_{DD}	V
High-level input leakage current	I_{LIH1}	V_I = V_{DD}	Other than X1 and XT1				3	μA
	I_{LIH2}		X1, XT1				20	μA
	I_{LIH3}	V_I = 13 V	Ports 4 and 5 (N-ch open drain)				20	μA
Low-level input leakage current	I_{LIL1}	V_I = 0 V	Other than X1 and XT1				−3	μA
	I_{LIL2}		X1, XT1				−20	μA
	I_{LIL3}		Ports 4 and 5 (N-ch open drain) When the input instruction is executed				−30	μA
High-level output leakage current	I_{LOH1}	V_O = V_{DD}	Other than ports 4 and 5				3	μA
	I_{LOH2}	V_O = 13 V	Ports 4 and 5 (N-ch open drain)				20	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V					−3	μA
Built-in pull-up resistor	R_{U1}	V_I = 0 V	Ports 0 to 3 and 6 to 8		50	100	200	kΩ
	R_{U2}		Ports 4 and 5		15	30	60	kΩ

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Power supply current[Note 1]	I_{DD1}	6.00 MHz[Note 2] crystal resonance C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10%[Note 3]			1.9	6.0	mA
			V_{DD} = 3.0 V ±10%[Note 4]			0.4	1.3	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 ±10%		720	2100	μA
				V_{DD} = 3.0 V ±10 %		270	800	μA
	I_{DD1}	4.19 MHz[Note 2] crystal resonance C1 = C2 = 22 pF	V_{DD} = 5.0 V ±10%[Note 3]			1.5	4.0	mA
			V_{DD} = 3.0 V ±10%[Note 4]			0.25	0.75	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ±10%		700	2000	μA
				V_{DD} = 3.0 V ±10%		230	700	μA
	I_{DD3}	32.768 kHz[Note 5] crystal resonance	Low-voltage mode	V_{DD} = 3.0 V ±10%		12	35	μA
				V_{DD} = 2.0 V ±10%		4.5	12	μA
				V_{DD} = 3.0 V T_A = 25 °C		12	24	μA
			Low-current-drain mode	V_{DD} = 3.0 V ±10%		6	18	μA
				V_{DD} = 3.0 V T_A = 25 °C		6	12	μA
	I_{DD4}		HALT mode	Low voltage mode V_{DD} = 3.0 V ±10%		8.5	25	μA
				V_{DD} = 2.0 V ±10%		3	9	μA
				V_{DD} = 3.0 V T_A = 25 °C		8.5	17	μA
				Low-current-drain mode V_{DD} = 3.0 V ±10%		3.5	12	μA
				V_{DD} = 3.0 V T_A = 25 °C		3.5	7	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5.0 V ±10%			0.05	10	μA
			V_{DD} = 3.0 V ±10%			0.02	5	μA
				T_A = 25 °C		0.02	3	μA

Notes 1. This current excludes the current which flows through the built-in pull-up resistors.

2. This value applies also when the subsystem clock oscillates.

3. Value when the processor clock control register (PCC) is set to 0011 and the μPD750008 is operated in the high-speed mode

4. Value when the PCC is set to 0000 and the μPD750008 is operated in the low-speed mode

5. This value applies when the system clock control register (SCC) is set to 1001 to stop the main system clock pulse and to start the subsystem clock pulse.

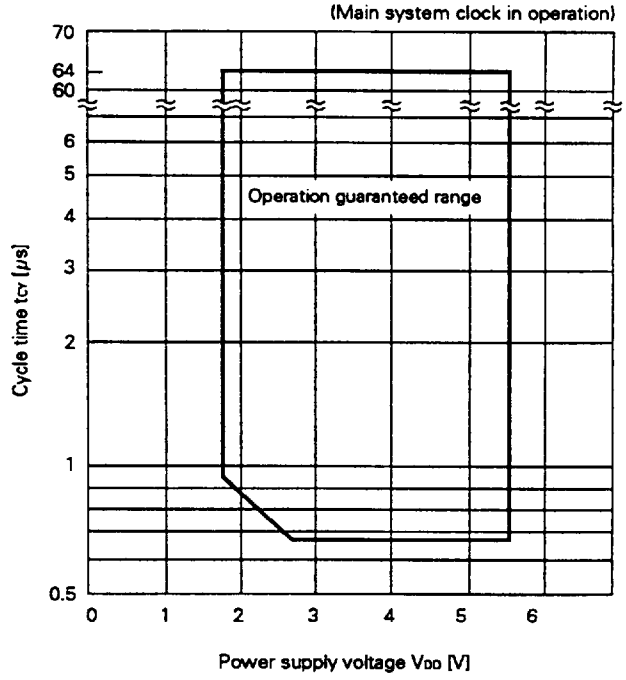
AC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operated by main system clock pulse	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operated by subsystem clock pulse		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0		Note 2			μs
		INT1, INT2, and INT4		10			μs
		KR0 to KR7		10			μs
$\overline{RESET}$ low level width	t_{RSL}			10			μs

Notes 1. The cycle time of the CPU clock (Φ) (minimum instruction execution time) depends on the connected resonator frequency, the system clock control register (SCC), and the processor clock control register (PCC).
The figure on the right side shows the cycle time t_{CY} characteristics for the supply voltage V_{DD} during main system clock operation.

2. This value becomes $2t_{CY}$ or 128/fx according to the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}
(Main system clock in operation)



Serial transfer operation

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... Internal clock output):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL1} t_{KH1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
				$t_{KCY1}/2 - 50$			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... External clock input):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL2} t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the resistance and capacitance of the SO output line load respectively.

SBI mode ($\overline{SCK}$ ... Internal clock output (master)):

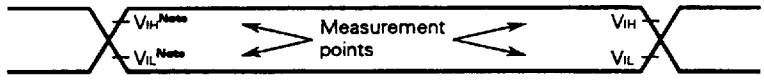
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL3}, t_{KH3}	V_{DD} = 2.7 to 5.5 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 50$			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO3}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY3}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY3}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY3}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY3}			ns

SBI mode ($\overline{SCK}$ ... External clock input (slave)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL4}, t_{KH4}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO4}	R = 1 kΩ C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY4}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY4}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY4}			ns

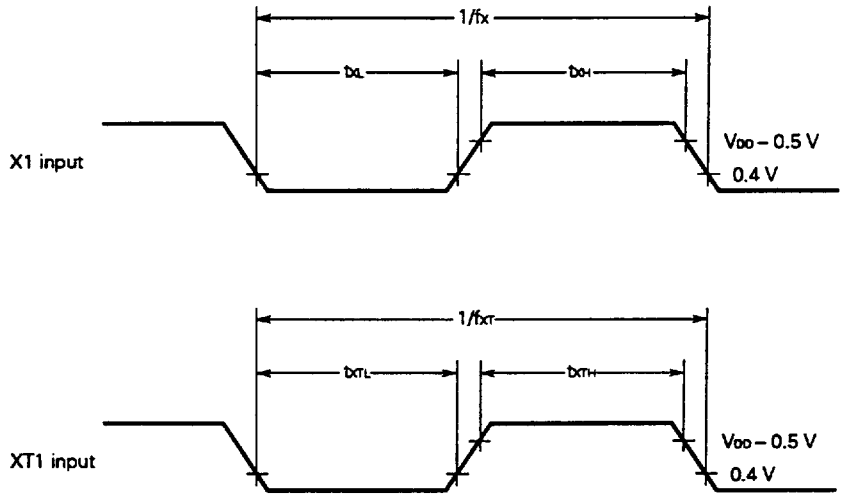
Note R and C are the resistance and capacitance of the SB0/SB1 output line load respectively.

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

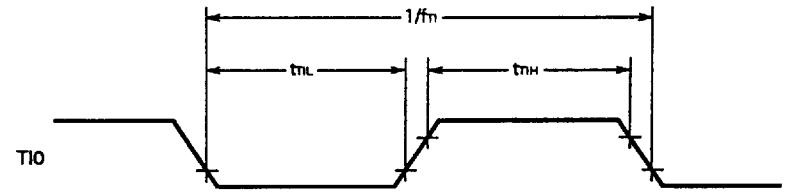


Note See **DC CHARACTERISTICS** for the values of V_{IH} and V_{IL}.

Clock Timing

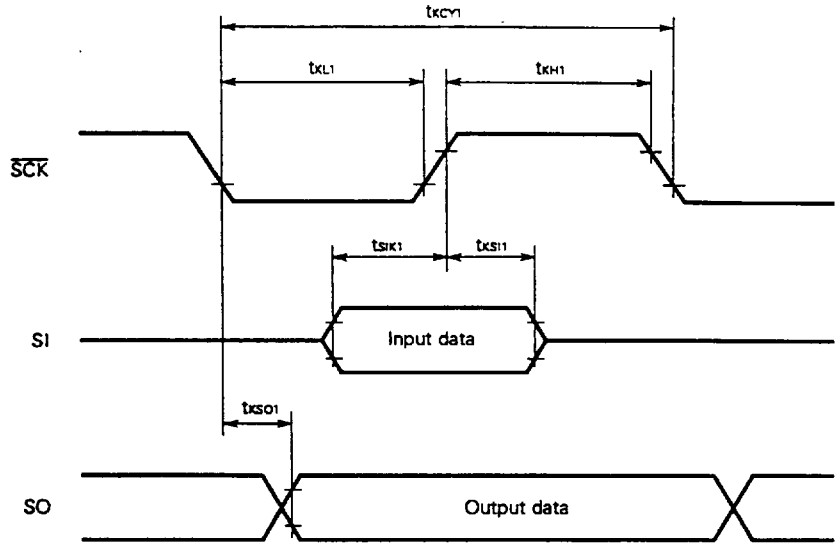


TI0 Timing

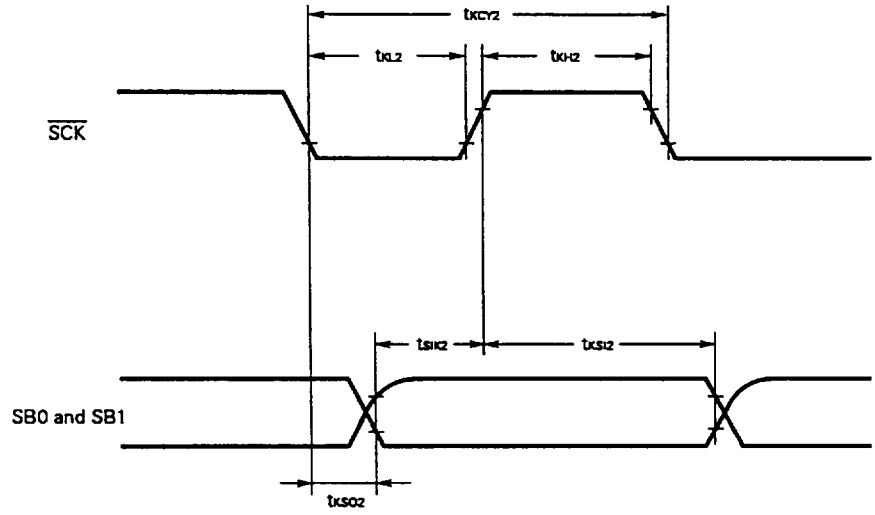


Serial Transfer Timing

Three-wire serial I/O mode:

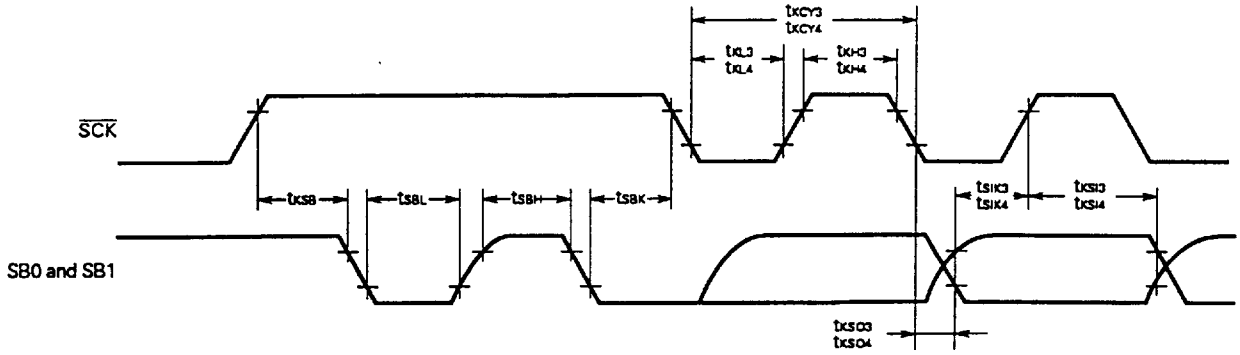


Two-wire serial I/O mode:

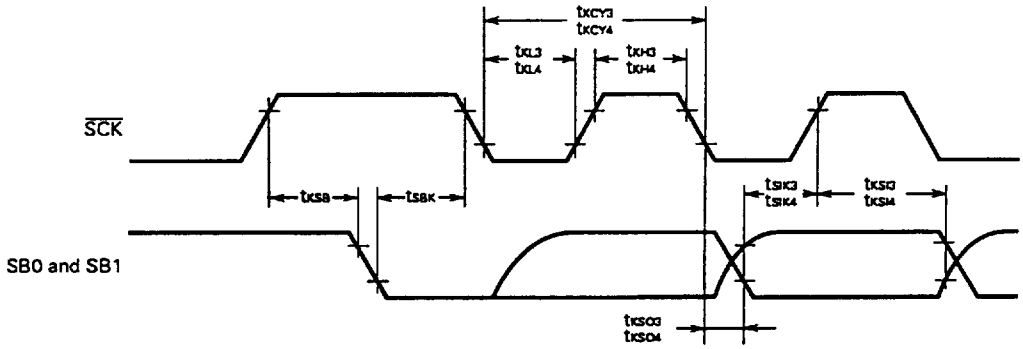


Serial Transfer Timing

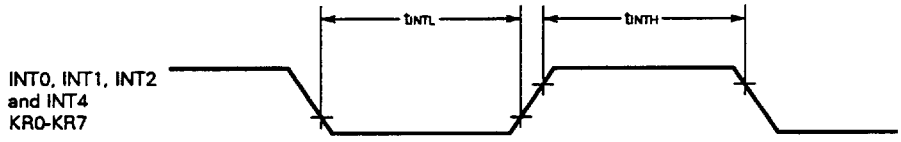
Bus release signal transfer:



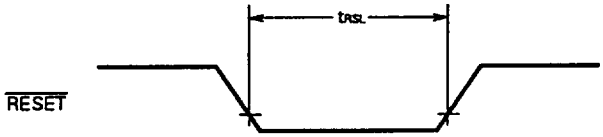
Command signal transfer:



Interrupt Input Timing



RESET Input Timing



DATA HOLD CHARACTERISTICS BY LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE
(T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Release signal setting time	t_{SREL}		0			μs
Oscillation settling time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		Note 2		ms
		Release by interrupt request		Note 3		ms

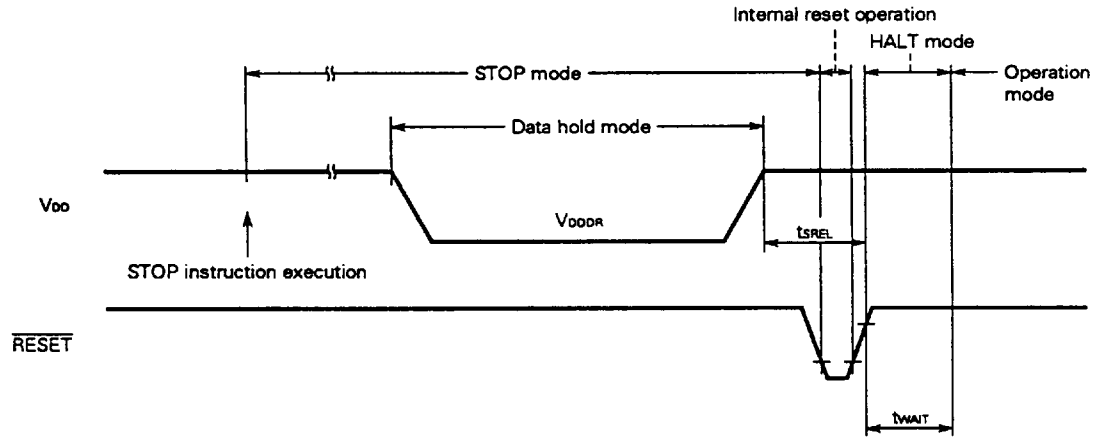
Notes 1. CPU operation stop time for preventing unstable operation at the beginning of oscillation.

2. Select either 2^{17}/fxx or 2^{15}/fxx with the mask option.

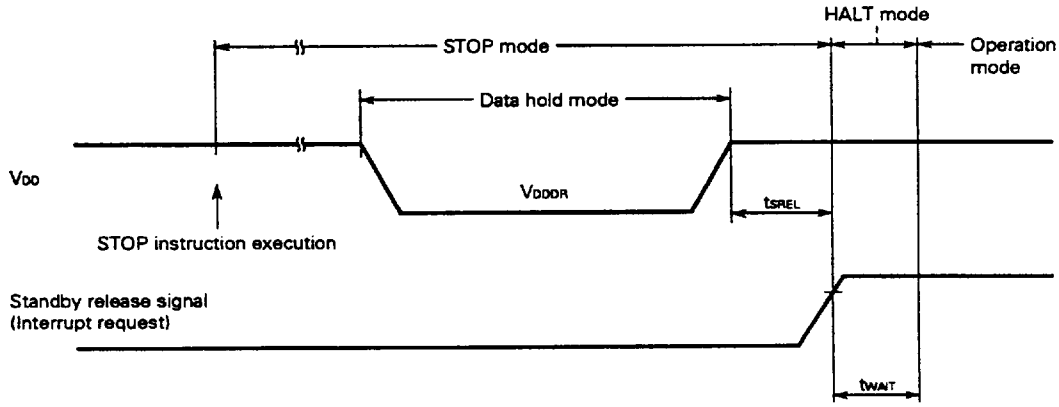
3. This value depends on the settings of the basic interval timer mode register (BTM) shown below.

BTM3	BTM2	BTM1	BTM0	Wait time (Values at fxx = 4.19 MHz in parentheses)
—	0	0	0	2^{20}/fxx (approx. 250 ms)
—	0	1	1	2^{17}/fxx (approx. 31.3 ms)
—	1	0	1	2^{15}/fxx (approx. 7.82 ms)
—	1	1	1	2^{13}/fxx (approx. 1.95 ms)

Data Hold Timing (STOP Mode Release by $\overline{RESET}$)

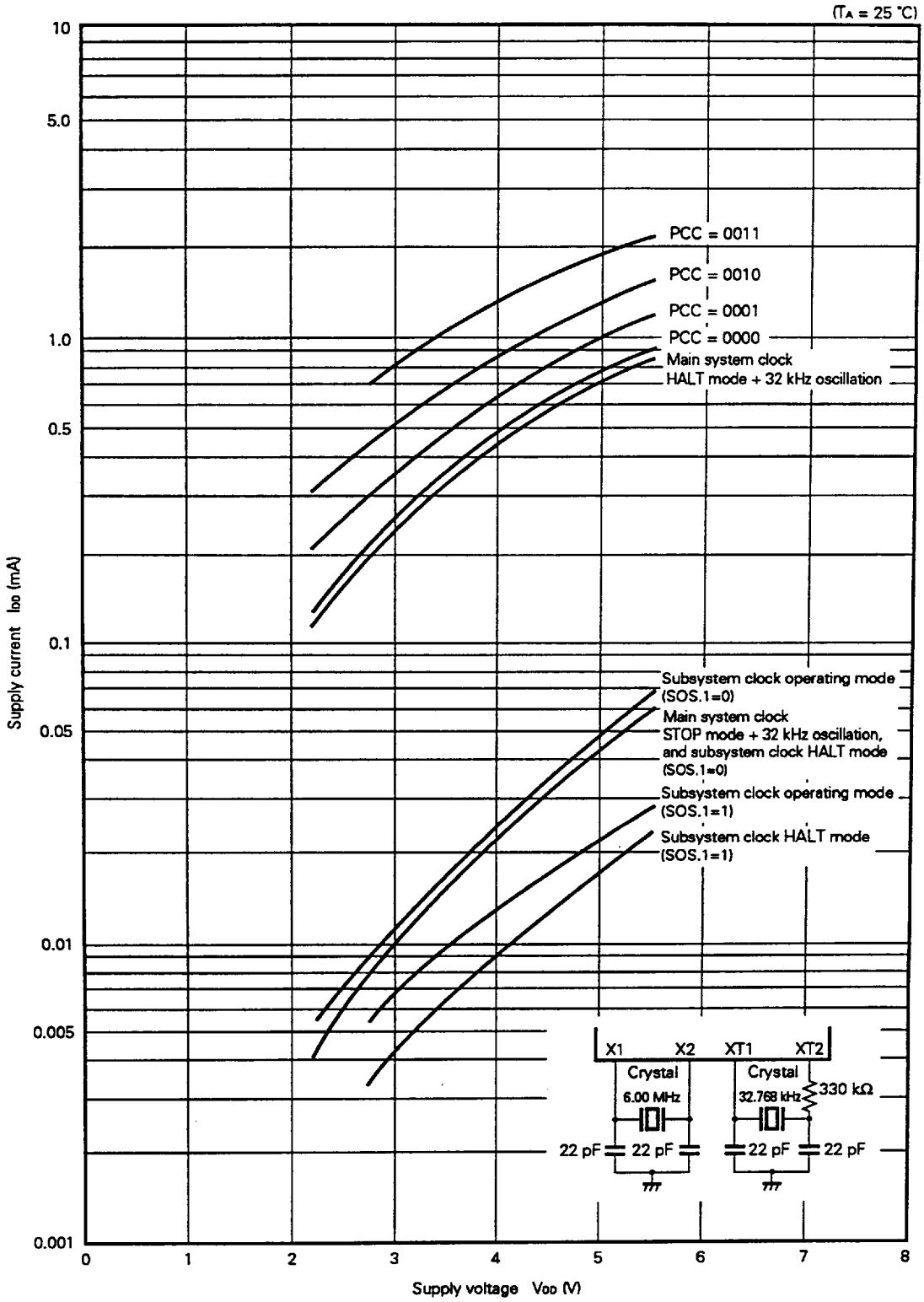


Data Hold Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

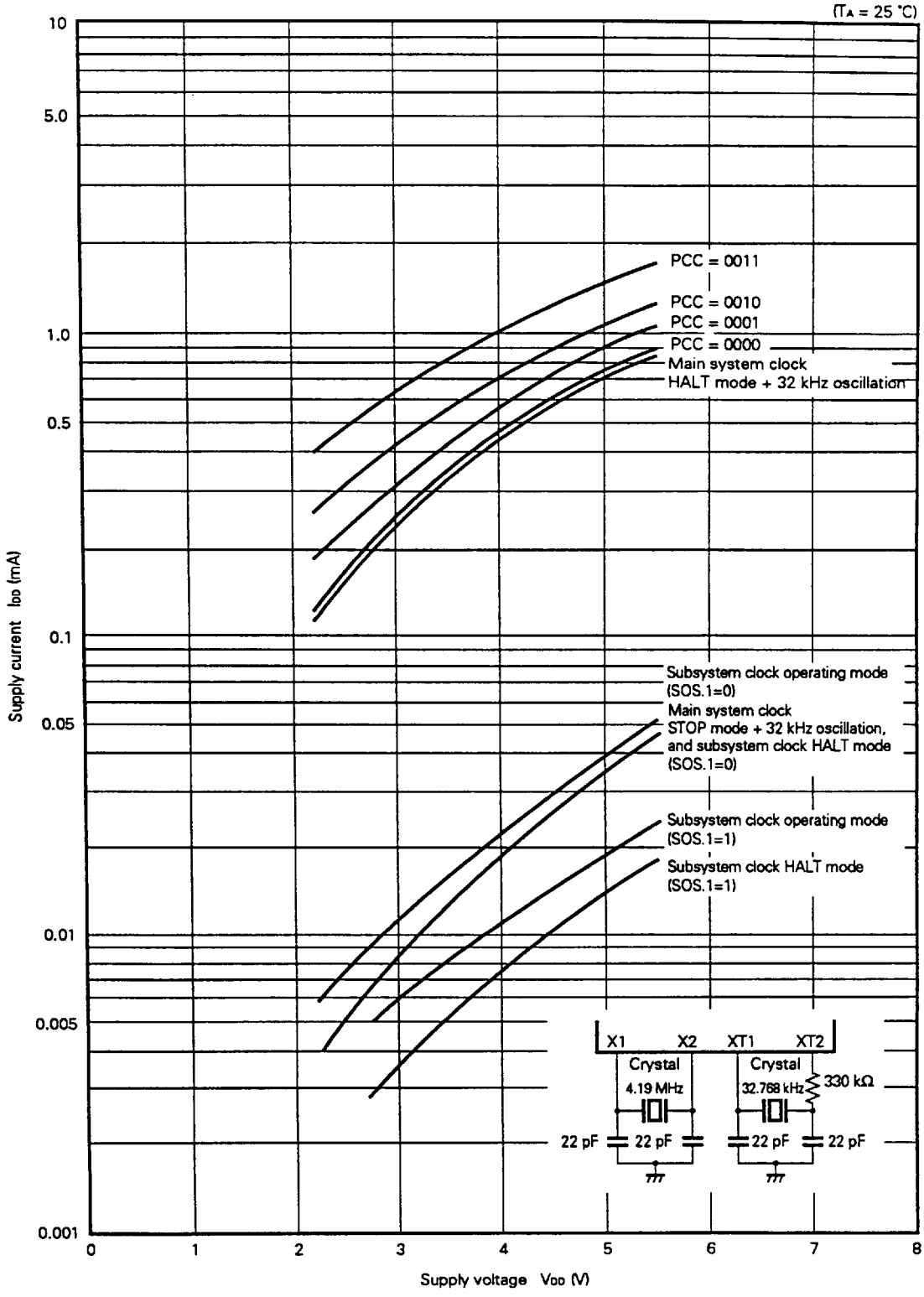


12. CHARACTERISTIC CURVE (REFERENCE VALUES)

I_{DD} vs V_{DD} (When the main system clock is operating at 6.00 MHz with a crystal)



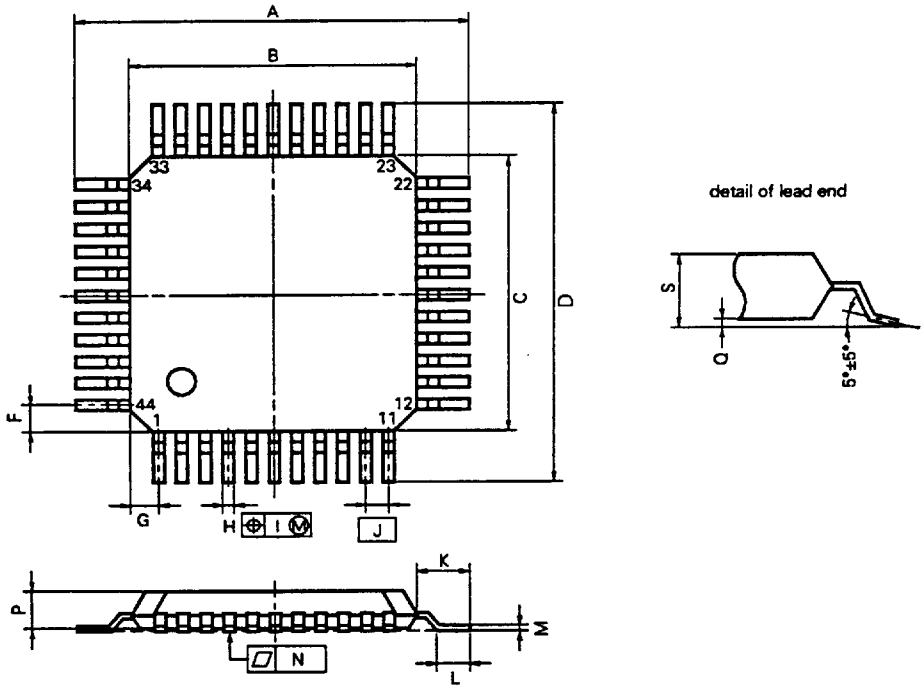
I_{DD} vs V_{DD} (When the main system clock is operating at 4.19 MHz with a crystal)



13. PACKAGE DRAWINGS

Package drawings of mass-produced products (1/2)

44 PIN PLASTIC QFP (□10)



P44GB-80-3B4-2

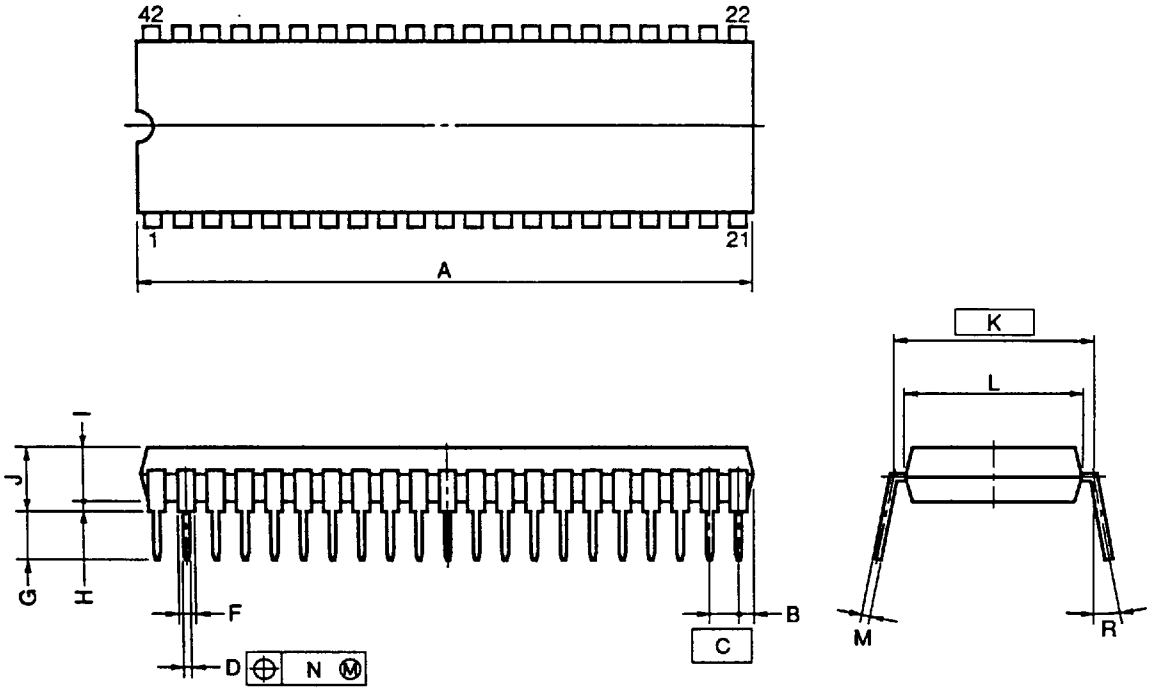
NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Caution The ES version is different from the corresponding mass-produced products in shape and material. See "ES package drawings."

Package drawings of mass-produced products (2/2)

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

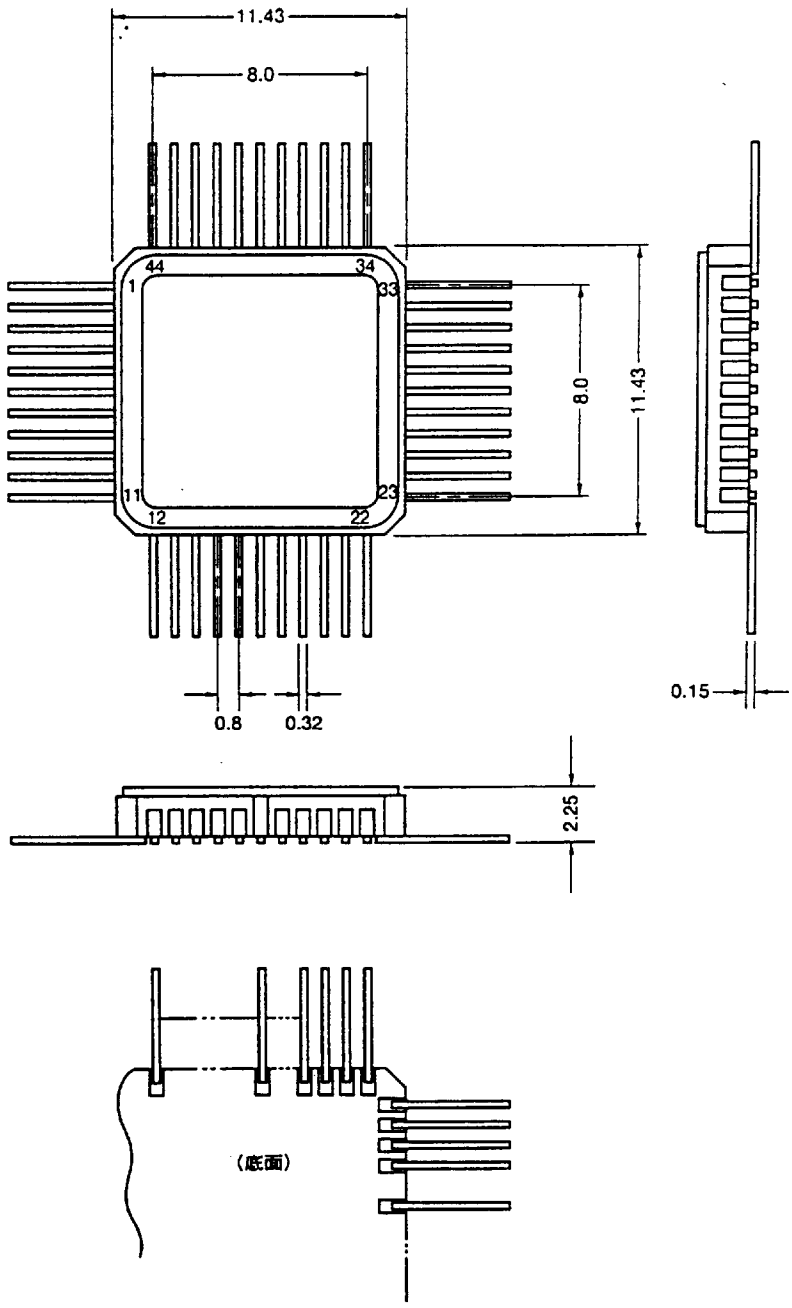
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

Caution The shape and material of the ES version are the same as those of the corresponding mass-produced products.

ES品の外形図

ES用44ピン・セラミックQFP　外形図（参考図）（単位：mm）



注意事項

1．1ピンの位置は，メタル・キャップと接続されている17ピンの位置から判断してください。

2．メタル・キャップは17ピンと接続されており，Vss（GND）レベルとなりますので注意してください。

3．リード先端の切断加工は工程管理されていませんので，リード長は規定されていません。

ES package drawing

Cautions 1. Find the location of pin 1 by checking the location of pin 17, which is connected to the metal cap.

2. The metal cap is connected to pin 17. The electrical level of the metal cap is Vss (GND).

3. The lead length has not been specified because leads are cut without any detailed specifications.

14. RECOMMENDED SOLDERING CONDITIONS

The μPD750004, μPD750006, and μPD750008 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document *SMD Surface Mount Technology Manual* (IE-1207).

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 14-1 Surface Mounting Type Soldering Conditions

μPD750004GB-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)
μPD750006GB-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)
μPD750008GB-×××-3B4 : 44-pin plastic QFP (10 × 10 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C Duration: 30 sec. max. (at 210 °C or above) Number of times: Twice max. < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C Duration: 40 sec. max. (at 200 °C or above) Number of times: Twice max. < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C max. Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering method should be avoided (except for partial heating method).

Table 14-2 Insertion Type Soldering Conditions

μPD750004CU-××× : 42-pin plastic shrink DIP (600 mil)
μPD750006CU-××× : 42-pin plastic shrink DIP (600 mil)
μPD750008CU-××× : 42-pin plastic shrink DIP (600 mil)

Soldering Method	Soldering Conditions
Wave soldering (terminal only)	Solder bath temperature: 260 °C max., Duration: 10 sec. max.
Partial heating method	Terminal temperature: 300 °C max., Duration: 3 sec. max. (for each pin)

Caution Apply wave soldering to terminals only. See to it that the jet solder does not contact with the chip directly.

APPENDIX A FUNCTIONS OF THE μPD75008, μPD750008, AND μPD75P0016

(1/2)

Item		μPD75008	μPD750008	μPD75P0016[Note]
Program memory		Masked ROM 0000H - 1F7FH (8064 × 8 bits)	Masked ROM 0000H - 1FFFH (8192 × 8 bits)	One-time PROM 0000H - 3FFFH (16384 × 8 bits)
Data memory		000H - 1FFH (512 × 4 bits)		
Instruction execution time	When selecting the main system clock	• 0.95, 1.91, 15.3 μs (when operating at 4.19 MHz)	• 0.95, 1.91, 3.81, 15.3 μs (when operating at 4.19 MHz) • 0.67, 1.33, 2.67, 10.7 μs (when operating at 6.0 MHz)	
	When selecting the subsystem clock	122 μs (when operating at 32.768 kHz)		
Pin connection	20 pins (SDIP) 38 pins (QFP)	NC	IC	V_{PP}
	24 pins (SDIP) 42 pins (QFP)	P21	P21/PTO1	
	6 - 9 pins (SDIP) 23-26 pins (QFP)	P33 - P30		P33/MD3 - P30/MD0
Stack	SBS register	Not provided	Provided	SBS.3 = 1 : Mk I mode selection SBS.3 = 0 : Mk II mode selection
	Stack area	000H - 0FFH	n00H - nFFH (n = 0, 1)	
	Stack operation for a subroutine call instruction	2-byte stack	Mk I mode: 2-byte stack Mk II mode: 3-byte stack	
Instruction	BRA !addr CALLA !addr	Not available	Mk I mode: Not available Mk II mode: Available	

	MOVT XA, @BCDE
	MOVT XA, @BCXA
	BR BCDE
	BR BCXA
			Available	

	CALL !addr	3 machine cycles	Mk I mode: 3 machine cycles, Mk II mode: 4 machine cycles	
	CALLF !faddr	2 machine cycles	Mk I mode: 2 machine cycles, Mk II mode: 3 machine cycles	
Timer		3 channels: • Basic interval timer • Timer/event counter • Clock timer	4 channels: • Basic interval/watchdog timer • Timer/event counter • Timer/counter • Clock timer	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (when the main system clock operates at 4.19 MHz)	• Φ, 524, 262, 65.5 kHz (when the main system clock operates at 4.19 MHz) • Φ, 750, 375, 93.7 kHz (when the main system clock operates at 6.0 MHz)	
BUZ output		• 2 kHz	• 2, 4, 32 kHz (when the main system clock operates at 4.19 MHz) • 2.86, 5.72, 45.8 kHz (when the main system clock operates at 6.0 MHz)	

Note Under development

(2/2)

Item		μPD75008	μPD750008	μPD75P0016[Note]
Serial interface		3 modes supported • Three-wire serial I/O mode: First transferred bit switchable between the LSB and MSB • Two-wire serial I/O mode • SBI mode		
SOS register	Feedback resistor cut flag (SOS.0)	Can incorporate feedback resistors that are specified with the mask option.	Incorporated	
	Sub-oscillator current cut flag (SOS.1)	Not provided	Incorporated	
Register bank selection register (RBS)		Not provided	Provided	
Standby release with INT0		Disable	Enable	
Number of vectored interrupts		External: 3, internal: 3	External: 3, internal: 4	
Processor clock control register		Available when PCC is 0, 2, or 3	Available when PCC is 0 to 3	
Operating power supply		2.7 to 6.0 V	2.2 to 5.5 V	★
Operating ambient temperature range		−40 to +85 °C		
Package		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 × 10 mm)		

Note Under development

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD750008:

Hardware	IE-75000-R[Note 1] IE-75001-R	In-circuit emulator for the 75XL series
	IE-75300-R-EM[Note 2]	Emulation board for the IE-75000-R and IE-75001-R
	EP-75008CU/GB-R	Emulation probe for the μPD750004CU/GB, μPD7500006CU/GB, and μPD750008CU/GB.
	PG-1500	PROM programmer
	PA-75P008CU	PROM programmer adapter for the μPD75P0016CU/GB. Connected to the PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A[Note 3]) • IBM PC/AT™ series (See "OS for IBM PC.")
	PG-1500 controller	
	RA75X relocatable assembler[Note 4]	
	DF750008 device file	

Notes 1. Maintenance service only

2. Under development
3. MS-DOS versions 5.00 and 5.00A provide a task swap function. This function, however, does not work with these software packages.
4. In the 75XL series, use the relocatable assembler common to the series together with a device file of each model. Use the DF750008 device file for the μPD750008 sub-series.

Remark For third-party development tools, refer to the *75XL Series Selection Guide* (IF-382).

OS for IBM PC

The following operating systems are supported for IBM PCs.

OS	Version
PC DOS™	Ver. 3.1 to Ver. 6.3, J6.1/V[Note] to J6.3/V[Note]
MS-DOS	Ver. 5.0 to Ver. 6.2, 5.0/V[Note] to 6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note English mode only

Caution Versions 5.00 and after of each operating system provide a task swap function. This function, however, does not work with these software packages.

APPENDIX C. RELATED DOCUMENTS

Refer to the following documents together with this manual.

The numbers listed in the tables are document numbers.

Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

Documents related to devices

Document name	Document No.	
	Japanese	English
User's Manual	IEU-884 (To be released soon)	-
75XL Series Selection Guide	IF-382	-

Documents related to development tools

	Document name		Document No.	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		EEU-951	EEU-1493
	EP-75008CU-R User's Manual		EEU-699	EEU-1317
	EP-75008GB-R User's Manual		EEU-698	EEU-1305
	PG-1500 User's Manual		EEU-651	EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual		EEU-704	EEU-1291

Other documents

Document name	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
SMD Surface Mount Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.