

1/2, 1/3 DUTY LCD DRIVER WITH KEY SCAN

■ GENERAL DESCRIPTION

The NJU6435 is a 1/2 or 1/3 duty LCD driver for segment type LCD panel with key scan function.

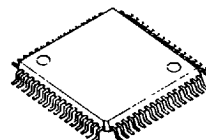
Display data and Key input data are communicated by serial data transmission, therefore, the communication between NJU6435 and MPU is performed by only 5 lines.

80-segment or 120-segment are displayed by 40-segment driver and 2- or 3-common driver.

The key scan function scanning up to 30 keys and the data is transferred to the MPU.

The NJU6435 can design simple front panel, therefore it is easy to apply car mounted audio, general audio and other products which have a display and key input.

■ PACKAGE OUTLINE



NJU6435F

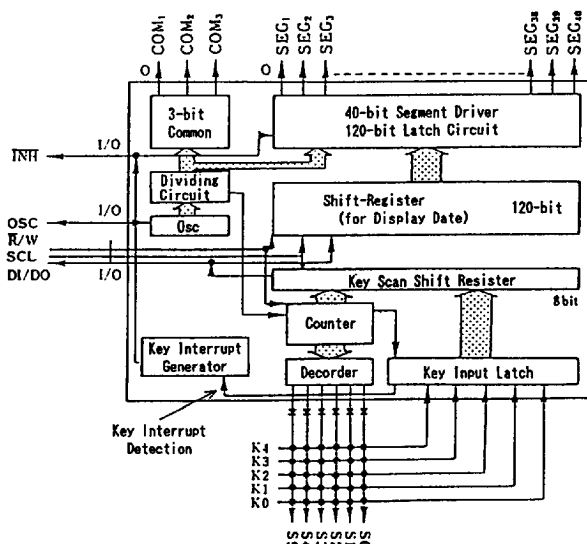
■ FEATURES

- 40-Segment Drivers
- Duty Ratio and Bias Level
 - 1/2 duty, 1/2 bias 80-Segment Drive (Version D)
 - 1/3 duty, 1/2 bias 120-segment Drive (Version E)
 - 1/3 duty, 1/3 bias 120-segment Drive (Version F)
- 30 Key Scan Function (6-out x 5-in Matrix)
- Serial Data Transmission
- Display Off Function (T_{NH} Terminal)
- Operating Voltage --- 5V±10%
- Package Outline --- QFP 64
- C-MOS Technology

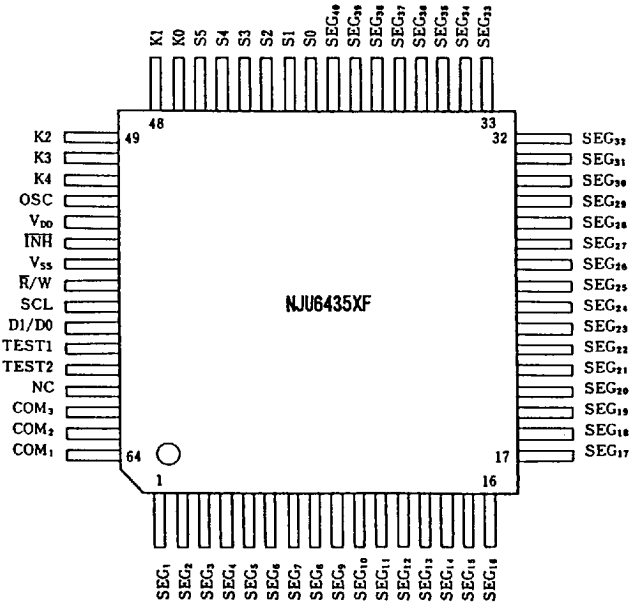
■ LINE UP

LINE UP	DUTY RATIO	BIAS LEVEL	MAX. DISPLAY SEGMENT	COMMON
NJU6435D	1/2 Duty	1/2 Bias	80 Segment	2
NJU6435E	1/3 Duty	1/2 Bias	120 Segment	3
NJU6435F	1/3 Duty	1/3 Bias	120 Segment	3

■ BLOCK DIAGRAM



PIN CONFIGURATION



TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1~40	SEG ₁ ~ SEG ₄₀	Segment Output Terminal
41~46	S0 ~ S5	Key Scanning Signal Output Terminal
47~51	K0 ~ K4	Key Scanning Input Terminal (Built-in Pull-down Resistance)
52	OSC	CR Oscillating Terminal (External C, R Connecting)
53,55	V _{DD} , V _{SS}	Power Supply
54	TNH	Display-Off Control / Key Input Interrupt Signal Output Terminal
56	R/W	Read / Write Control Terminal
57	SCL	Serial Data Transmission Clock Terminal
58	DI/DO	Serial Data Input / Output Terminal
59,60	TEST1, TEST2	Testing Terminal (Normally OPEN)
61	NC	Non Connection
62 63 64	COM ₃ COM ₂ COM ₁	Common Output Terminal. (In the Version D, COM ₃ is no active (V _{SS}))

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

Oscillation by connecting external resistor and capacitor.

This circuits supply the basical clock signal to other circuits like as common driver and segment driver and key scan circuits.

(1-2) Dividing Circuit

This circuit divide the oscillating frequency, and generate the common and segment output timing signals.

(1-3) Common Driver

Output the common driving signal for LCD.

(1-4) Segment Driver

Output the segment driving signal for LCD.

ON and OFF signal output according to the latched data.

(1-5) Shift-Register

During the $\bar{R}/W$ signal is "H", the data input to the shift-register by synchronousing the shift clock on SCL terminal.

(1-6) Counter circuit

This circuits generate key scanning timing. When the key input, the data in the counter is transferred to the key scan shift resistor.

(1-7) Decoder

Decoding the counter output and generate the key scan signal.

(1-8) Key Input Latch

When the key depressed, the decoder output is transfer to the latch.

(1-9) Key Scan Shift Register

Output the data sent from counter circuits and key input latch to the MPU by serial format through the DI/DO port.

(2) Mode of each terminal and Initialization

(2-1) Mode of each Terminal controlled by $\bar{R}/W$ signal

$\bar{R}/W$	$\overline{INH}$	DI / DO
H	LCD Display Control Mode (Input) "H" - Display ON "L" - Display Enforced OFF Key Scan is stopped	LCD Display Data Input Mode (Input) "H" - ON "L" - OFF
L	Key Scan Mode (Output) When key input, Interrupt signal Output LCD enforced off is not effective	Key Input Signal Output Mode (Output) After key interrupt signal output, key input data output from this terminal synchronized by the clock signal.

(2-2) Initialization

The NJU6435 series doesn't have a initialization function for the display data.

Therefore, the data in the Shift Register and Latch connected to the segment driver is unfixed when the power turns on.

To avoid the no meaning display, the $\bar{R}/W$ = "H" and $\overline{INH}$ = "L" status should be kept during the display data transmission from the controller to the NJU6435.

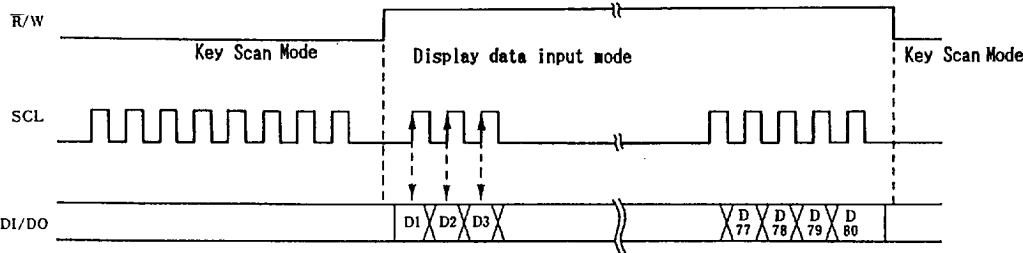
(3) Display Data Correspond to Segment Terminals

(3-1) Version D (1/2 Duty)

Data	Segment	COM ₁	COM ₂
D1	SEG ₁	○	
D2	SEG ₂	○	
D3	SEG ₃	○	
D4	SEG ₄	○	
D37	SEG ₃₇	○	
D38	SEG ₃₈	○	
D39	SEG ₃₉	○	
D40	SEG ₄₀	○	
D41	SEG ₁		○
D42	SEG ₂		○
D43	SEG ₃		○
D44	SEG ₄		○
D77	SEG ₃₇		○
D78	SEG ₃₈		○
D79	SEG ₃₉		○
D80	SEG ₄₀		○

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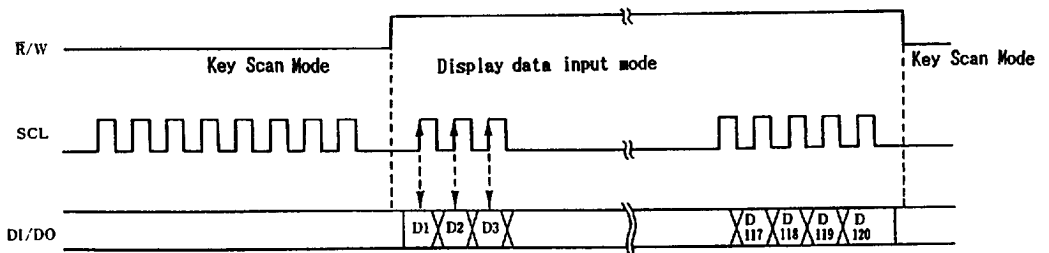
• Data Input / Output Timing



(3-2) Version E and F (1/3 Duty)

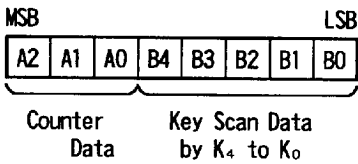
Data	Segment	COM ₁	COM ₂	COM ₃
D1	SEG ₁	○		
D2	SEG ₂	○		
D3	SEG ₃	○		
D4	SEG ₄	○		
D37	SEG ₃₇	○		
D38	SEG ₃₈	○		
D39	SEG ₃₉	○		
D40	SEG ₄₀	○		
D41	SEG ₁		○	
D42	SEG ₂		○	
D43	SEG ₃		○	
D44	SEG ₄		○	
D77	SEG ₃₇		○	
D78	SEG ₃₈		○	
D79	SEG ₃₉		○	
D80	SEG ₄₀		○	
D81	SEG ₁			○
D82	SEG ₂			○
D83	SEG ₃			○
D84	SEG ₄			○
D117	SEG ₃₇			○
D118	SEG ₃₈			○
D119	SEG ₃₉			○
D120	SEG ₄₀			○

• Data Input / Output Timing

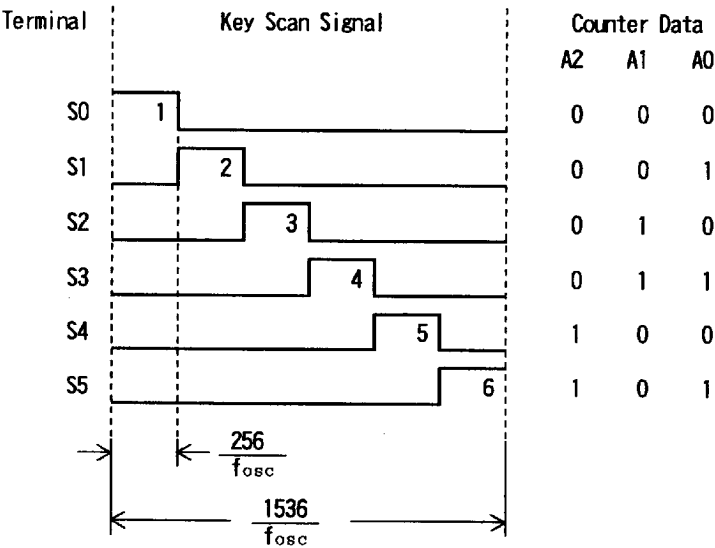


(4) Key Input Data Output Format

(4-1) Data Format

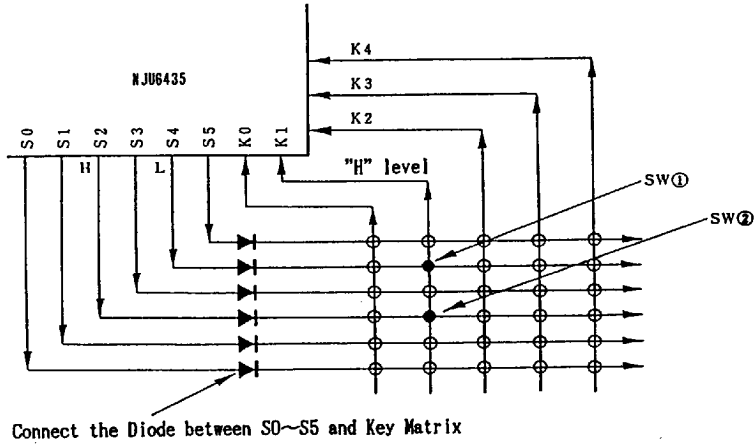


Key Scan Signal Correspond to Counter Data is as follows:



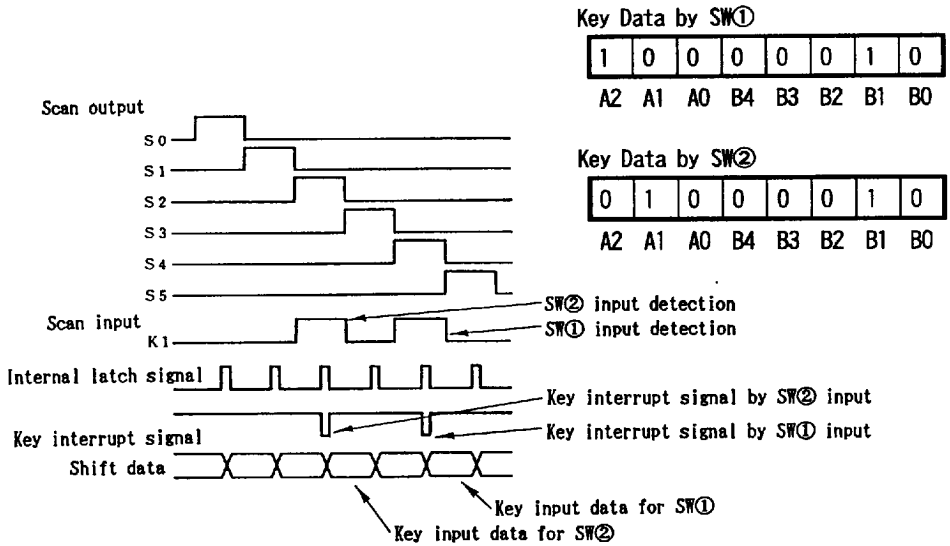
(4-2) Key Scan Output Data in Double or More Input.

In case of two or more key are depressed at same time, the output data is as follows:
Below example is mentioned SW① and SW② are depressed at once.

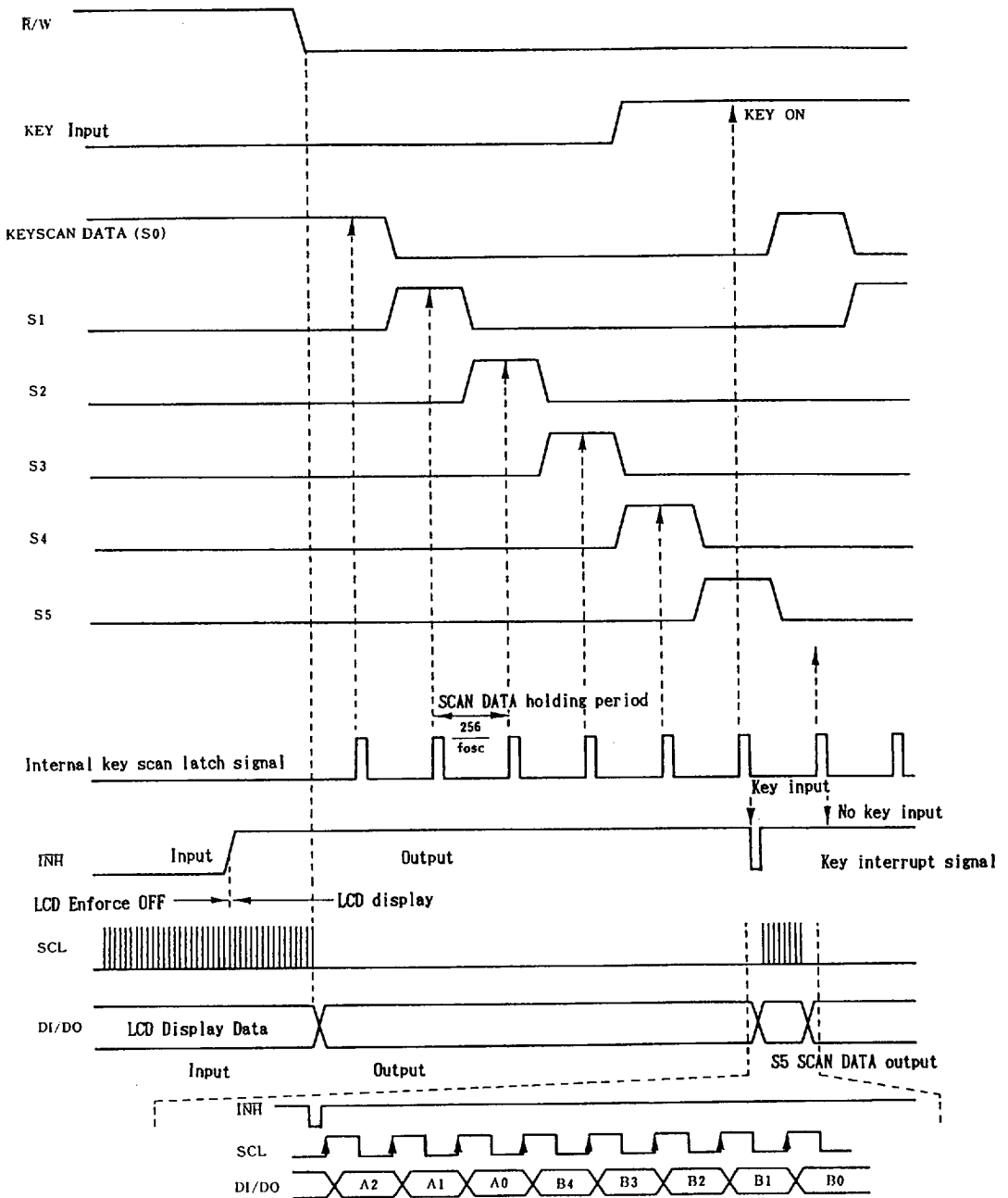


In this time, two of key scan code is output as follows:

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· Key Scan Timing Chart



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Input Voltage (1)	V_{IN}	- 0.3 ~ $V_{DD}+7.0$	V
Output Current (2)	$I_{O(1)}$	100	μA
Output Current (3)	$I_{O(2)}$	1.0	mA
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	- 30 ~ + 85	$^{\circ}C$
Storage Temperature	T_{stg}	- 55 ~ + 150	$^{\circ}C$

* 1) $\bar{R}/W, SCL, \overline{INH}, S_0 \sim S_5, DI/DO$ Terminals

* 2) $SEG_1 \sim SEG_{40}$ Terminals

* 3) COM_1, COM_2, COM_3 Terminals

ELECTRICAL CHARACTERISTICS DC Characteristics

(Ta=-20~+85°C, V_{DD}=5.0V±10%, V_{SS}=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{DD}		4.5	5.0	5.5	V
Operating Current	I _{DD}	V _{DD} Terminal			2.0	mA
"H" Input Voltage (1)	V _{IH(1)}	T _{NH} , K ₀ ~K ₄ Terminals	0.7V _{DD}			V
"H" Input Voltage (2)	V _{IH(2)}	R/W, SCL, DI/DO Terminals	0.8V _{DD}			V
"L" Input Voltage (1)	V _{IL(1)}	T _{NH} , K ₀ ~K ₄ Terminals			0.3V _{DD}	V
"L" Input Voltage (2)	V _{IL(2)}	R/W, SCL, DI/DO Terminals			0.2V _{DD}	V
"H" Input Current	I _{IH}	R/W, SCL, DI/DO, T _{NH} , K ₀ ~K ₄ Terminals			5	μA
"L" Input Current	I _{IL}	R/W, SCL, DI/DO, T _{NH} , K ₀ ~K ₄ Terminals			5	μA
"H" Output Voltage (1)	V _{OH(1)}	I _o =-40μA T _{NH} , DI/DO, S ₀ ~S ₅ Terminals	4.2			V
"H" Output Voltage (2)	V _{OH(2)}	I _o =-10μA SEG ₁ ~SEG ₄₀ Terminals	4.0			V
"H" Output Voltage (3)	V _{OH(3)}	I _o =-100μA COM ₁ ~COM ₃ Terminals	4.4			V
"L" Output Voltage (1)	V _{OL(1)}	I _o =400μA T _{NH} , DI/DO, S ₀ ~S ₅ Terminals			0.4	V
"L" Output Voltage (2)	V _{OL(2)}	I _o =10μA SEG ₁ ~SEG ₄₀ Terminals			1.0	V
"L" Output Voltage (3)	V _{OL(3)}	I _o =100μA COM ₁ ~COM ₃ Terminals			0.6	V
COM 1/2 Level Voltage	V _{MC1/2}	I _o =±100μA COM ₁ , COM ₂ Terminals 1)	1.9	2.5	3.1	V
COM 1/3 Level Voltage	V _{MC1/3}	I _o =±100μA COM ₁ ~COM ₃ Terminals 2)	1.06	1.66	2.26	V
COM 2/3 Level Voltage	V _{MC2/3}	I _o =±100μA COM ₁ ~COM ₃ Terminals 2)	2.73	3.33	3.93	V
SEG 1/3 Level Voltage	V _{MS1/3}	I _o =±10μA SEG ₁ ~SEG ₄₀ Terminals 2)	0.66	1.66	2.66	V
SEG 2/3 Level Voltage	V _{MS2/3}	I _o =±10μA SEG ₁ ~SEG ₄₀ Terminals 2)	2.33	3.33	4.33	V
External Resistance	R	OSC Terminal		51		kΩ
External Capacitance	C	OCS Terminal		680		pF
Oscillator Frequency	f _{osc}	R=51kΩ, C=680pF	40	50	60	kHz

Note 1) Version D and E

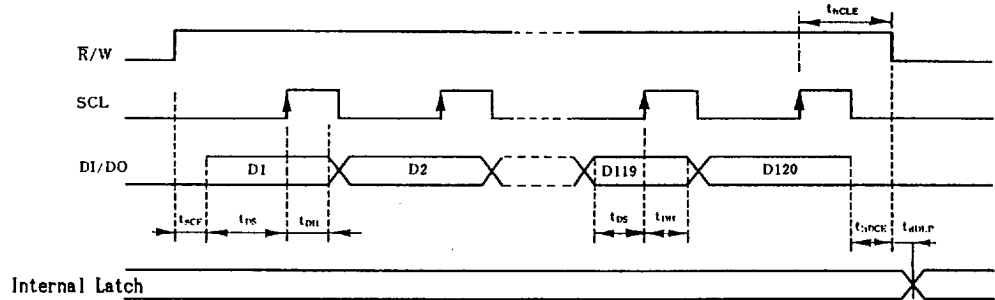
2) Version F

AC Characteristics

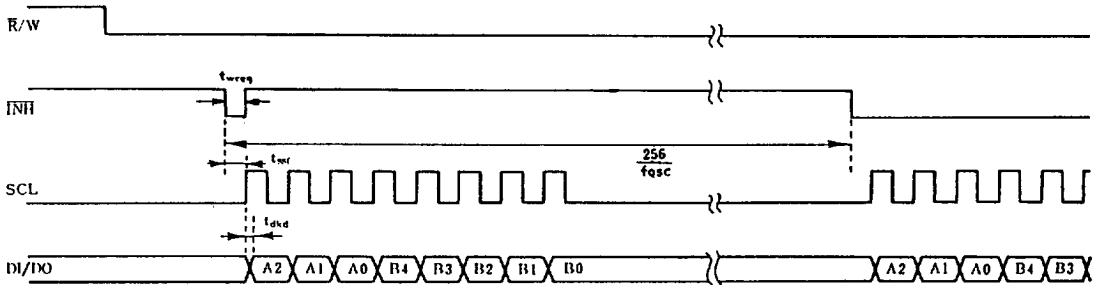
(Ta=-20~+85°C, VDD=5.0V±10%, VSS=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	tw _{CLL}	SCL Terminal	0.50			μs
"H" Clock Pulse Width	tw _{CLH}	SCL Terminal	0.50			μs
Data Set-up Time	td _S	SCL, DI/DO Terminals	0.50			μs
Data Hold Time	td _H	SCL, DI/DO Terminals	0.50			μs
CE Set-up Time	ts _{CE}	R/W, DI/DO Terminals	1.0			μs
CE Hold Time (1)	th _{DCE}	R/W, DI/DO Terminals	1.0			μs
CE Hold Time (2)	th _{CLE}	R/W, SCL Terminals	1.50			μs
Data Latch Delay Time	td _{DLP}				1.0	μs
"L" Clock Enable Pulse Width	tw _{CEL}	R/W Terminal	4.0			μs
Request Pulse Width	tw _{req}	TNH Terminal		1/f _{osc}		μs
Data Shift Set-up Time	tss _f	TNH, SCL Terminals	0.5			μs
Data Output Delay Time	td _{kd}	SCL, DI/DO Terminals	0.1			μs

Input Timing Characteristics

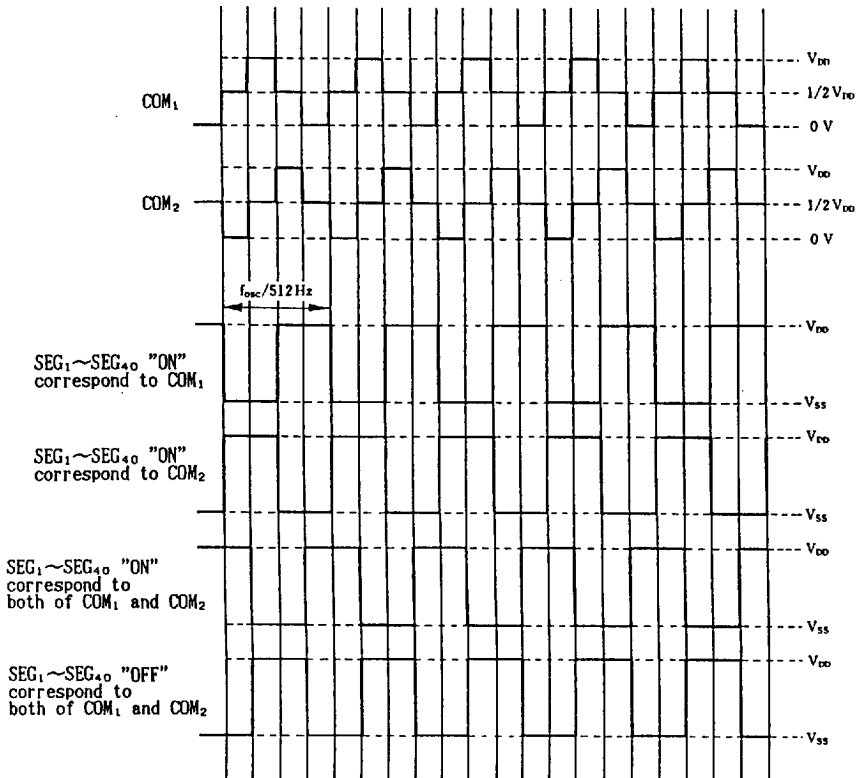


Output Timing Characteristics

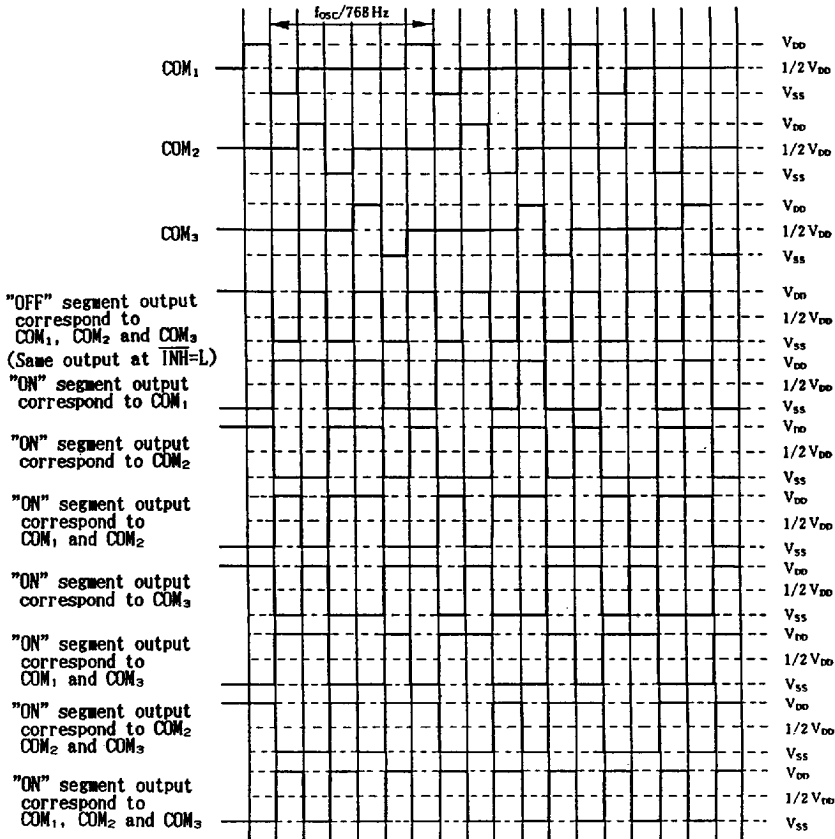


(5) LCD Driving Waveform

(5-1) Version D (1/2Bias,1/2Duty)



(5-2) Version E (1/2Bias,1/3Duty)



Timing diagram for the 74VHC163 3-bit counter. The diagram shows the clock input ($f_{osc}/768 \text{ Hz}$) and the outputs of the three counters (COM_1 , COM_2 , COM_3) over 16 clock cycles. The outputs are labeled as "OFF" segment output, "ON" segment output, and "ON" segment output. The voltage levels are indicated on the right: V_{DD} , $2/3 V_{DD}$, $1/3 V_{DD}$, V_{SS} , and V_{DD} . The diagram shows that the outputs are active-low, with "OFF" segment output being high and "ON" segment output being low.

■ APPLICATION CIRCUIT

