

8M x 64/72 One-Bank Unbuffered SDRAM Module

Features

- 168-Pin Unbuffered 8-Byte Dual In-Line Memory Module
- Intended for PC133 applications
 - Clock Frequency: 133MHz
 - Clock Cycle: 7.5ns
 - Clock Assess Time: 5.4ns
- Inputs and outputs are LVTTTL (3.3V) compatible
- Single 3.3V \pm 0.3V Power Supply
- Single Pulsed $\overline{\text{RAS}}$ interface
- SDRAMs have 4 internal banks
- Module has 1 physical bank
- Fully Synchronous to positive Clock Edge
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge commands
- Programmable Operation:
 - CAS Latency: 3
 - Burst Type: Sequential or Interleave
 - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
 - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Suspend Mode and Power Down Mode
- 12/9/2 Addressing (Row/Column/Bank)
- 4096 Refresh cycles distributed across 64ms
- Card size: 5.25" x 1.375" x 0.106"
- Gold contacts
- SDRAMs in TSOP Type II Package
- Serial Presence Detect with Write Protect

Description

IBM13N8644HCB / IBM13N8734HCB are unbuffered 168-pin Synchronous DRAM Dual In-Line Memory Modules (DIMMs) which are organized as 8Mx64 and 8Mx72 high-speed memory arrays and are configured as one 8M x 64/72 physical bank. The DIMMs use eight (8Mx64) or nine (8Mx72) 8Mx8 SDRAMs in 400mil TSOP II packages. The DIMMs achieve high-speed data transfer rates of up to 133MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK2). Internal operating modes are defined by combinations of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{S0/S2}}$, DQMB, and CKE0 signals. A command decoder initiates the necessary timings

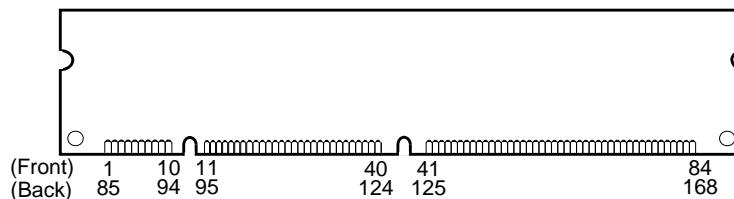
for each operation. A 14-bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any Access operation, the $\overline{\text{CAS}}$ latency, burst type, burst length, and Burst operation type must be programmed into the DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 168-pin DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products include both EDO DRAM and SDRAM unbuffered DIMMs in both non-parity x64 and ECC-Optimized x72 configurations.

Card Outline





Pin Description

CK0, CK2	Clock Inputs	DQ0 - DQ63	Data Input/Output
CK1, CK3	Unused (terminated) Clock Inputs	CB0 - CB7	Check Bit Data Input/Output
CKE0	Clock Enable	DQMB0 - DQMB7	Data Mask
\overline{RAS}	Row Address Strobe	V_{DD}	Power (3.3V)
\overline{CAS}	Column Address Strobe	V_{SS}	Ground
\overline{WE}	Write Enable	NC	No Connect
$\overline{S0}, \overline{S2}$	Chip Selects	SCL	Serial Presence Detect Clock Input
A0 - A9, A11	Address Inputs	SDA	Serial Presence Detect Data Input/Output
A10 /AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0, BA1	SDRAM Bank Address Inputs	WP	Serial Presence Detect Write Protect Input

Pinout

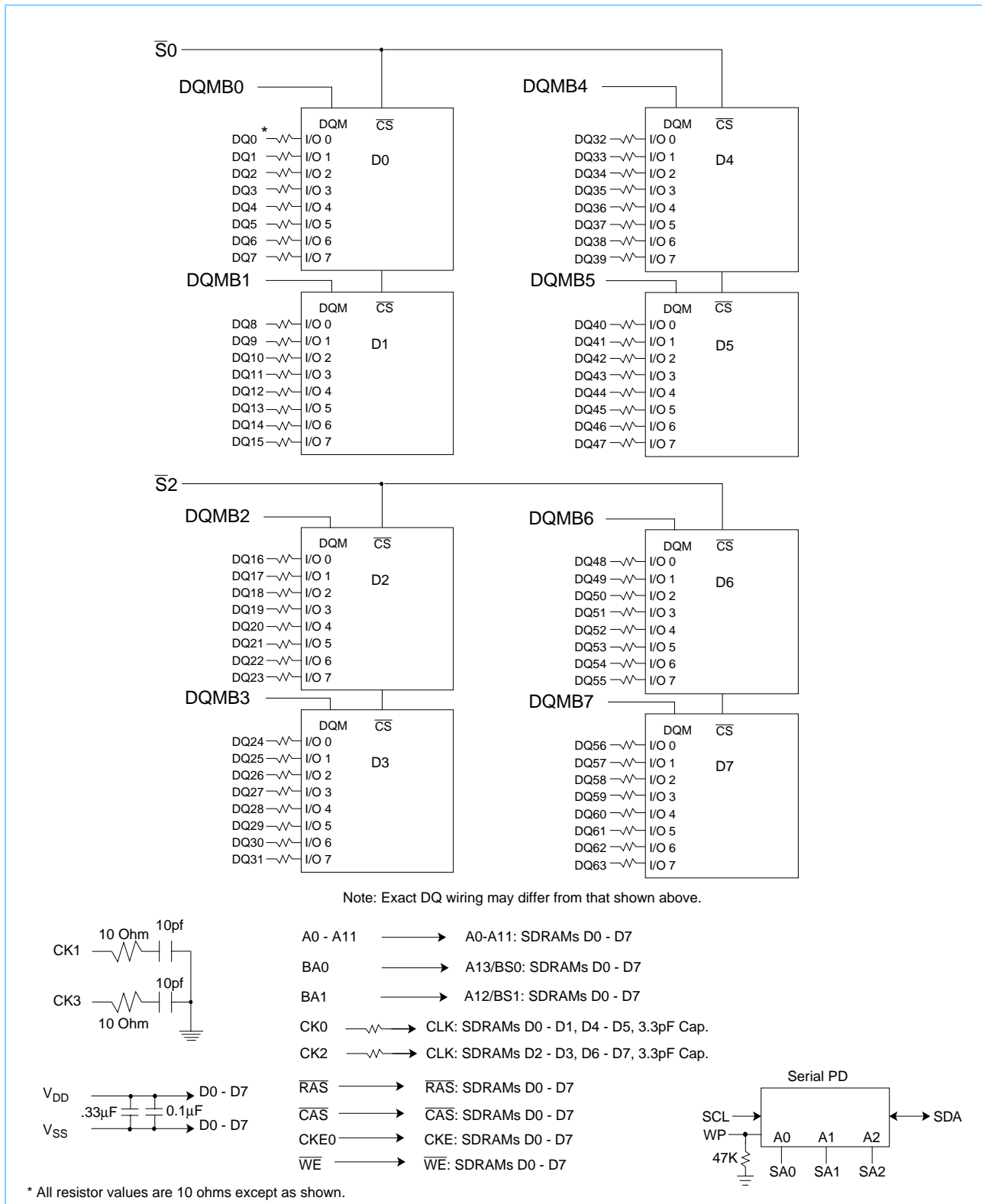
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S2}$	129	NC	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	\overline{WE}	111	\overline{CAS}	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S0}$	114	NC	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	\overline{RAS}	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	*CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	BA1	123	A11	60	DQ20	144	DQ52	81	WP	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	*CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	NC	63	NC	147	NC	84	V_{DD}	168	V_{DD}

Note: All pin assignments are consistent for all 8-byte unbuffered versions. Check bits (CB0 - CB7) are applicable only to the x72 DIMM; for the x64 DIMM these pins are no connects (NC). *CK1 and CK3 are terminated.

Ordering Information

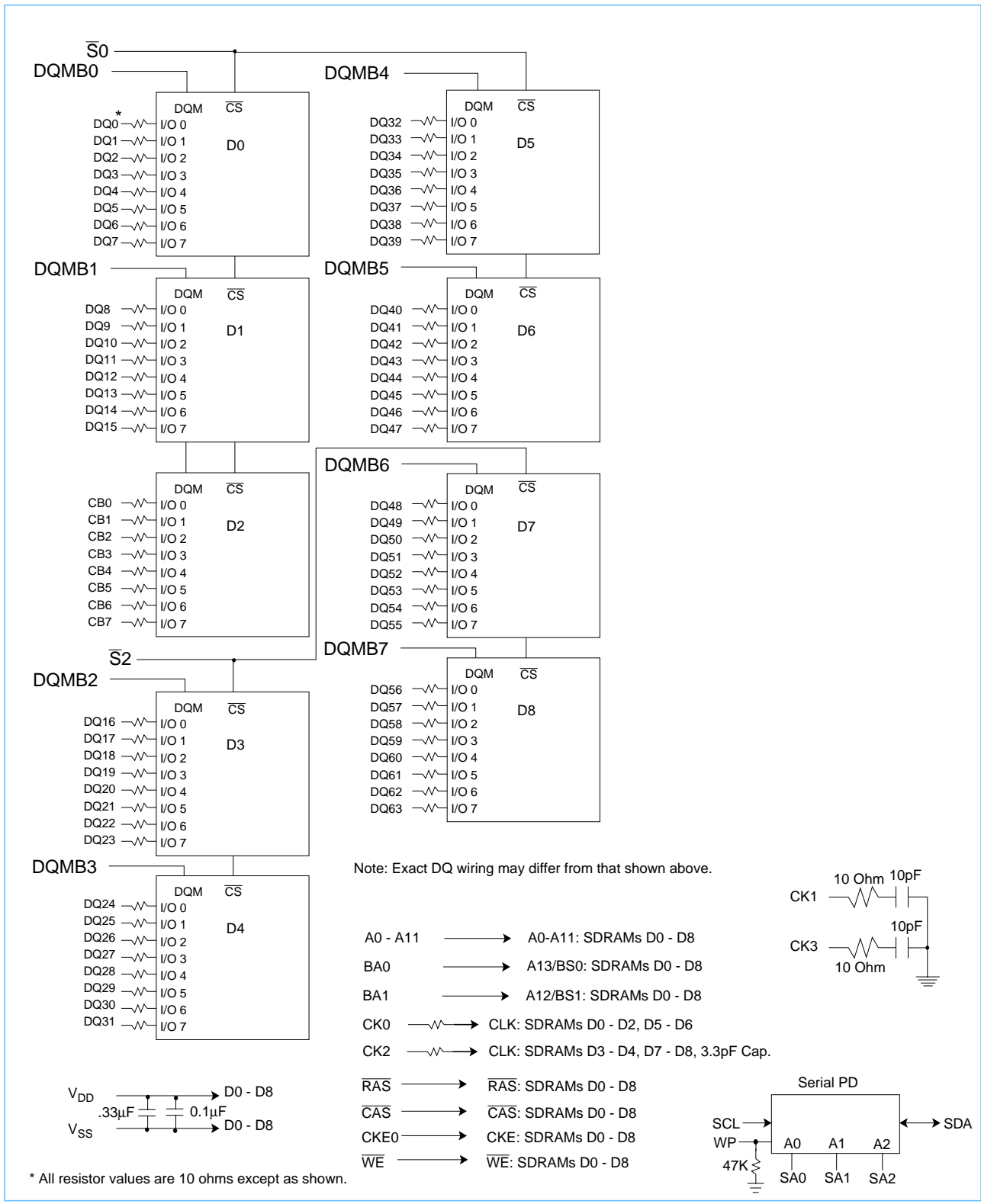
Part Number	Organization	Clock Cycle	Leads	Dimension	Power	Notes
IBM13N8644HCB-75AT	8Mx64	7.5ns	Gold	5.25" x 1.375" x 0.106"	3.3V	1
IBM13N8734HCB-75AT	8Mx72					
IBMB3N8644HCB -75AT	8Mx64					
IBMB3N8734HCB -75AT	8Mx72					

- Functionally equivalent assembly to IBM13N8644HCB and IBM13N8734HCB, manufactured using SDRAMs from a SDRAM technology licensee. SPD data reflects the IBM13N8644HCB and IBM13N8734HCB part numbers.

8Mx64 SDRAM DIMM Block Diagram (1 Bank, 8Mx8 SDRAMs)




8Mx72 SDRAM DIMM Block Diagram (1 Bank, 8Mx8 SDRAMs)



Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0, CK2	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0	Input	Level	Active High	Activates the CK0 and CK2 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0}, \overline{S2}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}, \overline{CAS}, \overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, \overline{CAS} , \overline{RAS} , and \overline{WE} define the operation to be executed by the SDRAM.
BA0, BA1	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A8 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	Level	—	Data and Check Bit Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
SA0 - SA2	Input	Level	—	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	Input Output	Level	—	Serial Data. Bidirectional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pull-up resistor is required on the system board.
SCL	Input	Pulse	—	Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the "high" state, a pull-up resistor is recommended on the system board.
WP	Input	Level	Active High	Hardware Write Protect. When WP is active, writing to the EEPROM array is inhibited. On the DIMM, this input is connected to the EEPROM Write Protect input and is also tied to ground through a 47K ohm pull-down resistor.
V_{DD}, V_{SS}	Supply			Power and ground for the module.



Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes	
0	Number of Serial PD Bytes Written during Production	128	80		
1	Total Number of Bytes in Serial PD device	256	08		
2	Fundamental Memory Type	SDRAM	04		
3	Number of Row Addresses on Assembly	12	0C		
4	Number of Column Addresses on Assembly	9	09		
5	Number of DIMM Banks	1	01		
6 - 7	Data Width of Assembly	8M x 64	x64	4000	
		8M x 72	x72	4800	
8	Voltage Interface Level of this Assembly	LVTTTL	01		
9	SDRAM Device Cycle Time at CL=3	7.5ns	75		
10	SDRAM Device Access Time from Clock at CL=3	5.4ns	54	1	
11	DIMM Configuration Type	8M x 64	Non-Parity	00	
		8M x 72	ECC	02	
12	Refresh Rate/Type	SR/1x(15.625us)	80		
13	Primary SDRAM Device Width	x8	08		
14	Error Checking SDRAM Device Width	8M x 64	N/A	00	
		8M x 72	x8	08	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01		
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F		
17	SDRAM Device Attributes: Number of Device Banks	4	04		
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	2, 3	06		
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	0	01		
20	SDRAM Device Attributes: $\overline{\text{WE}}$ Latency	0	01		
21	SDRAM Module Attributes	Unbuffered	00		
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Precharge All, Auto-Precharge, $V_{DD} \pm 10\%$	0E		
23	Minimum Clock Cycle at CL=2	15.0ns	F0		
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2	9.0ns	90	1	
25	Minimum Clock Cycle Time at CL=1	N/A	00		
26	Maximum Data Access Time (t_{AC}) from Clock at CL=1	N/A	00		
27	Minimum Row Precharge Time (t_{RP})	20ns	14		
28	Minimum Row Active to Row Active delay (t_{RFD})	15ns	0F		
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD})	20ns	14		
30	Minimum $\overline{\text{RAS}}$ Pulse width (t_{RAS})	45ns	2D		
31	Module Bank Density	64MB	10		
32	Address and Command Setup Time Before Clock	1.5ns	15		
33	Address and Command Hold Time After Clock	0.8ns	08		
34	Data Input Setup Time Before Clock	1.5ns	15		
35	Data Input Hold Time After Clock	0.8ns	08		
36 - 61	Reserved	Undefined	00		
62	SPD Revision	2	02		

1. See the AC output load circuit in the AC Characteristics section below
2. cc = Checksum Data byte, 00-FF (Hex)
3. "R" = Alphanumeric revision code, A-Z, 0-9
4. rr = ASCII coded revision code byte "R"
5. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex)
6. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex)
7. ss = Serial number data byte, 00-FF (Hex)
8. For PC-100 applications only.



Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
63	Checksum for bytes 0 - 62	Checksum Data	cc	2
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	8M x 64, -75A ASCII '13N8644HC"R"-75AT'	31334E383634344843rr 2D37354154202020	3, 4
		8M x 72, -75A ASCII '13N8734HC"R"-75AT'	31334E383733344843rr 2D37354154202020	
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	5, 6
95 - 98	Module Serial Number	Serial Number	ssssssss	7
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	100 MHz	64	8
127	Attributes for Clock Frequency defined in byte 126	CK0, CK2, CL3, concurrent AP	A5	8
128 - 255	Open for Customer Use	Undefined	00	

1. See the AC output load circuit in the AC Characteristics section below
 2. cc = Checksum Data byte, 00-FF (Hex)
 3. "R" = Alphanumeric revision code, A-Z, 0-9
 4. rr = ASCII coded revision code byte "R"
 5. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex)
 6. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex)
 7. ss = Serial number data byte, 00-FF (Hex)
 8. For PC-100 applications only.



Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SDRAM Devices	-0.3 to $V_{DD}+0.3$		
		Serial PD Device	-0.3 to +6.5		
V_{OUT}	Output Voltage	SDRAM Devices	-0.3 to $V_{DD}+3.3$		
		Serial PD Device	-0.3 to +6.5		
T_A	Operating Temperature (ambient)		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation	x64	4.2	W	1
		x72	4.7		
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A= 0$ to 70°C)

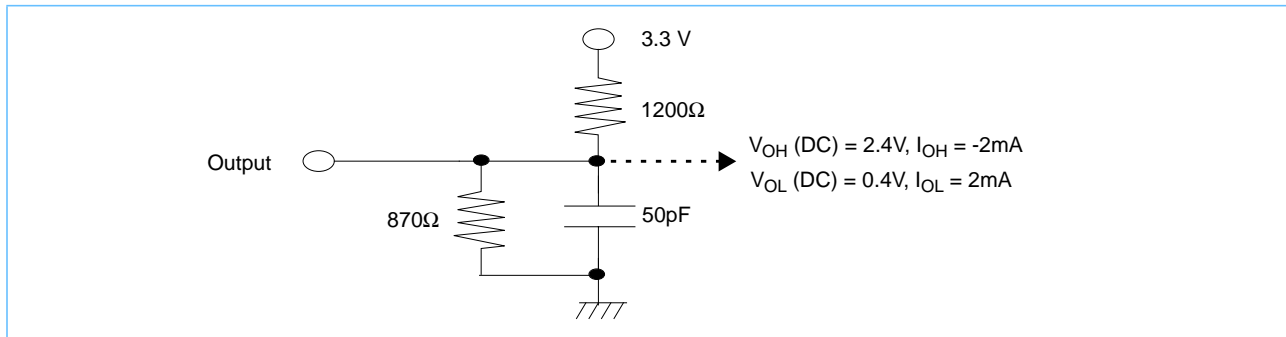
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	$V_{DD} + 0.3$	V	1, 2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 3

1. All voltages referenced to V_{SS} .
2. $V_{IH}(\text{max}) = V_{DD} + 1.2\text{V}$ for pulse width $\leq 5\text{ns}$.
3. $V_{IL}(\text{min}) = V_{DD} - 1.2\text{V}$ for pulse width $\leq 5\text{ns}$.

Capacitance ($T_A= 25^{\circ}\text{C}$, $f=1\text{MHz}$, $V_{DD}= 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Organization		Units
		x64 Max.	x72 Max.	
C_{11}	Input Capacitance (A0 - A9, A10/AP, A11, BA0, BA1, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	74	77	pF
C_{12}	Input Capacitance (CKE0)	54	58	pF
C_{13}	Input Capacitance ($\overline{\text{S0}}$, $\overline{\text{S2}}$)	30	33	pF
C_{14}	Input Capacitance (CK0 - CK3)	40	40	pF
C_{15}	Input Capacitance (DQMB0 - DQMB7)	17	21	pF
C_{16}	Input Capacitance (SA0 - SA2, SCL, WP)	9	9	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	10	10	pF
C_{IO2}	Input/Output Capacitance (SDA)	11	11	pF

DC Output Load Circuit



Output Characteristics $(T_A = 0 \text{ to } +70^\circ\text{C}, V_{DD} = 3.3V \pm 0.3V)$

Symbol	Parameter	x64		x72		Units	Notes	
		Min.	Max.	Min.	Max.			
$I_{I(L)}$	Input Leakage Current, any input $(0.0V \leq V_{IN} \leq V_{DD})$, All Other Pins Not Under Test = 0V	RAS, CAS, WE, CKE0, A0-A9, A10/AP, A11, BA0, BA1	-40	+40	-45	+45	μA	
		CK0	-20	+20	-25	+25		
		CK2	-20	+20	-20	+20		
		$\overline{S}0$	-20	+20	-25	+25		
		$\overline{S}2$	-20	+20	-20	+20		
		DQMB1	-5	+5	-10	+10		
		DQMB0, 2, 3, 4, 5, 6, 7	-5	+5	-5	+5		
		DQ0 - 63	-5	+5	-5	+5		
		CB0 - 7	0	0	-5	+5		
		SA0, SA1, SA2, SCL, SDA	-10	+10	-10	+10		
		WP	-10	+50	-10	+50		
$I_{O(L)}$	Output Leakage Current $(D_{OUT}$ is disabled, $0.0V \leq V_{OUT} \leq V_{DD})$	DQ0 - 63	-5	+5	-5	+5	μA	
		CB0 - 7	0	0	-5	+5		
V_{OH}	Output Level (LVTTTL) Output "H" Level Voltage $(I_{OUT} = -2.0mA)$	SDA	-10	+10	-10	+10	V	1
			2.4	-	2.4	-		
V_{OL}	Output Level (LVTTTL) Output "L" Level Voltage $(I_{OUT} = +2.0mA)$		-	0.4	-	0.4		

1. See DC output load circuit.

Operating, Standby, and Refresh Currents ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

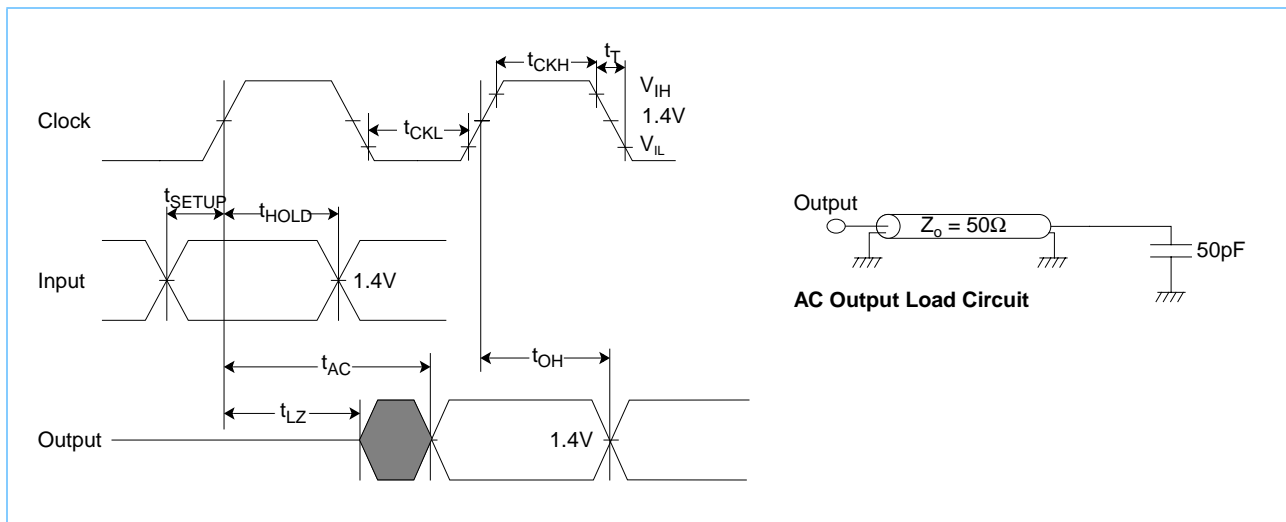
Parameter	Symbol	Test Condition	Organization		Units	Notes
			x64	x72		
Operating Current	I_{CC1}	1 Bank operation $t_{RC} = t_{RC}(\text{min})$, $t_{CK} = \text{min}$ Active-Precharge command cycling without Burst operation	600	675	mA	1, 2
Precharge Standby Current in Power Down Mode	I_{CC2P}	$\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$	8	9	mA	
	I_{CC2PS}	$\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{Infinity}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$	8	9	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	$\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$	280	315	mA	3
	I_{CC2NS}	$\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{Infinity}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$	48	54	mA	4
No Operating Current (Active state: 4 bank)	I_{CC3N}	$\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$	320	360	mA	3
	I_{CC3P}	$\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ (Power Down Mode)	24	27	mA	5
Burst Operating Current	I_{CC4}	$t_{CK} = \text{min}$, Read/write command cycling, multiple banks active, gapless data, BL = 4	960	1080	mA	2, 6
Auto (CBR) Refresh Current	I_{CC5}	$t_{CK} = \text{min}$, $t_{RC} = t_{RC}(\text{min})$, CBR command cycling	1160	1305	mA	
Self Refresh Current	I_{CC6}	$\text{CKE0} \leq 0.2\text{V}$	8	9	mA	
Serial PD Device Standby Current	I_{SB}	$V_{IN} = \text{GND}$ or V_{DD}	30	30	μA	7
Serial PD Device Active Power Supply Current	I_{CCA}	SCL Clock Frequency = 100KHz	1	1	mA	8

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC} . Input signals are changed up to three times during $t_{RC}(\text{min})$.
2. The specified values are obtained with the output open.
3. Input signals are changed once during three clock cycles.
4. Input signals are stable.
5. Active standby current will be higher if Clock Suspend is entered during a Burst Read cycle (add 1mA per DQ).
6. Input signals are changed once during $t_{ck}(\text{min})$.
7. $V_{DD} = 3.3\text{V}$
8. Input pulse levels $V_{DD} \times 0.1$ to $V_{DD} \times 0.9$, input rise and fall times 10ns, input and output timing levels $V_{DD} \times 0.5$, output load 1 TTL gate and $CL=100\text{pf}$.

AC Characteristics $(T_A = 0 \text{ to } +70^\circ\text{C}, V_{DD} = 3.3\text{V} \pm 0.3\text{V})$

1. An initial pause of $200\mu\text{s}$, with DQMB0-7 and CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
3. In addition to meeting the transition rate specification, the CK0 , CK2 , and CKE0 signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC timing tests have $V_{IL} = 0.8 \text{ V}$ and $V_{IH} = 2.0 \text{ V}$ with the timing referenced to the 1.40V crossover point.
5. AC measurements assume $t_T = 1.2 \text{ ns}$.

AC Characteristics Diagrams



Clock and Clock Enable Parameters

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, \overline{CAS} Latency = 3	7.5	1000	ns	
t_{AC3}	Clock Access Time, \overline{CAS} Latency = 3	—	5.4	ns	1
t_{CKH}	Clock High Pulse Width	2.5	—	ns	2
t_{CKL}	Clock Low Pulse Width	2.5	—	ns	2
t_{CES}	Clock Enable Set-up Time	1.5	—	ns	
t_{CEH}	Clock Enable Hold Time	0.8	—	ns	
t_{SB}	Power down mode Entry Time	0	7.5	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. Access time is measured at 1.4V. In AC Characteristics section, see notes.
2. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).



Common Parameters

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t _{CS}	Command Setup Time	1.5	—	ns	
t _{CH}	Command Hold Time	0.8	—	ns	
t _{AS}	Address and Bank Select Set-up Time	1.5	—	ns	
t _{AH}	Address and Bank Select Hold Time	0.8	—	ns	
t _{RCD}	\overline{RAS} to \overline{CAS} Delay	20.0	—	ns	1
t _{RC}	Bank Cycle Time	67.5	—	ns	1
t _{RAS}	Active Command Period	45	100000	ns	1
t _{RP}	Precharge Time	20.0	—	ns	1
t _{RRD}	Bank to Bank Delay Time	15	—	ns	1
t _{CCD}	\overline{CAS} to \overline{CAS} Delay Time	1	—	CLK	

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	75A		Units	Notes
		Min.	Max.		
t _{RSC}	Mode Register Set Cycle Time	2	—	CLK	1

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t _{OH}	Data Out Hold Time	2.7	—	ns	
t _{LZ}	Data Out to Low Impedance Time	0	—	ns	
t _{HZ3}	Data Out to High Impedance Time	3	5.4	ns	1
t _{DQZ}	DQM Data Out Disable Latency	2	—	CLK	1

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Refresh Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10		ns	

1. 4096 auto refresh cycles.

Write Cycle

Symbol	Parameter	-75A		Units
		Min.	Max.	
t_{DS}	Data In Set-up Time	1.5	—	ns
t_{DH}	Data In Hold Time	0.8	—	ns
t_{DPL}	Data input to Precharge	15	—	ns
t_{DAL3}	Data In to Active Delay CAS Latency = 3	5	—	CLK
t_{DQW}	DQM Write Mask Latency	0	—	CLK

Presence Detect Read and Write Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
f_{SCL}	SCL Clock Frequency		100	KHZ	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μ s	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μ s	
$t_{HD:STA}$	Start Condition Hold Time	4.0		μ s	
t_{LOW}	Clock Low Period	4.7		μ s	
t_{HIGH}	Clock High Period	4.0		μ s	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μ s	
$t_{HD:DAT}$	Data in Hold Time	0		μ s	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	μ s	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μ s	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The Write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal Erase/Program cycle. During the Write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.



Functional Description and Timing Diagrams

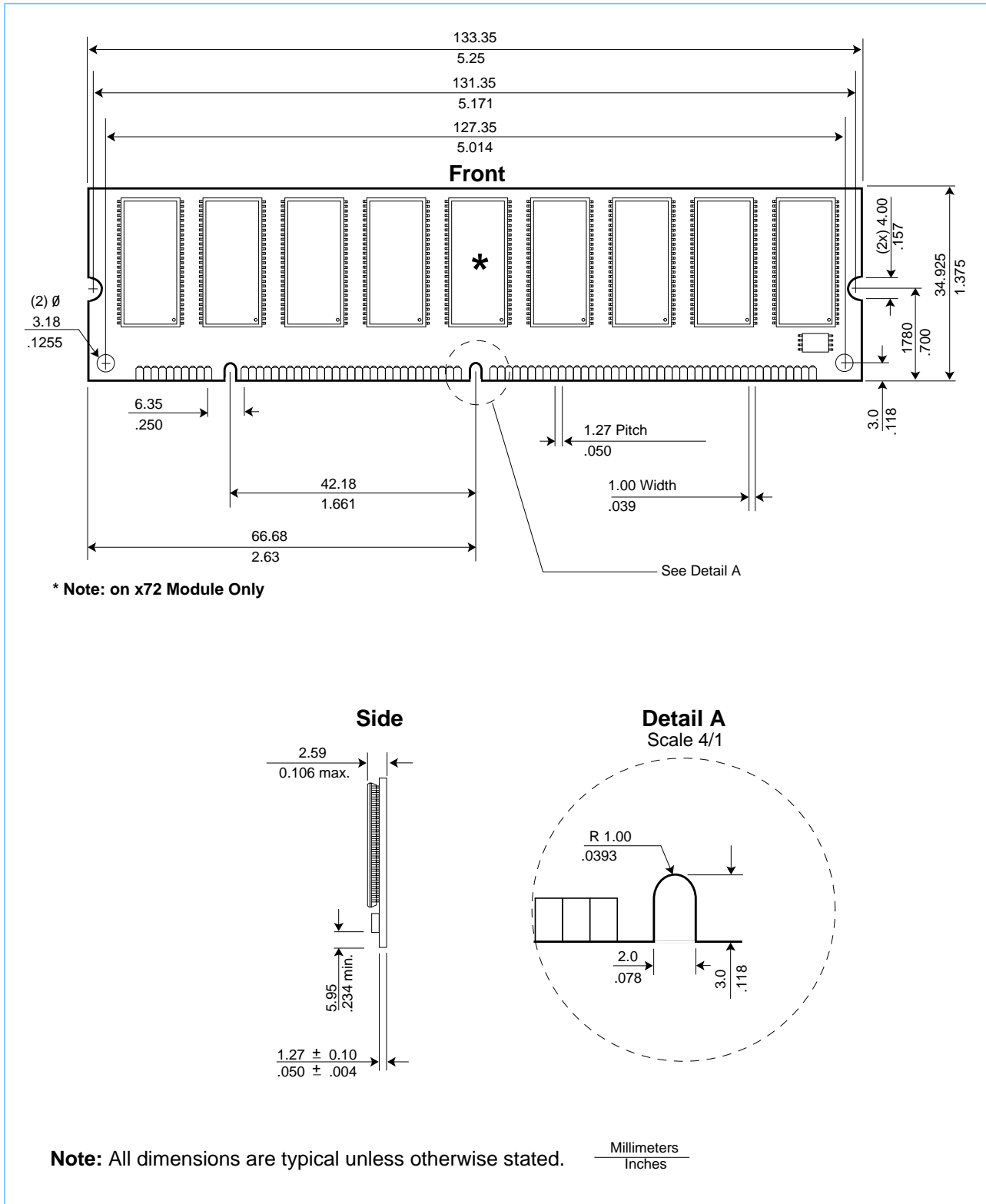
Refer to the IBM 64Mb Die Revision C Synchronous DRAM data sheet, document 19L3265, for the functional description and timing diagrams for SDRAM operation.

Refer to the IBM Application Notes *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.



Layout Drawing





Revision Log

Rev	Contents of Modification
6/99	Initial release.
7/99	Removed Preliminary
12/99	Updated ordering information



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