HN58C256 Series — Under Development

T-46-13-27

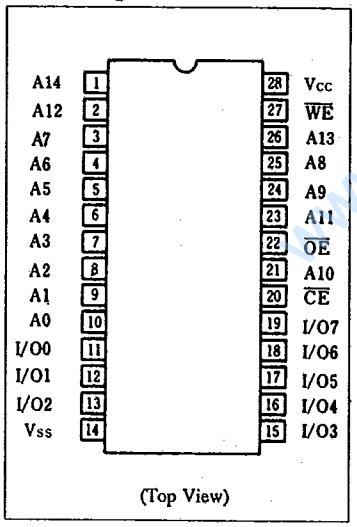
32768-Word × 8-Bit Electrically Erasable and Programmable CMOS ROM

The Hitachi HN58C256 is an electrically erasable and programmable ROM organized as 32768-word x 8-bit. It realizes high speed, low power consumption, and a high reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page reprogramming function to make its erase and write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 150 ns max / 200 ns max
- Low power dissipation: 20 mW/MHz, typ (Active); 100 µW max (Standby)
- $\overline{Data}$ polling
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode) and 10 year data retention

Pin Arrangement



(Top View)

Ordering Information

Type No.	Access Time	Package
HN58C256P-15	150 ns	600-mil 28-pin
HN58C256P-20	200 ns	plastic DIP (DP-28)
HN58C256FP-15	150 ns	28-pin
HN58C256FP-20	200 ns	plastic SOP*1 (FP-28D/DA)

Notes: *1. T is added to the end of the type no. for an SOP of 3.00 mm (max) thickness.
Die shipment is also available. Because the die has a $\overline{RES}$ pad, it can perform a reset function (refer to HN58C66 data sheet).

Pin Description

Pin Name	Function
A0–A14	Address
I/O0–I/O7	Input/Output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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Block Diagram

T-46-13-27