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SSI 32R1500R/1501R
5V, 4-Channel MR Read/Write Device
Advance Information

January 1996

3

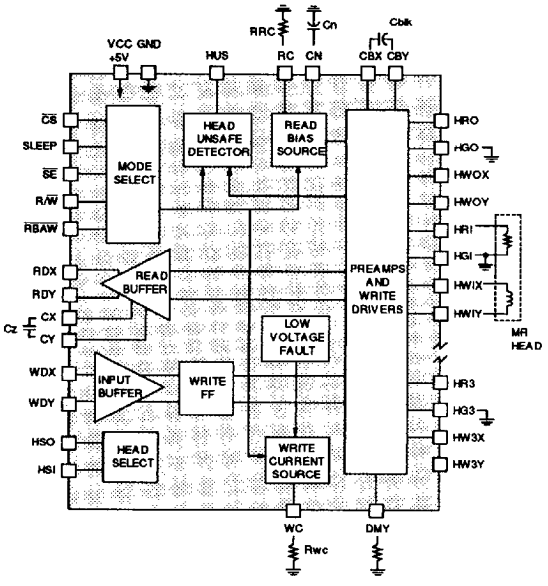
DESCRIPTION

The SSI 32R1500R/1501R is a BiCMOS monolithic integrated circuit designed for use with 4-terminal magneto-resistive head and thin film write composite recording heads. It provides a low noise MR head amplifier, MR bias current control, thin film write driver, write current control, and MR/TFH fault detection circuit for up to four channels. The device allows multiple channel write functions for servo writing. Two or four heads can be selected in the servo write mode. Read bias active in write (RBAW) is recommended to achieve the fastest write to read recovery. The 32R1500/1501R requires a single 5V supply and comes in a 48-lead TQFP package.

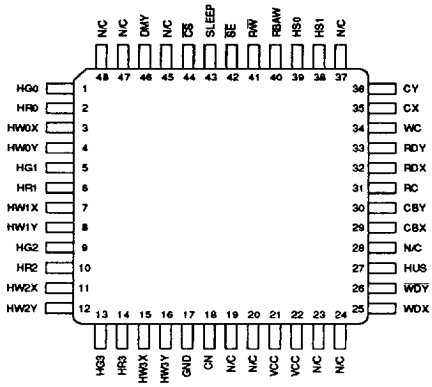
FEATURES

- **One side grounded input, fully differential ouput MR amplifier**
- **Unselected MR/TF heads are at GND potential**
- **MR/TF head unsafe**
- **Damping resistor bond option**
- **MR head bias current range = 10 - 20 mA**
- **MR read gain = 200 V/V @ 25Ω MR resistance**
- **MR read input noise = 0.8 nV/√Hz (Nom)**
- **Differential PECL write data input with flip-flop (32R1500R), or without flip-flop, (32R1501R) bond option**
- **Head voltage swing = 8 Vp-p (Nom)**
- **Write current range = 15 - 45 mA**
- **Power supply fault protection**
- **Servo bank write**

BLOCK DIAGRAM



PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNTIONAL DESCRIPTION

CIRCUIT OPERATION

The SSI 32R1500R/1501R addresses up to 4 four-terminal MR heads providing write drive or read bias and amplification. The mode control and head selection are accomplished with TTL pins SLEEP, $\overline{CS}$, R/$\overline{W}$, $\overline{SE}$, and HSn as shown in Tables 1 and 2. All of the TTL inputs have an internal pull-up resistor except HSn. HSn inputs have internal pull-down resistors.

TABLE 1: Head Selection

HS1	HS0	READ, WRITE MODE HEAD SELECTED	SERVO MODE HEAD SELECTED
0	0	0	0, 1
0	1	1	2, 3
1	0	2	X
1	1	3	0, 1, 2, 3

TABLE 2: Mode Selection

SLEEP	$\overline{CS}$	R/$\overline{W}$	$\overline{SE}$	MODE
1	1	X	X	Sleep
0	1	X	X	Idle
X	0	1	X	Read
X	0	0	1	Write
X	0	0	0	Servo

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the 32R1500R/1501R as a current switch and activates the Head Unsafe (HUS) detect circuitry. For the 32R1500R, head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each Low to High transition of the differential PECL signal [WDX-WDY]. Changing from read or idle mode to write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin, i.e., the Y side of the head will be higher potential than X side. The 32R1501R is the no flip-flop version, the head current is toggled between the X and Y side of the selected head on each transition of the [WDX-WDY] signal. When the potential of WDY is higher than WDX, the potential on the Y side of the head is higher causing Iw to flow from Y to X. The write current is externally programmed either by a resistor Rwc connected from pin WC to GND or by a current sink from pin WC. The magnitude of the current (0-pk) is given by:

$$Iw = \frac{Vwc \times Aw}{Rwc} = \frac{Kw}{Rwc}$$

where Aw is 20 mA/mA and Vwc is 1.25V.

Note that the actual head current Ix,y is given by:

$$Ix,y = \frac{Iw}{1 + (Rh + Rd)}$$

where Rh is the DC resistance of the head and Rd is the damping resistance (500Ω for 32R1501R).

HEAD UNSAFE (HUS)

Write mode, a high indicates unsafe condition

- Write data frequency too low
- Head transient voltage too low
- Shorted head
- No write current
- Open head
- Head short to ground

Servo write mode, a high indicates unsafe condition

- Write data frequency too low
- Open head (one or more heads)

Read mode, a low indicates unsafe condition

- Open head
- Shorted head
- Read bias not ready

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which activates the MR bias current generator and low noise differential amplifier. The outputs of the read amplifier RDX and RDY are emitter followers. The (HRn, HGn) inputs are non-inverting to the (RDX, RDY) outputs.

The DC current necessary for biasing the MR sensor is externally programmed either by a resistor Rrc connected from pin RC to GND or by a current sink. The magnitude of the bias current is given by:

$$Imr = \frac{Vrc \times Ar}{Rrc} = \frac{Kr}{Rrc}$$

where Ar is 10 mA/mA and Vrc is 1.5V.

An external capacitor connected from pin CN to GND is used for reducing the noise from MR bias current source. A low inductance capacitor with a value of 0.22 µF is recommended. An external floating capacitor Cblk connected between pins CBX and CBY respectively is required for DC blocking. Care should be taken to use low inductance high frequency capacitors and to locate them as close to the pins as possible – because the stray inductance will degrade amplifier's noise and frequency response performance. The value of the DC blocking capacitor Cblk will have a direct effect on the write to read recovery time. For fast recovery time, the capacitor value should be kept as small as possible. The value of the capacitor Cblk also sets the low frequency cutoff of the read amplifier. Nominal -3 dB low-frequency corner is given by:

$$f - \frac{1}{2\pi \times 26\Omega \times Cblk}$$

An external capacitor Cz connected between CX and CY introduces a zero to compensate for input parasitic inductance at the MR head ports. Peak frequency is given by:

$$f_{pk} - \frac{1}{2\pi \times 800 \times C_z}$$

FUNCTIONAL DESCRIPTION (continued)

IDLE MODE

Taking $\overline{CS}$ high selects idle mode which deactivates both the write current source and MR bias current. The voltage at the RC pin remains active so that an internal dummy head can be switched on to provide proper voltage biasing for the noise filtering capacitor Cn. The pins RDX/RDY are switched into high impedance state to facilitate multiple device applications where these pins could be wire OR'ed.

SLEEP MODE

Taking both SLEEP and $\overline{CS}$ high will put the device in sleep mode. The change in the DC blocking capacitors are not preserved in this low power mode.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit provides data security by disabling the write current generator and MR bias current during a voltage fault or power startup regardless of mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
WC	I	Write Current: sets the magnitude of the write current.
RC	I	Read Current: sets the magnitude of the MR bias current.
SLEEP	I	Sleep select, TTL.
HW0X - HW3X	O	Inductive write head X connection.
HW0Y - HW3Y	O	Inductive write head Y connection.
HR0 - HR3	I	MR read head connection, signal input.
HG0 - HG3	I	MR read head connection, ground side.
HUS	O	Head Unsafe: open collector; a high level indicates an unsafe write or servo write condition, a low indicates an unsafe condition in read mode.
$\overline{CS}$	I	Chip Select: a high inhibits the chip; TTL.
VCC	I	5V supply.
WDX, WDY	I	Differential PECL Write Data Input, a positive transition of (WDX - WDY) toggles the direction of the head current Head Select. (32R1500R)
HS0 - HS1	I	Head Select: Select one of four heads; TTL.
RDMY	I	Dummy MR registor.
R/$\overline{W}$	I	Read/Write: a high selects read mode; TTL.
$\overline{RBAW}$	I	Read Bias Active in Write mode: TTL
RDX, RDY	O	Differential MR head Read Data Output.
GND	I	Ground.
CBX, CBY	I	Floating DC blocking cap Cblk.
CX, CY	I	Zero capacitor to cancel read input parasitic inductor, Cz.
CN	I	Noise filter Cap Cn.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may result in permanent damage to the device.

PARAMETER		RATING
DC supply range	V_{CC}	-0.3 to 6V
Digital input voltage	TTL	-0.3 to V_{CC} + 0.3 V_{DC}
	PECL	0 to V_{CC} V_{DC}
Write current	I_W	60 mA
MR bias current	I_{MR}	30 mA
Write head voltage	V_H	0 to V_{CC} V
MR head voltage	V_{MR}	0 to 0.45V
Output current	RDX, RDY	-10 mA
	HUS*	+8 mA
Storage temperature	T_{STG}	-55 to 150°C

* Apply only at HUS is low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC supply voltage	VCC	4.5 to 5.5V
Write head load range	L_H	0.1 to 1.5 µH
Write head resistor	R_{WH}	5 to 50Ω
MR head range	R_{MR}	15 to 35Ω

ELECTRICAL SPECIFICATIONS (continued)

POWER SUPPLY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC supply current	read		16 + 2 Imr	28 + 2.21 mr	mA
	write		13 + Iw	22 + 1.1 Iw	mA
	servo, 2 heads		18 + 2 Iw	25 + 2.2 Iw	mA
	servo, 4 heads		22 + 4 Iw	32 + 4.4 Iw	mA
	idle		6	12	mA
	sleep		1	3	mA
Power dissipation	read		80 + 10 Imr	154 + 12.2 Imr	mW
	write		65 + 5 Iw	121 + 6.1 Iw	mW
	servo, 2 heads		90 + 10 Iw	138 + 12.1 Iw	mW
	servo, 4 heads		110 + 20 Iw	176 + 24.2 Iw	mW
	idle		30	66	mW
	sleep		5	16.5	mW
VCC fault voltage	Iw = 0.2 mA		3.6	3.9	V

DIGITAL INPUTS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input high voltage	V_{IH1}		2			V
Input low voltage	V_{IL1}				0.8	V
Input high current	I_{IH1}	Vih1 = 2.7V			100	µA
Input low current	Z_{IL1}	Vil1 = 0.4V	-400			µA
PECL high voltage	V_{IH2}		VCC -1.17		VCC - 0.7	V
PECL low voltage	V_{IL2}		VCC - 2		V_{IH2}-0.3	V
PECL Δ voltage (WDX - WDY)			0.3	0.8		V
PECL high current	I_{IH2}	Vin = VCC -0.9V		100	200	µA
PECL low current	I_{IL2}	Vin = VCC -1.7V		75	150	µA
WUS high current		VOH = 5V			20	µA
WUS low voltage		IOL = 2 mA			0.5	V

READ CHARACTERISTICS

Unless otherwise specified, Rmr = 25Ω; Rdmy = Rmr, Rrc = 1.5 kΩ, Lrh = 0 nH, Cn = 0.22 µF, Cb = 0.033 µF, Cz = 0 pF, Rl = 4 kΩ differential, Vin = 1 mVp-p, fin = 5 MHz.

MR Head resistance			15	25	35	Ω
MR bias current range			6	10	16	mA
MR current setting voltage	V_{RC}		1.4	1.5	1.6	V
MR current gain	A_R		9	10	11	A/A
"Kr" factor		Kr = Ar • Vrc	13	15	17	V
Unselected MR current					20	µA
Input impedance		AC		3		Ω
Differential voltage gain		Rmr = 15Ω, Rrc = 1.5 kΩ		300		V/V
		Rmr = 20Ω, Rrc = 1.5 kΩ		230		V/V
		Rmr = 25Ω, Rrc = 1.5 kΩ		200		V/V
		Rmr 30Ω, Rrc = 1.5 kΩ		150		V/V
		Rmr = 35Ω, Rrc = 1.5 kΩ		130		V/V
Bandwidth	-1 dB	Rmr = 25Ω	25	40		MHz
	-3 dB	Rmr = 25Ω	45	80		MHz
Input noise *1		1 MHz < BW < 15 MHz		0.8	1.4	nV/√Hz
Input noise *2		1 MHz < BW < 15 MHz		1.2	1.8	nV/√Hz

*1 Exclude noise from Rmr and Rdmy.

*2 Include noise from Rmr = 25Ω and Rdmy = 25Ω.

READ CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Dynamic range	Gain falls to 90%	2			mV
Output offset voltage	Rmr = Rdmy	250		250	mV
Output current		0.8	1.5		mA
Output voltage		2.5	3.3	4.1	V
Output resistance	Single-ended, DC		50	100	Ω
PSRR	Vin = 100 mVp-p, 5 MHz	45	60		dB
GNR	Vin = 100 mVp-p, 5 MHz	45	60		dB
Channel separation	Vin = 100 mVp-p, 5 MHz	45	65		dB

Note: 1. Choose Rdmy values as close as possible to any MR heads.
2. Place Cn, Cb capacitors right next to the pins.

WRITE/SERVO CHARACTERISTICS
Unless otherwise specified, Lwh = 220 nH, Rwh = 15Ω, Rc = 830Ω

Write current range		15	30	45	mA
Write current gain Aw			20		A/A
Write current setting voltage Vwc		1.15	1.25	1.35	V
"kw" factor	kw = Aw • Vwc	22	25	28	V
Differential head swing	Open head, Iw = 40 mA	6	8		Vp-p
	Open head, servo	5.5	8		Vp-p
Unselected head current	DC			0.1	mA
	AC			1	mApk
Damping resistor Rd	32R1500R/1501R	375	500	625	Ω
	32R1500/1501	2000	3000	4000	Ω
Head differential load capacitance				15	pF

SWITCHING CHARACTERISTICS

Unless otherwise specified, Rmr = 25Ω; Rdmy = Rmr, Rrc = 1 kΩ; Cn = 0.22 µF, Cb = 0.033 µF, Cx = 3 pF
Lwh = 220 nH, Rwh = 15Ω, Rwc = 830Ω,
T(R/$\overline{W}$) = 100 µs, T($\overline{CS}$) = 1 ms, T(HS) = 100 µs

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/$\overline{W}$	write to read RBAW = LOW	0.9 Rmr < Rdmy < 1.1 Rmr 90% of AC envelope ±100 mV of read DC		0.5	1.5	µs
	RBAW = HIGH	0.9 Rmr < Rdmy < 1.1 Rmr 90% of AC envelope ±100 mV of read DC		3	10	µs
	read to write	90% of Write Current			1	µs
$\overline{CS}$	idle to read	90% of AC envelope ±100 mV of read DC		15	50	µs
	select to unselect	10% of write current			1	µs
SLEEP	sleep to read	90% of AC envelope ±100 mV of read DC		80	500	µs
HS 0, 1, 2, 3	to any MR	90% of AC envelope ±100 mV of read DC 5% of ΔMR		1 5	3 20	µs µs
Write data frequency		Valid HUS	1		50	MHz
Rise/fall time		Iw = 30 mA, Lh = 220 nH, Rh = 15Ω 10% to 90% points		4	6	ns
Head current delay	Td3	50% (WDX - WDY) to 50% (Ix - Iy)			40	ns
Write current asymmetry		Preparation dealy difference			1	ns

ELECTRICAL SPECIFICATIONS (continued)

HEAD UNSAFE DETECTION

Unless otherwise specified, Rmr = 25Ω; Rdmy = Rmr, Rrc = 1.5 kΩ; Cn = 0.22 µF, Cb = 0.033 µF, Cx = 0 pF
Lwh = 200 nH, Rwh = 15Ω, Rwc = 830Ω, f(write Data) = 10 MHz

WRITE MODE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Idle/Read to HUS ready					1	µs
Safe to unsafe	Td1	Write data frequency too low	0.5	1.2	2.5	µs
Unsafe to safe	Td2	Alter one (Ix - Iy) terminition		0.2	0.4	µs

READ MODE

Open threshold	Rmr/Rdmy	1.3	2		Ω/Ω
Short threshold	Rmr/Rdmy		0.5	0.7	Ω/Ω
Idle/Write to HUS ready				1	µs

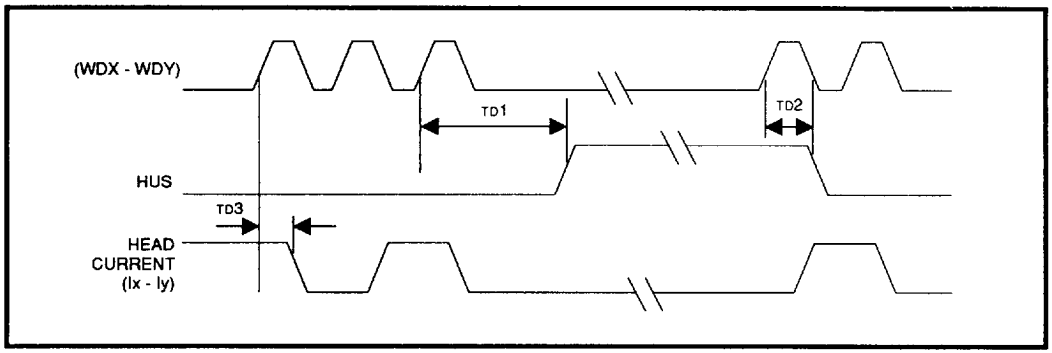


FIGURE 1: 32R1500R Write Mode Timing

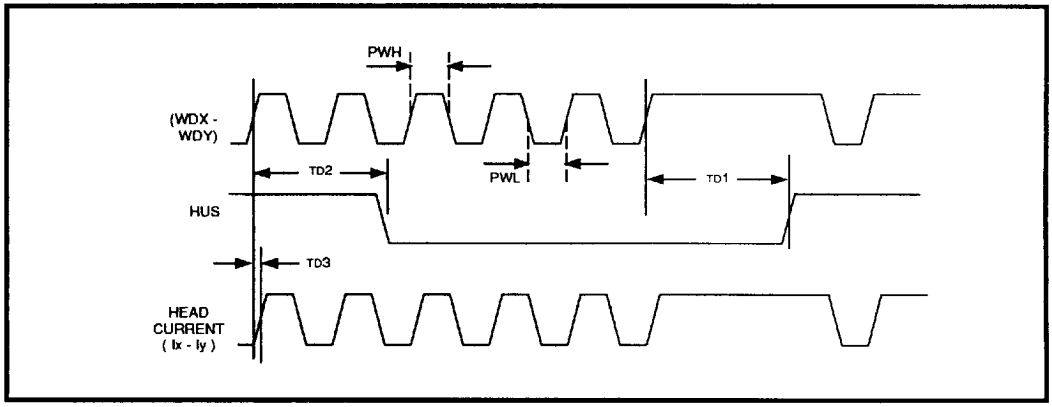
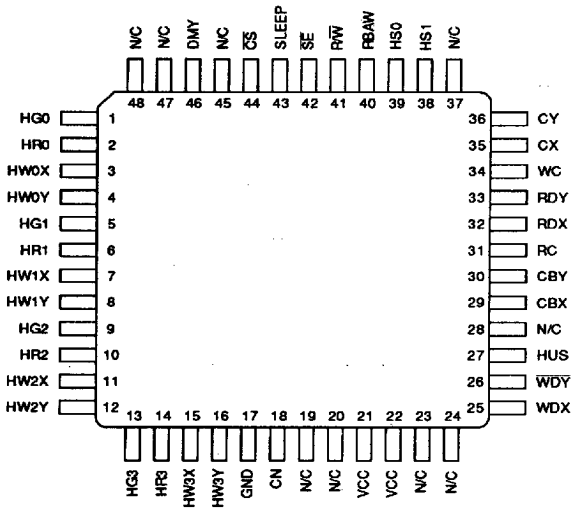


FIGURE 2: 32R1501R Write Mode Timing Diagram

SSI 32R1500R/1501R
5V 4-Channel
MR Read/Write Device

PACKAGE PIN DESIGNATIONS
(Top View)



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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