

Vishay Siliconix

# P-Channel 40 V (D-S) MOSFET

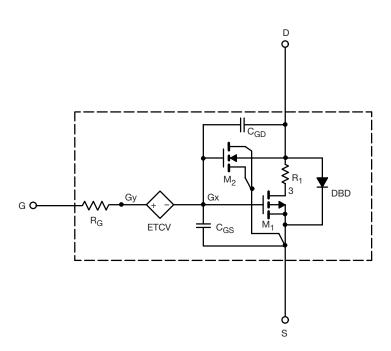
### **DESCRIPTION**

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -  $55\,^{\circ}\text{C}$  to +  $125\,^{\circ}\text{C}$  temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC

## **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



#### Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

# **SPICE Device Model Si4401DDY**

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SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	1.3	-	V
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -10.2 \text{ A}$	0.012	0.012	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -8.4 \text{ A}$	0.019	0.018	
Forward Transconductancea	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 10.2 A	9	10	S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 8.2 A	- 0.79	- 0.80	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	2990	3007	pF
Output Capacitance	C <sub>oss</sub>		336	335	
Reverse Transfer Capacitance	C <sub>rss</sub>		289	291	
Total Gate Charge	Qg	$V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10.2 \text{ A}$	62	64	nC
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 10.2 A	33	33	
Gate-Source Charge	Q <sub>gs</sub>		9.8	9.8	
Gate-Drain Charge	$Q_{gd}$		15.7	15.7	

## Notes

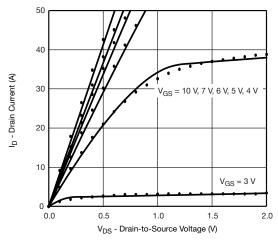
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

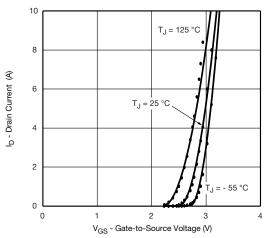
b. Guaranteed by design, not subject to production testing.

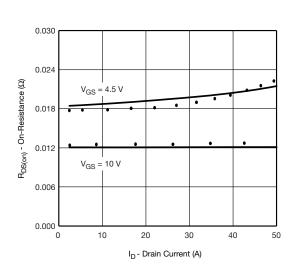


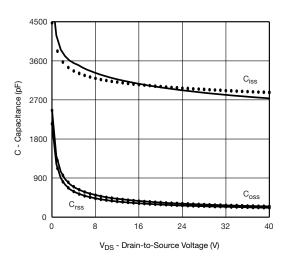
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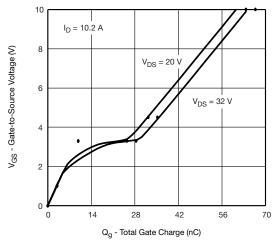
# COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25~{}^{\circ}\text{C}$ , unless otherwise noted

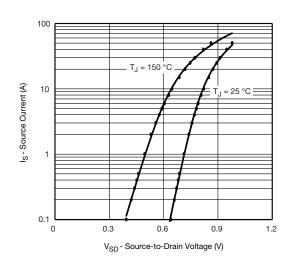












**Note**Dots and squares represent measured data.



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