, INC.

PEEL™22CV10A-15/PEEL™22CV10AL-15
CMOS Programmable Electrically Erasable Logic Device

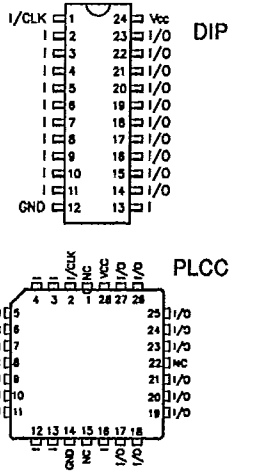
Features

- **Advanced CMOS EEPROM Technology**
- **High Performance**
  - — t_{PD} = 15ns, f_{max} = 66.7MHz
- **Low Power Consumption**
  - — 115mA at 25MHz
  - — 75mA at 25MHz (L)
- **EE Reprogrammability**
  - — Low-risk reprogrammable inventory
  - — Superior programming and functional yield
  - — Erases and programs in seconds
- **Development and Programming Support**
  - — Third-party software and programmers
  - — ICT PEEL Development System and software.
- **Architectural Flexibility**
  - — 132 product term x 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Variable product term distribution (8 to 16 per output) for greater logic flexibility
  - — Independently programmable I/O macrocells
  - — Synchronous preset, asynchronous clear
  - — Independently programmable output enables
- **Application Versatility**
  - — Replaces random SSI/MSI logic
  - — Pin and JEDEC compatible with all 22V10 devices

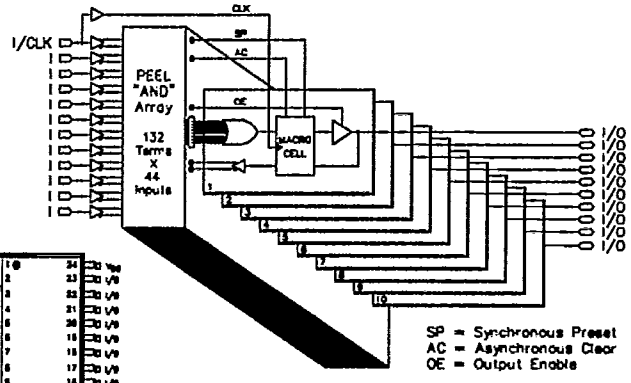
General Description

The ICT PEEL22CV10A-15 are CMOS Programmable Electrically Erasable Logic Devices that provide a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to early generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10A rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10A allows cost effective plastic packaging, low risk inventory, reduced development and retrofit costs, and enhanced testability to ensure 100% field programmability and function. The PEEL22CV10A's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10. Applications for the PEEL22CV10A include: replacement of random SSI/MSI logic circuitry and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10A is provided by ICT and third-party manufacturers.

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [6]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

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Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T_A	Ambient Temperature	Commercial	0	+ 70	°C
		Industrial	− 40	+ 85	°C
T_R	Clock Rise Time	See note 4		250	ns
T_F	Clock Fall Time	See note 4		250	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

3

D.C. Electrical Characteristics

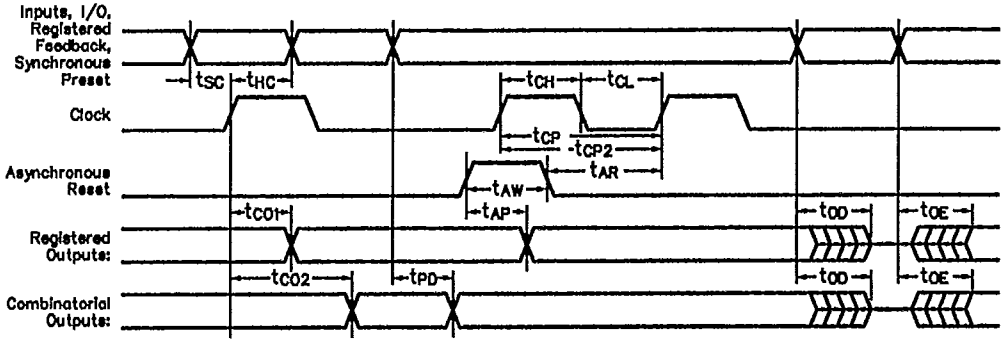
Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2..4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C	− 30	−135	mA
I_{CC}	V_{CC} Current, Active	V_{IN} = 0 or 3V[5,11] f = 25 MHz All outputs disabled.		115	mA
			L	75	mA
C_{IN} [8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT} [8]	Output Capacitance			12	pF

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Parameter	22CV10A-15		Unit
		Min	Max	
t_{PD}	Input[6] to non-registered output		15	ns
t_{OE}	Input [6] to output enable [7]		15	ns
t_{OD}	Input [6] to output disable [7]		15	ns
t_{CO1}	Clock to output		10	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		19	ns
t_{CF}	Clock to feedback		6	ns
t_{SC}	Input [6] or feedback setup to clock	10		ns
t_{HC}	Input [6] hold after clock	0		ns
t_{CL},t_{CH}	Clock width - clock low time, clock high time [4]	7.5		ns
t_{CP}	Min clock period Extenal (t_{SC} + t_{CO1})	20		ns
f_{max1}	Max clock freq. Internal Feedback ($1/t_{SC}+t_{CF}$)[13]	62.5		MHz
f_{max2}	Max clock freq. External ($1/t_{CP}$)[13]	50.0		MHz
f_{max3}	Max clock freq. No Feedback ($1/t_{CL}+t_{CH}$)[13]	66.7		MHz
t_{AW}	Asynchronous Reset pulse width	15		ns
t_{AP}	Input [6] to Asynchronous Reset		18	ns
t_{AR}	Asynchronous Reset recovery time		18	ns
t_{RESET}	Power-on reset time for registers in clear state [4]		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in ta, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application. This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on intial characterization and are tested after any design or process modification which may affect operational frequency.