

# MOS INTEGRATED CIRCUIT

# $\mu$ PD42S4210A, 424210A

## 4 M-BIT DYNAMIC RAM

### 256 K-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE

#### Description

The  $\mu$ PD42S4210A, 424210A are 262 144 words by 16 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The  $\mu$ PD42S4210A, 424210A are packed in 44-pin plastic TSOP(II) and 40-pin plastic SOJ.

#### Features

- Hyper page mode
- 262 144 words by 16 bits organization
- Single +5.0 V  $\pm$  10 % power supply

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
$\mu$ PD42S4210A-50, 424210A-50	50 ns	84 ns	20 ns
$\mu$ PD42S4210A-60, 424210A-60	60 ns	104 ns	25 ns
$\mu$ PD42S4210A-70, 424210A-70	70 ns	124 ns	30 ns

- The  $\mu$ PD42S4210A can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh

Part number	Refresh cycle	Refresh
$\mu$ PD42S4210A	512 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
$\mu$ PD424210A	512 cycles / 8 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S4210AG5-50	50 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S4210AG5-60	60 ns		
μPD42S4210AG5-70	70 ns		
<del>μPD42S4210AG5-50-7KF</del>	<del>50 ns</del>	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
<del>μPD42S4210AG5-60-7KF</del>	<del>60 ns</del>		
<del>μPD42S4210AG5-70-7KF</del>	<del>70 ns</del>		
μPD42S4210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD42S4210ALE-60	60 ns		
μPD42S4210ALE-70	70 ns		
μPD424210AG5-50	50 ns	44-pin Plastic TSOP (II) (400 mil)	
μPD424210AG5-60	60 ns		
μPD424210AG5-70	70 ns		
<del>μPD424210AG5-50-7KF</del>	<del>50 ns</del>	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
<del>μPD424210AG5-60-7KF</del>	<del>60 ns</del>		
<del>μPD424210AG5-70-7KF</del>	<del>70 ns</del>		
μPD424210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD424210ALE-60	60 ns		
μPD424210ALE-70	70 ns		

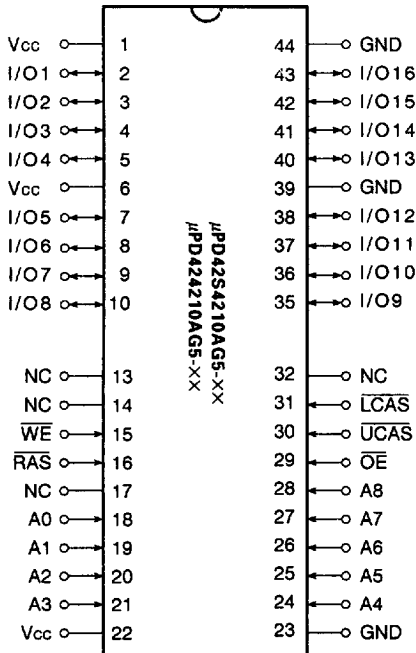
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

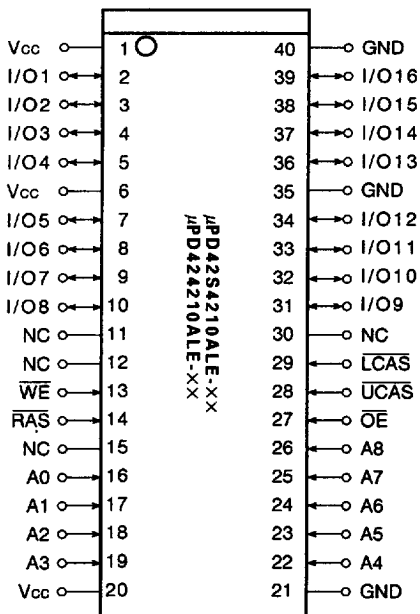
Pin Configurations (Marking Side)

44-pin, Plastic TSOP (II)  
(400 mil)



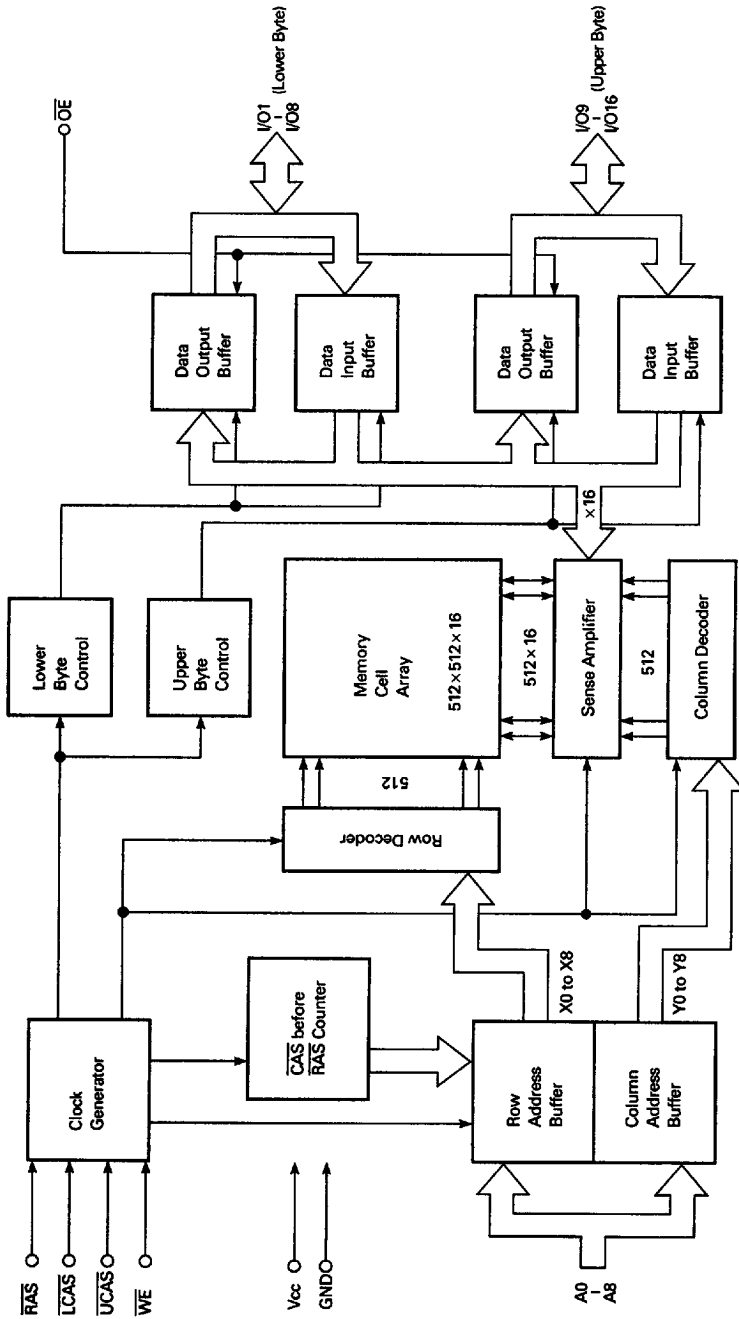
- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
- LCAS : Column Address Strobe (lower)
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

40-pin Plastic SOJ  
(400 mil)



- A0 to A8 : Address Inputs
- I/O1 to I/O16 : Data Inputs/Outputs
- RAS : Row Address Strobe
- UCAS : Column Address Strobe (upper)
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Block Diagram



■ 6427525 0057656 609 ■

**Input/Output Pin Functions**

The μPD42S4210A, 424210A have input pins  $\overline{RAS}$ ,  $\overline{CAS}$  <sup>Note</sup>,  $\overline{WE}$ ,  $\overline{OE}$ , A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262 144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$ . Then, switch the address bus to column address and activate $\overline{CAS}$ . Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (tASR, tASC) and hold time (tRAH, tCAH) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$ .
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ .
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{OE}$ . If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

**Note**  $\overline{CAS}$  means  $\overline{UCAS}$  and  $\overline{LCAS}$ .

**Hyper Page Mode**

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

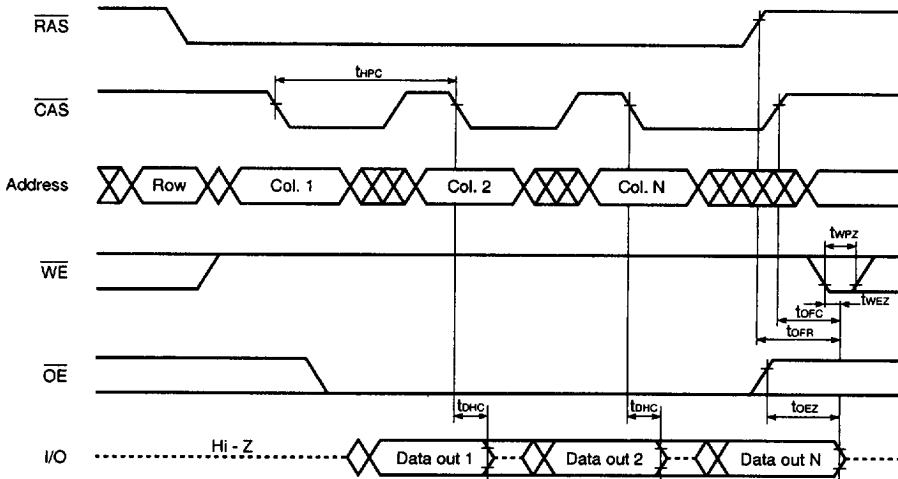
1. Data output time is extended.

In the hyper page mode, the output data is held to the next  $\overline{CAS}$  cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the  $\overline{CAS}$  cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the  $\overline{CAS}$  cycle time becomes shorter.

2. The  $\overline{\text{CAS}}$  cycle time in the hyper page mode is shorter than that in the fast page mode.  
 In the hyper page mode, due to the data extend function, the  $\overline{\text{CAS}}$  cycle time can be shorter than in the fast page mode if the timing margin is the same.  
 Taking a device whose  $t_{\text{RAC}}$  is 60 ns as an example, the  $\overline{\text{CAS}}$  cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one  $\overline{\text{RAS}}$  cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

**Hyper Page Mode Read Cycle**



To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on the state of each signal.

- (1)  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  : inactive (at the end of read cycle)  
 $\overline{\text{WE}}$  : inactive,  $\overline{\text{OE}}$  : active  
 $t_{\text{OFC}}$  is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.  
 $t_{\text{OFR}}$  is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.
- (2) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)  
 $\overline{\text{WE}}$  : active,  $\overline{\text{OE}}$  : active...  $t_{\text{WEZ}}$ ,  $t_{\text{WPZ}}$  are effective.  
 $\overline{\text{WE}}$  : inactive,  $\overline{\text{OE}}$  : inactive...  $t_{\text{OEZ}}$  is effective.

**Electrical Specifications**

- $\overline{\text{CAS}}$  means  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V <sub>T</sub>		-1.0 to +7.0	V
Supply Voltage	V <sub>CC</sub>		-1.0 to +7.0	V
Output Current	I <sub>O</sub>		50	mA
Power Dissipation	P <sub>D</sub>		1	W
Operating Temperature	T <sub>opt</sub>		0 to +70	°C
Storage Temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
High Level Input Voltage	V <sub>IH</sub>		2.4		V <sub>CC</sub> +1.0	V
Low Level Input Voltage	V <sub>IL</sub>		-1.0		+0.8	V
Ambient Temperature	T <sub>a</sub>		0		70	°C

**Capacitance (T<sub>a</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C <sub>I1</sub>	Address			5	pF
	C <sub>I2</sub>	RAS, CAS, WE, OE			7	pF
Data Input/Output Capacitance	C <sub>I/O</sub>	I/O			7	pF



DC Characteristics (Recommended Operating Conditions unless otherwise noted)

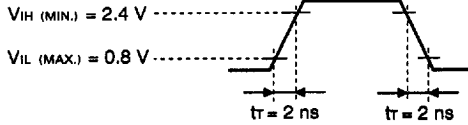
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current	Icc1	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 3
			$\text{trac} = 60 \text{ ns}$		80		
			$\text{trac} = 70 \text{ ns}$		70		
Standby current	μPD42S4210A	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.}), I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			2	mA	
					0.15		
	μPD424210A	$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{IH}(\text{MIN.}), I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			2		
					1		
RAS only refresh current	Icc3	$\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ $\text{trc} = \text{trc}(\text{MIN.}), I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 3, 4
			$\text{trac} = 60 \text{ ns}$		80		
			$\text{trac} = 70 \text{ ns}$		70		
Operating current (Hyper page mode)	Icc4	$\overline{\text{RAS}} \leq V_{IL}(\text{MAX.}), \overline{\text{CAS}}$ Cycling $\text{thpc} = \text{thpc}(\text{MIN.}), I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2, 5
			$\text{trac} = 60 \text{ ns}$		80		
			$\text{trac} = 70 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	Icc5	$\overline{\text{RAS}}$ Cycling $\text{trc} = \text{trc}(\text{MIN.})$ $I_o = 0 \text{ mA}$	$\text{trac} = 50 \text{ ns}$		90	mA	1, 2
			$\text{trac} = 60 \text{ ns}$		80		
			$\text{trac} = 70 \text{ ns}$		70		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh current (512 Cycles / 128 ms, only for the μPD42S4210A)	Icc6	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : 512 Cycles / 128 ms $\overline{\text{RAS}}, \overline{\text{CAS}}$ : $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Address : $V_{IH}$ or $V_{IL}$ WE, OE : $V_{IH}$ $I_o = 0 \text{ mA}$	$\text{trac} \leq$ 200 ns		200	μA	1, 2
			$\text{trac} \leq$ 1 μs		300		
Self refresh current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, only for the μPD42S4210A)	Icc7	$\overline{\text{RAS}}, \overline{\text{CAS}}$ : $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH}(\text{MAX.})$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			150	μA	2
Input leakage current	Ii (L)	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current	Io (L)	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage	VoH	$I_o = -2.5 \text{ mA}$	2.4			V	
Low level output voltage	VoL	$I_o = +2.1 \text{ mA}$			0.4	V	

- Notes**
- Icc1, Icc3, Icc4, Icc5 and Icc6 depend on cycle rates (trc and thpc).
  - Specified values are obtained with outputs unloaded.
  - Icc1 and Icc3 are measured assuming that address can be changed once or less during  $\overline{\text{RAS}} \leq V_{IL}(\text{MAX.})$  and  $\overline{\text{CAS}} \geq V_{IH}(\text{MIN.})$ .
  - Icc3 is measured assuming that all column address inputs are held at either high or low.
  - Icc4 is measured assuming that all column address inputs are switched only once during each hyper page cycle.

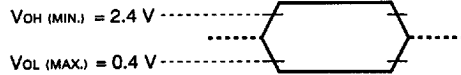
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	t <sub>RC</sub>	84	-	104	-	124	-	ns		
RAS Precharge Time	t <sub>RP</sub>	30	-	40	-	50	-	ns		
CAS Precharge Time	t <sub>CPN</sub>	7	-	10	-	10	-	ns		
RAS Pulse Width	t <sub>RAS</sub>	50	10 000	60	10 000	70	10 000	ns		
CAS Pulse Width	t <sub>CAS</sub>	7	10 000	10	10 000	12	10 000	ns		
RAS Hold Time	t <sub>RSH</sub>	7	-	10	-	12	-	ns		
CAS Hold Time	t <sub>CSH</sub>	35	-	40	-	50	-	ns		
RAS to CAS Delay Time	t <sub>RCD</sub>	11	37	14	45	14	52	ns	1	
RAS to Column Address Delay Time	t <sub>RAD</sub>	9	25	12	30	12	35	ns	1	
CAS to RAS Precharge Time	t <sub>CRP</sub>	5	-	5	-	5	-	ns	2	
Row Address Setup Time	t <sub>ASR</sub>	0	-	0	-	0	-	ns		
Row Address Hold Time	t <sub>RAH</sub>	7	-	10	-	10	-	ns		
Column Address Setup Time	t <sub>ASC</sub>	0	-	0	-	0	-	ns		
Column Address Hold Time	t <sub>CAH</sub>	7	-	10	-	12	-	ns		
OE Lead Time Referenced to RAS	t <sub>OES</sub>	0	-	0	-	0	-	ns		
CAS to Data Setup Time	t <sub>CLZ</sub>	0	-	0	-	0	-	ns		
OE to Data Setup Time	t <sub>OLZ</sub>	0	-	0	-	0	-	ns		
OE to Data Delay Time	t <sub>OED</sub>	10	-	13	-	15	-	ns		
Masked Byte Write Hold Time Referenced to RAS	t <sub>MRH</sub>	0	-	0	-	0	-	ns		
Transition Time (Rise and Fall)	t <sub>T</sub>	1	50	1	50	1	50	ns		
Refresh Time	μPD42S4210A	t <sub>REF</sub>	-	128	-	128	-	128	ms	3
	μPD424210A		-	8	-	8	-	8	ms	

**Notes** 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD(MAX)}$ and $t_{RCD} \leq t_{RCD(MAX)}$	$t_{RAC(MAX)}$	$t_{RAC(MAX)}$
$t_{RAD} > t_{RAD(MAX)}$ and $t_{RCD} \leq t_{RCD(MAX)}$	$t_{AA(MAX)}$	$t_{RAD} + t_{AA(MAX)}$
$t_{RCD} > t_{RCD(MAX)}$	$t_{CAC(MAX)}$	$t_{RCD} + t_{CAC(MAX)}$

$t_{RAD(MAX)}$  and  $t_{RCD(MAX)}$  are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ( $t_{RAC}$ ,  $t_{AA}$  or  $t_{CAC}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{RAD} \geq t_{RAD(MAX)}$  and  $t_{RCD} \geq t_{RCD(MAX)}$  will not cause any operation problems.

- $t_{CRP(MIN)}$  requirement is applied to  $\overline{RAS}$ ,  $\overline{CAS}$  cycles.
- This specification is applied only to the μPD42S4210A.

**Read Cycle**

Parameter	Symbol	$t_{RAC} = 50 \text{ ns}$		$t_{RAC} = 60 \text{ ns}$		$t_{RAC} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	$t_{RAC}$	-	50	-	60	-	70	ns	1
Access Time from $\overline{CAS}$	$t_{CAC}$	-	13	-	15	-	18	ns	1
Access Time from Column Address	$t_{AA}$	-	25	-	30	-	35	ns	1
Access Time from $\overline{OE}$	$t_{OEA}$	-	13	-	15	-	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	$t_{RAL}$	25	-	30	-	35	-	ns	
Read Command Setup Time	$t_{RCS}$	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	$t_{RRH}$	0	-	0	-	0	-	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	$t_{RCH}$	0	-	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	$t_{OEZ}$	0	10	0	13	0	15	ns	3

**Notes** 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$t_{RAD} \leq t_{RAD(MAX)}$ and $t_{RCD} \leq t_{RCD(MAX)}$	$t_{RAC(MAX)}$	$t_{RAC(MAX)}$
$t_{RAD} > t_{RAD(MAX)}$ and $t_{RCD} \leq t_{RCD(MAX)}$	$t_{AA(MAX)}$	$t_{RAD} + t_{AA(MAX)}$
$t_{RCD} > t_{RCD(MAX)}$	$t_{CAC(MAX)}$	$t_{RCD} + t_{CAC(MAX)}$

$t_{RAD(MAX)}$  and  $t_{RCD(MAX)}$  are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ( $t_{RAC}$ ,  $t_{AA}$  or  $t_{CAC}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{RAD} \geq t_{RAD(MAX)}$  and  $t_{RCD} \geq t_{RCD(MAX)}$  will not cause any operation problems.

- Either  $t_{RCH(MIN)}$  or  $t_{RRH(MIN)}$  should be met in read cycles.
- $t_{OEZ(MAX)}$  defines the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{OH}$  or  $V_{OL}$ .

**Write Cycle**

Parameter	Symbol	t <sub>TRAC</sub> = 50 ns		t <sub>TRAC</sub> = 60 ns		t <sub>TRAC</sub> = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	twch	7	-	10	-	10	-	ns	1
$\overline{WE}$ Pulse Width	twp	7	-	10	-	10	-	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	trwl	7	-	10	-	12	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	tcwl	7	-	10	-	12	-	ns	
$\overline{WE}$ Setup Time	twcs	0	-	0	-	0	-	ns	2
OE Hold Time	toeh	0	-	0	-	0	-	ns	
Data-in Setup Time	t <sub>DS</sub>	0	-	0	-	0	-	ns	3
Data-in Hold Time	t <sub>DH</sub>	7	-	10	-	10	-	ns	3

- Notes**
1. t<sub>WP(MIN.)</sub> is applied to late write cycles or read modify write cycles. In early write cycles, t<sub>WCH(MIN.)</sub> should be met.
  2. If t<sub>WCS</sub> ≥ t<sub>WCS(MIN.)</sub>, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  3. t<sub>OS(MIN.)</sub> and t<sub>DH(MIN.)</sub> are referenced to the  $\overline{CAS}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{WE}$  falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	t <sub>TRAC</sub> = 50 ns		t <sub>TRAC</sub> = 60 ns		t <sub>TRAC</sub> = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	107	-	133	-	157	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	trwd	64	-	77	-	89	-	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tcwd	27	-	32	-	37	-	ns	1
Column Address to $\overline{WE}$ Delay Time	tawd	39	-	47	-	54	-	ns	1

- Note 1.** If t<sub>WCS</sub> ≥ t<sub>WCS(MIN.)</sub> the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>TRWD</sub> ≥ t<sub>TRWD(MIN.)</sub>, t<sub>TCWD</sub> ≥ t<sub>TCWD(MIN.)</sub>, t<sub>AWD</sub> ≥ t<sub>AWD(MIN.)</sub>, and t<sub>CPWD</sub> ≥ t<sub>CPWD(MIN.)</sub>, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t <sub>RWC</sub>	20	-	25	-	30	-	ns	
RAS Pulse Width	t <sub>RASP</sub>	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	t <sub>HCAS</sub>	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	t <sub>CP</sub>	7	-	10	-	10	-	ns	
Access Time from CAS Precharge	t <sub>ACP</sub>	-	27	-	35	-	40	ns	
CAS Precharge to WE Delay Time	t <sub>CPWD</sub>	41	-	52	-	59	-	ns	1
RAS Hold Time from CAS Precharge	t <sub>RHCP</sub>	27	-	35	-	40	-	ns	
Read Modify Write Cycle Time	t <sub>HRWC</sub>	52	-	66	-	75	-	ns	
Data Output Hold Time	t <sub>DHC</sub>	5	-	5	-	5	-	ns	
Output Buffer Turn-off Delay from WE	t <sub>WEZ</sub>	0	10	0	13	0	15	ns	2,3
WE Pulse Width	t <sub>WPZ</sub>	7	-	10	-	10	-	ns	3
Output Buffer Turn-off Delay from RAS	t <sub>OFR</sub>	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from CAS	t <sub>OFC</sub>	0	10	0	13	0	15	ns	2,3

- Notes**
- If  $t_{WC} \geq t_{WC(MIN.)}$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If  $t_{RW} \geq t_{RW(MIN.)}$ ,  $t_{CWD} \geq t_{CWD(MIN.)}$ ,  $t_{AWD} \geq t_{AWD(MIN.)}$ , and  $t_{CPWD} \geq t_{CPWD(MIN.)}$ , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
  - $t_{OFC(MAX.)}$ ,  $t_{OFR(MAX.)}$  and  $t_{WEZ(MAX.)}$  define the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
  - To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OE}$  as follows. The effective specification depends on state of each signal.

(1)  $\overline{RAS}$ ,  $\overline{CAS}$  : inactive (at the end of read cycle)

$\overline{WE}$  : inactive,  $\overline{OE}$  : active

$t_{OFC}$  is effective when  $\overline{RAS}$  is inactivated before  $\overline{CAS}$  is inactivated.

$t_{OFR}$  is effective when  $\overline{CAS}$  is inactivated before  $\overline{RAS}$  is inactivated.

(2) Both  $\overline{RAS}$  and  $\overline{CAS}$  are active or either  $\overline{RAS}$  or  $\overline{CAS}$  is active (in read cycle)

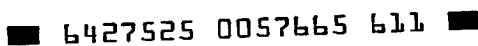
$\overline{WE}$  : active,  $\overline{OE}$  : active ...  $t_{WEZ}$ ,  $t_{WPZ}$  are effective

$\overline{WE}$  : inactive,  $\overline{OE}$  : inactive ...  $t_{OZ}$  is effective.

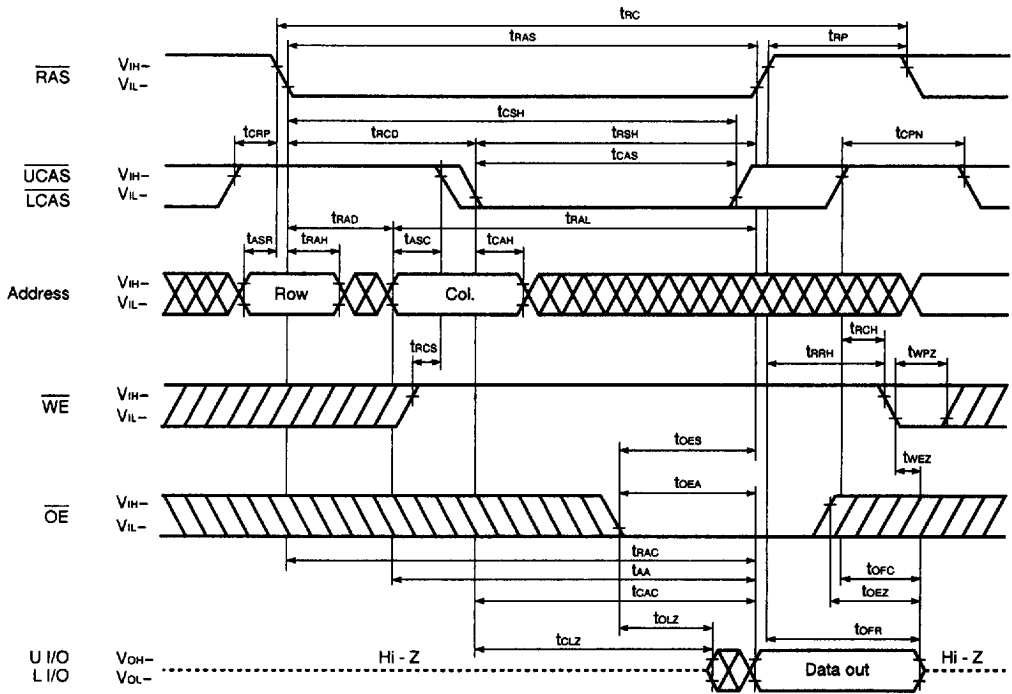
**Refresh Cycle**

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	tCSR	5	-	5	-	5	-	ns	
CAS Hold Time (CAS before RAS Refresh)	tCHR	10	-	10	-	10	-	ns	
RAS Precharge CAS Hold Time	tRPC	5	-	5	-	5	-	ns	
RAS Pulse Width (CAS before RAS Self Refresh Cycle)	tRASS	100	-	100	-	100	-	μs	1
RAS Precharge Time (CAS before RAS Self Refresh Cycle)	tRPS	90	-	110	-	130	-	ns	1
CAS Hold Time (CAS before RAS Self Refresh Cycle)	tCHS	-50	-	-50	-	-50	-	ns	1
WE Hold Time (Hidden Refresh Cycle)	tWHR	15	-	15	-	15	-	ns	

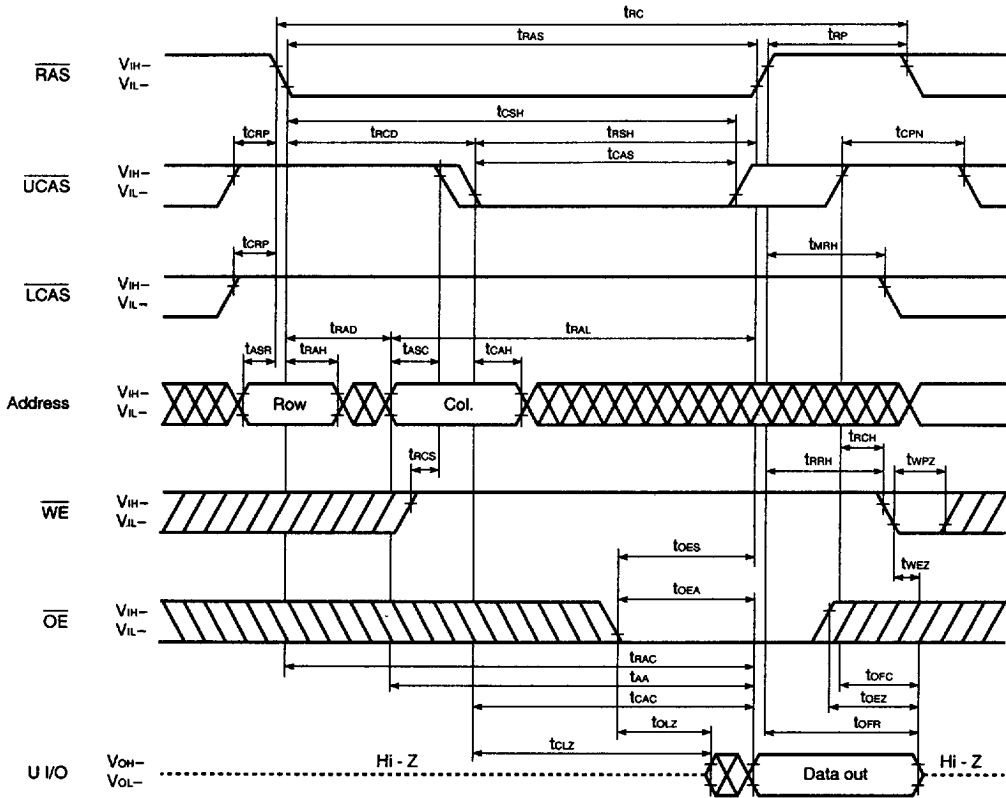
**Note 1.** This specification is applied only to the μPD42S4210A.



Read Cycle



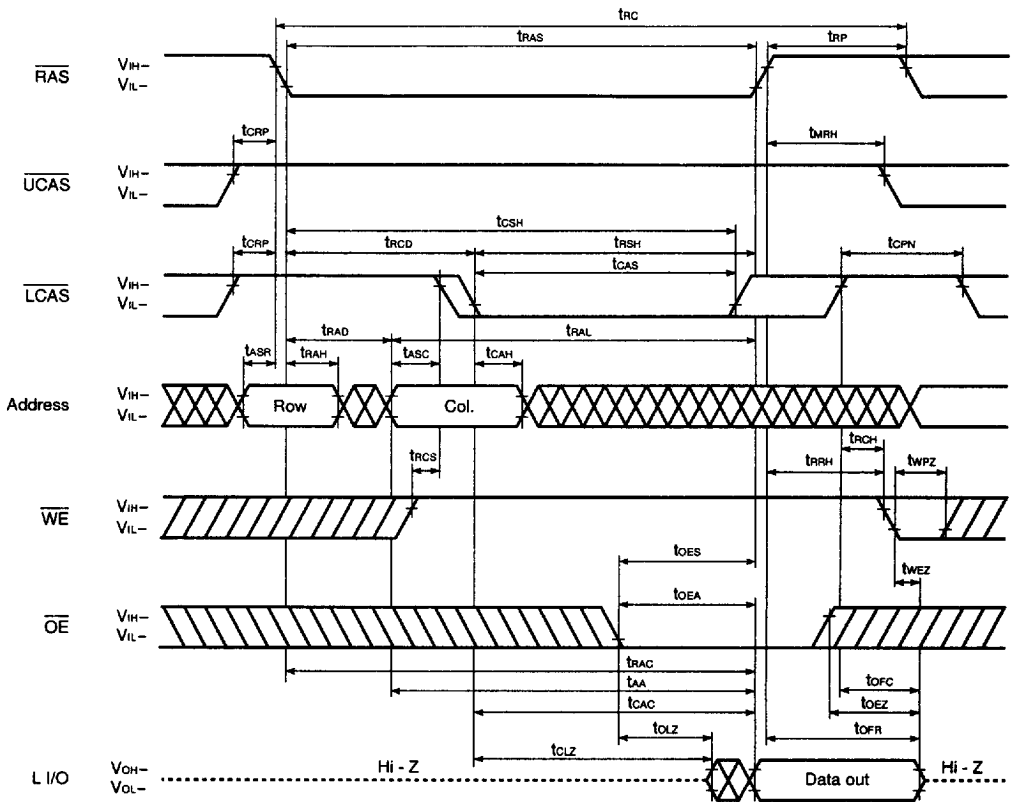
Upper Byte Read Cycle



Remark L I/O : Hi-Z

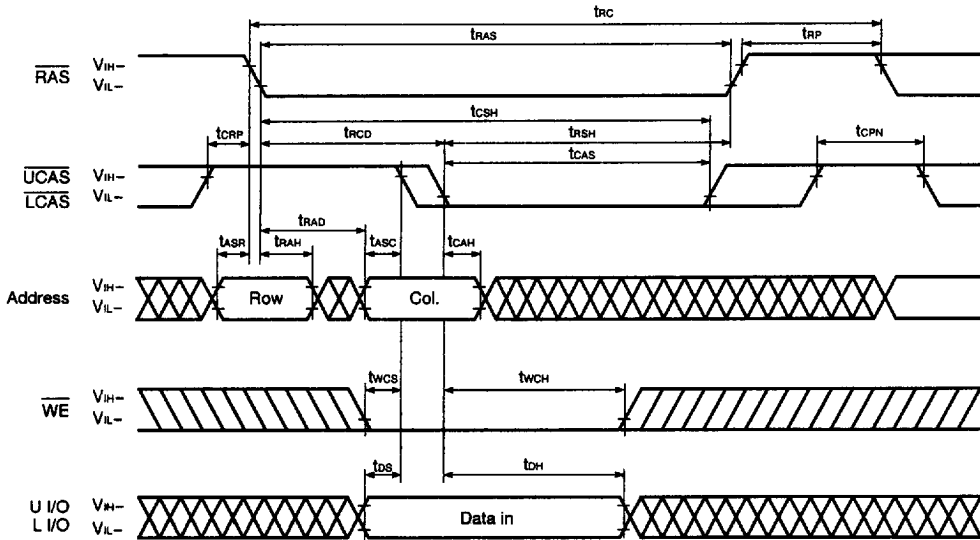


Lower Byte Read Cycle



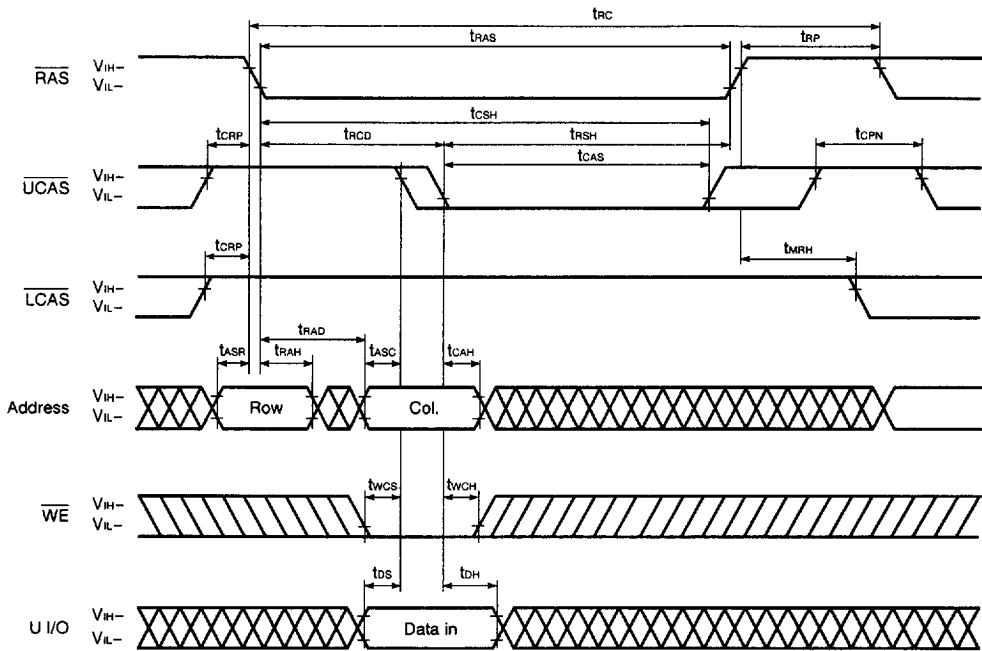
Remark U I/O : Hi-Z

Early Write Cycle



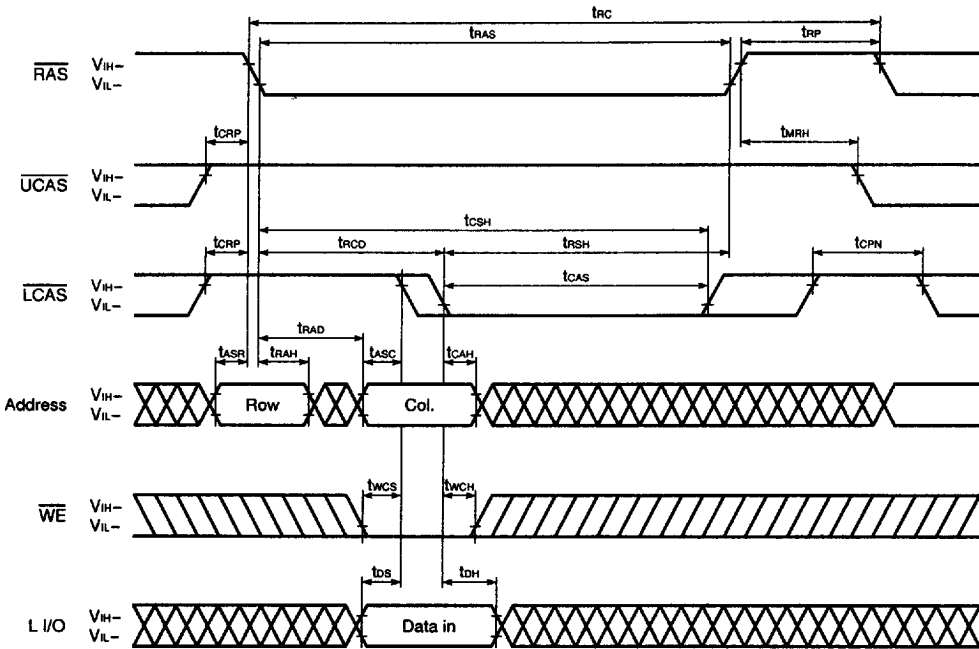
Remark  $\overline{OE}$ : Don't care

Upper Byte Early Write Cycle



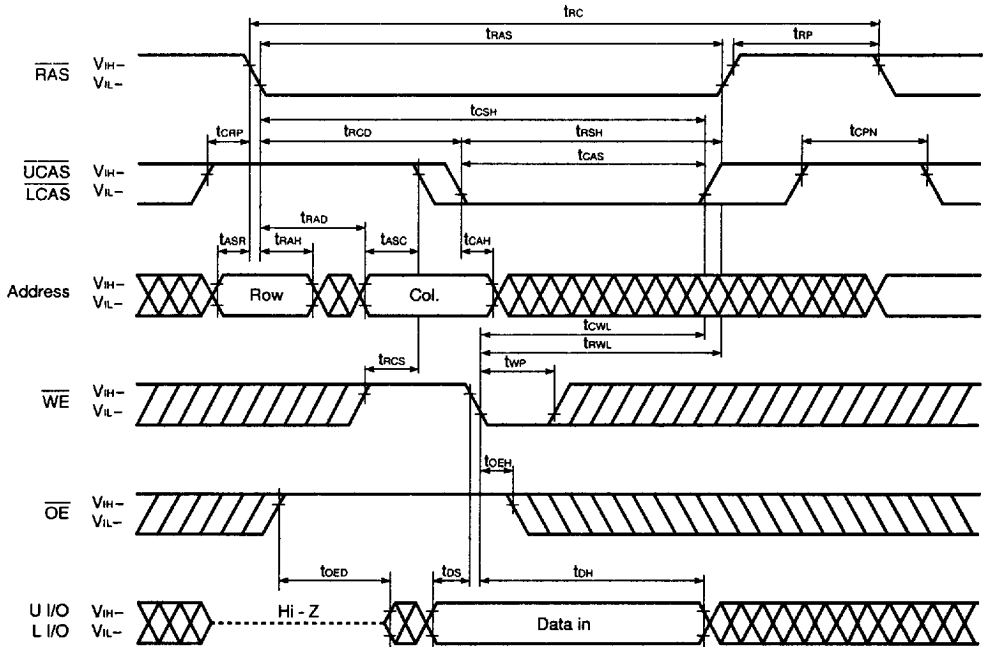
Remark  $\overline{OE}$ , L I/O : Don't care

Lower Byte Early Write Cycle

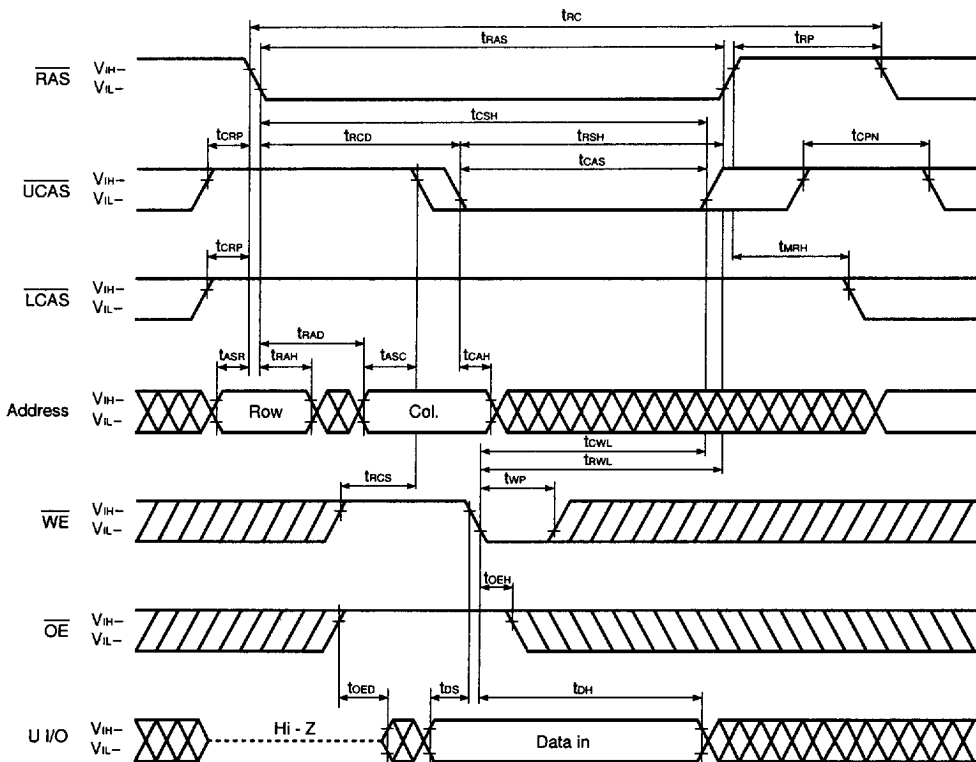


Remark  $\overline{\text{OE}}$ , U I/O : Don't care

Late Write Cycle

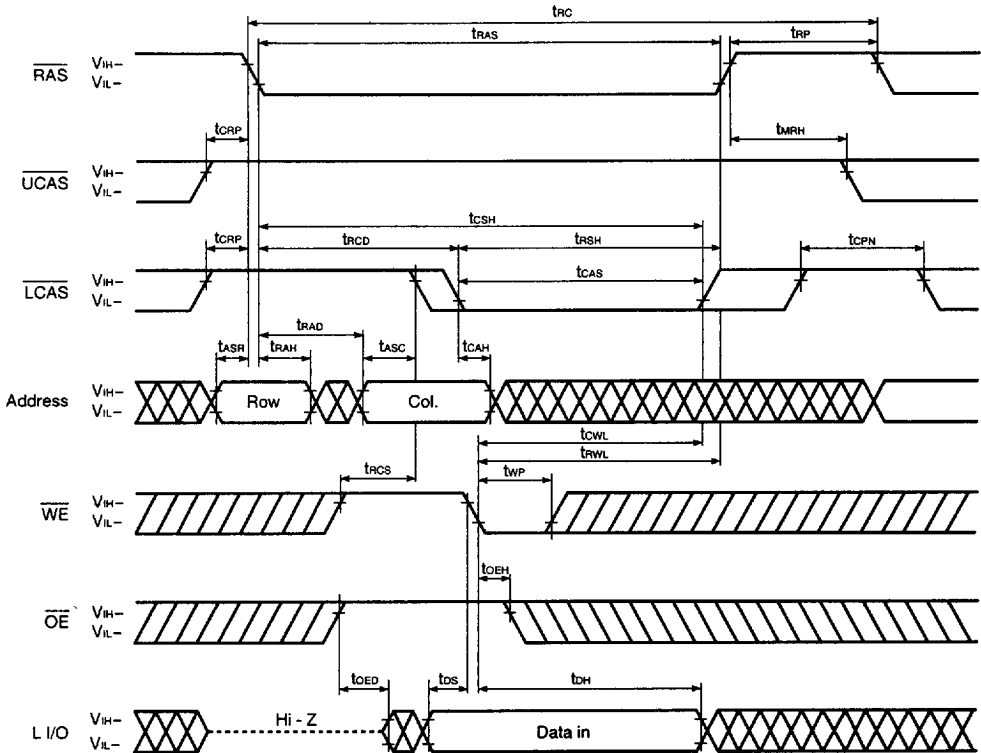


Upper Byte Late Write Cycle



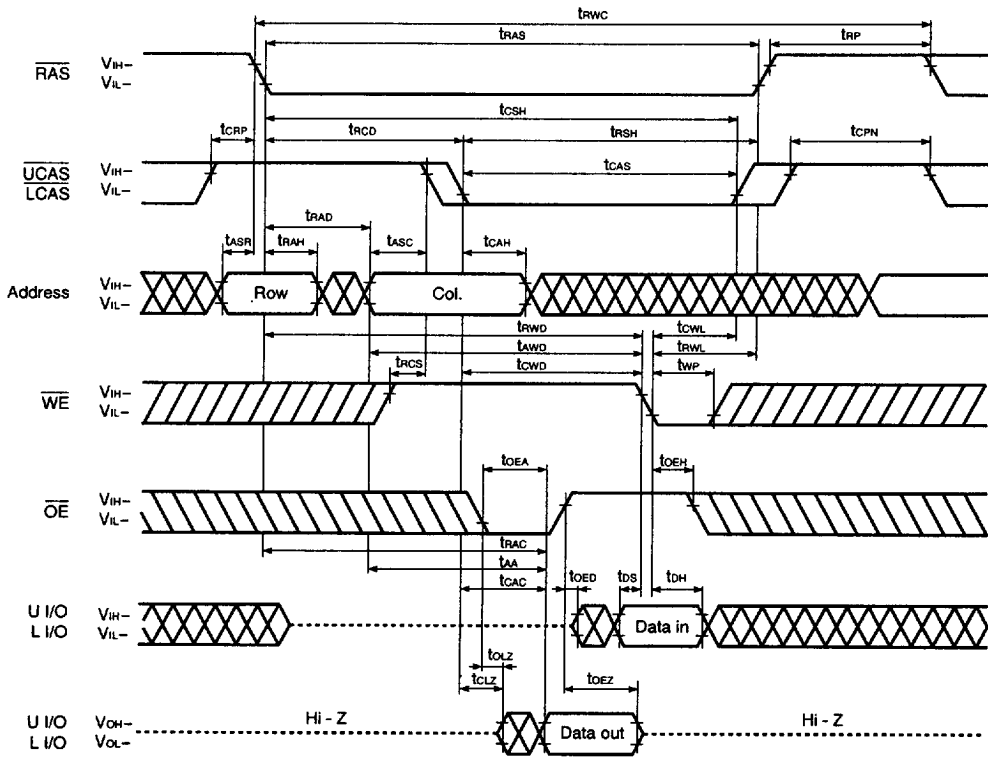
Remark L I/O : Don't care

Lower Byte Late Write Cycle



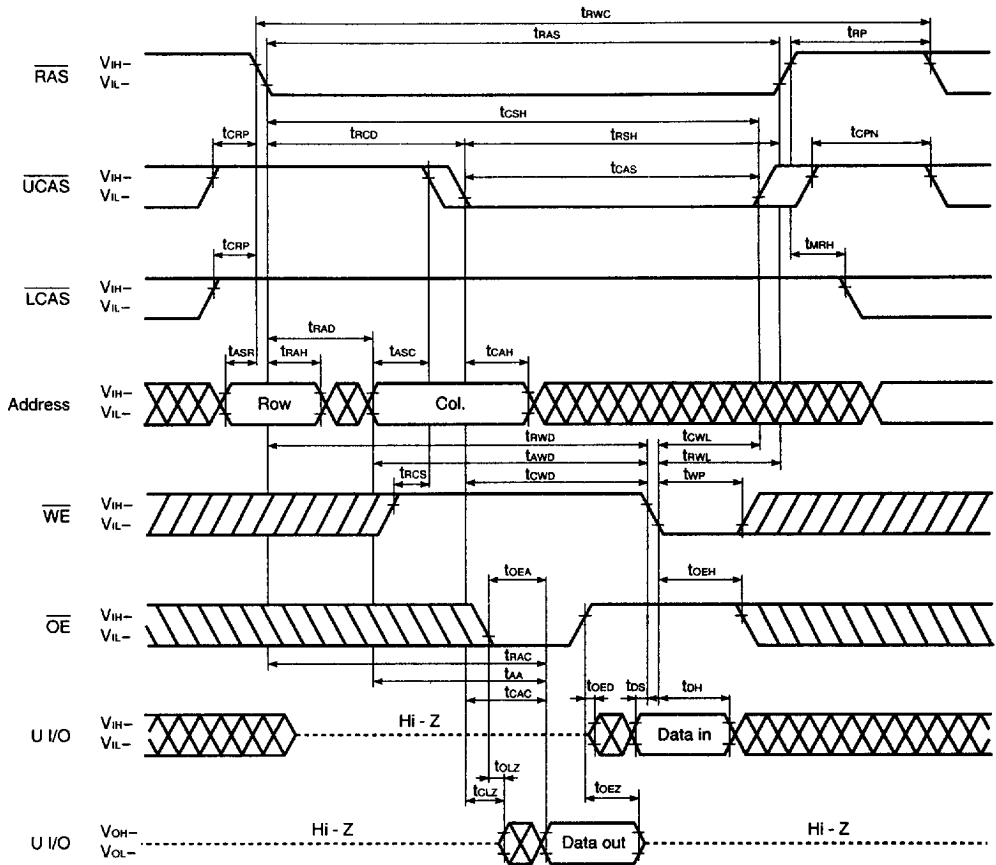
Remark U I/O : Don't care

Read Modify Write Cycle



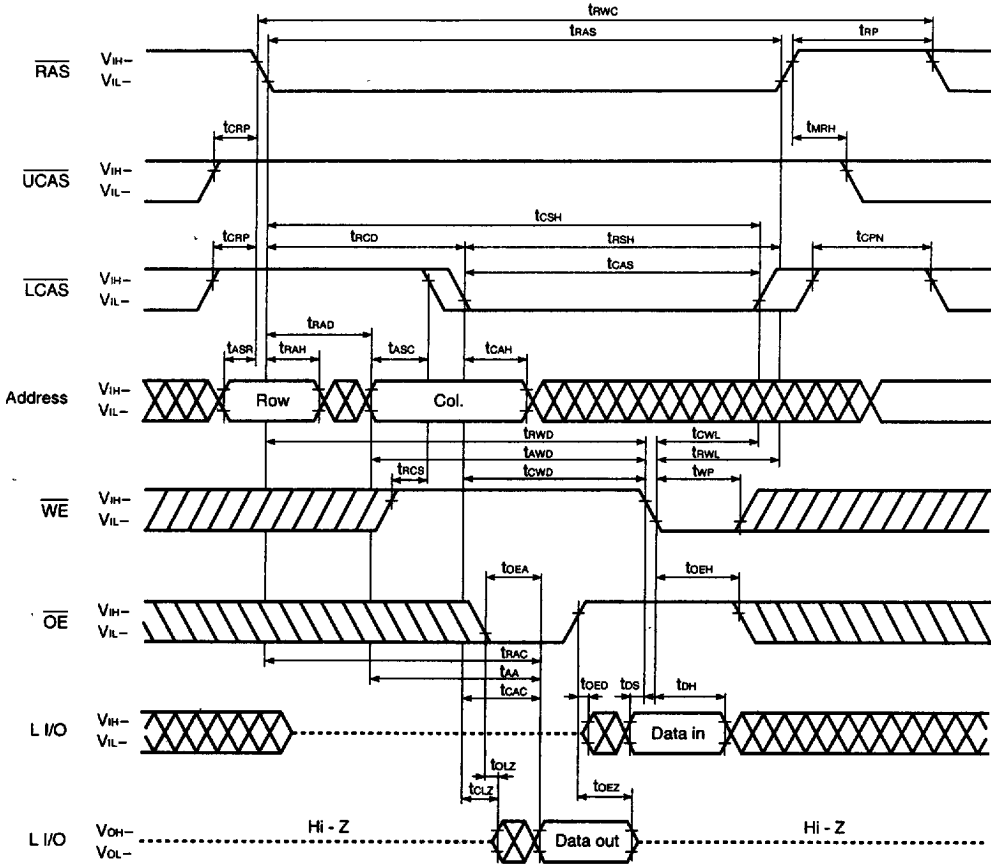


Upper Byte Read Modify Write Cycle



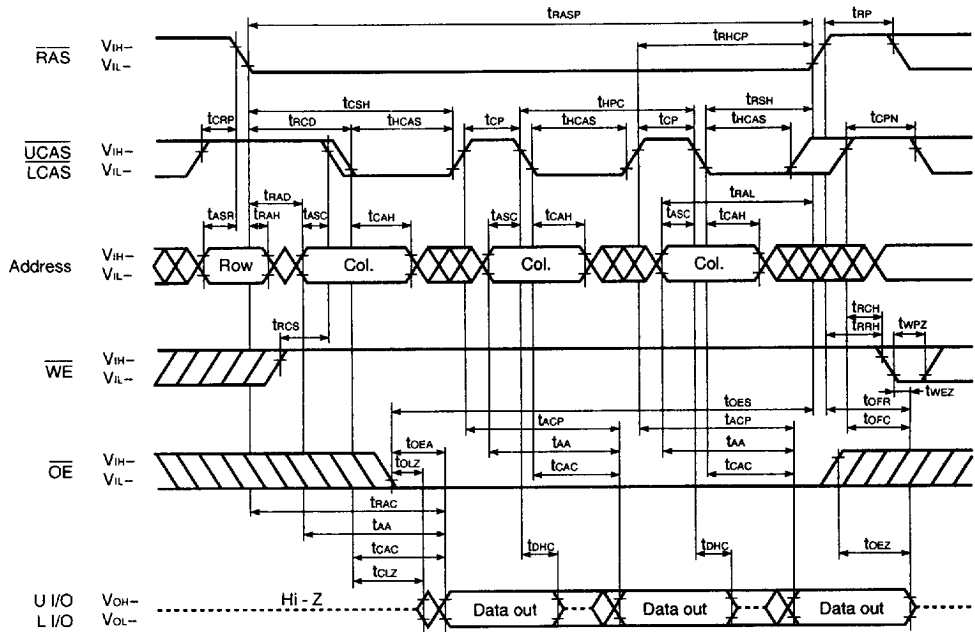
**Remark** In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



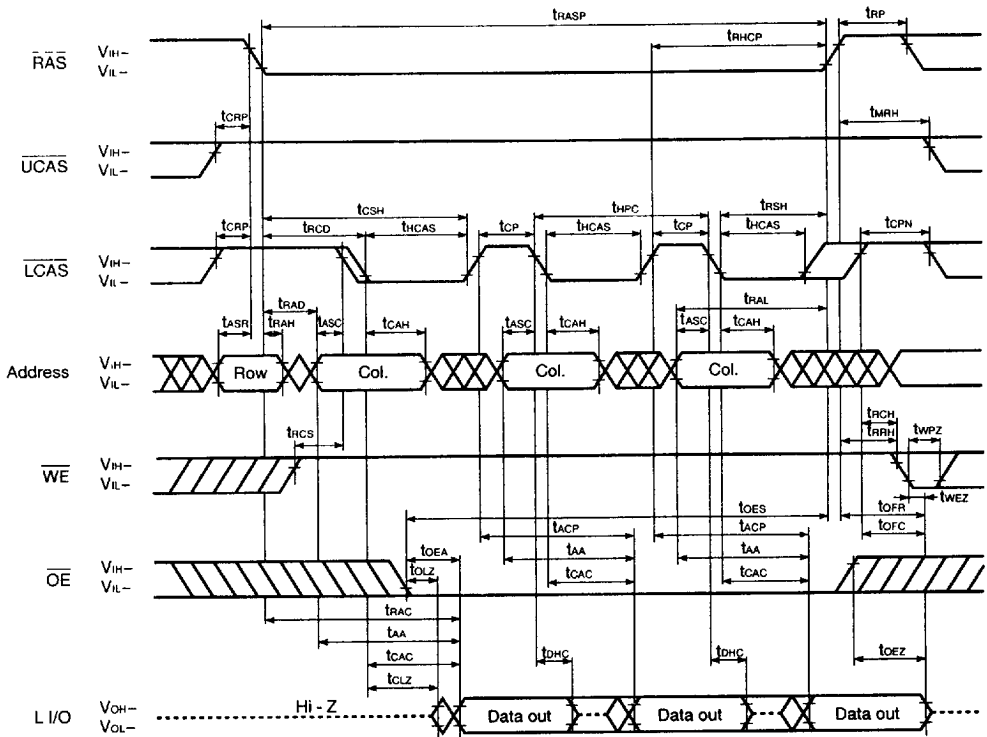
**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Read Cycle





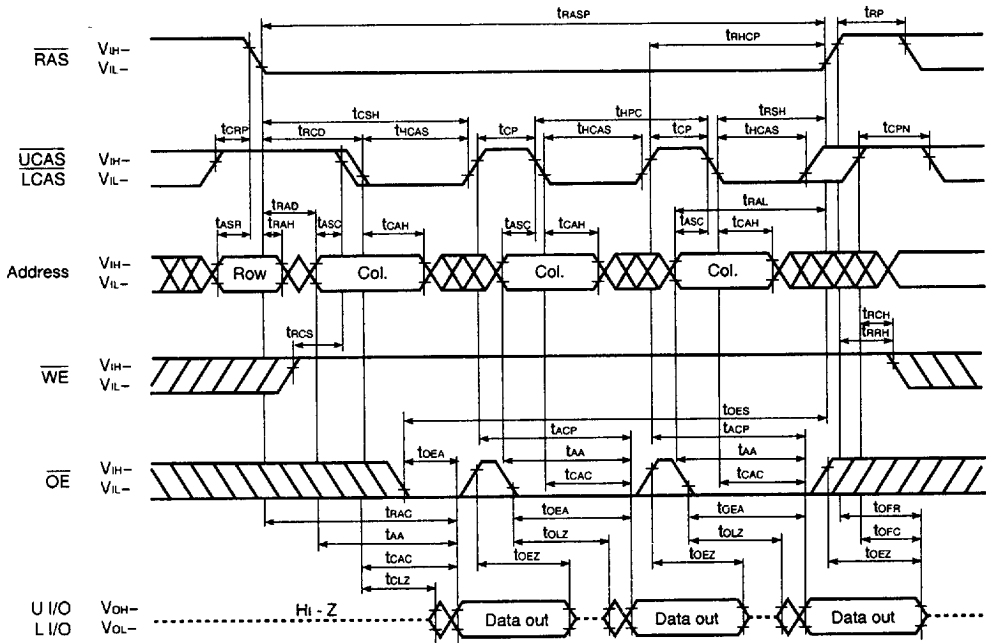
Hyper Page Mode Lower Byte Read Cycle



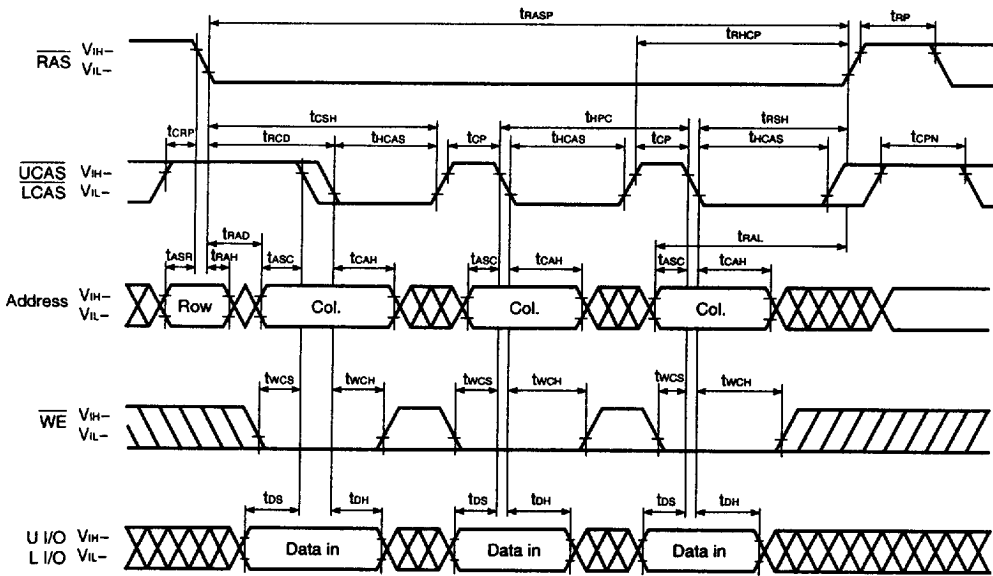
Remark U I/O : Hi-Z



Hyper Page Mode Read Cycle ( $\overline{\text{OE}}$  Control)



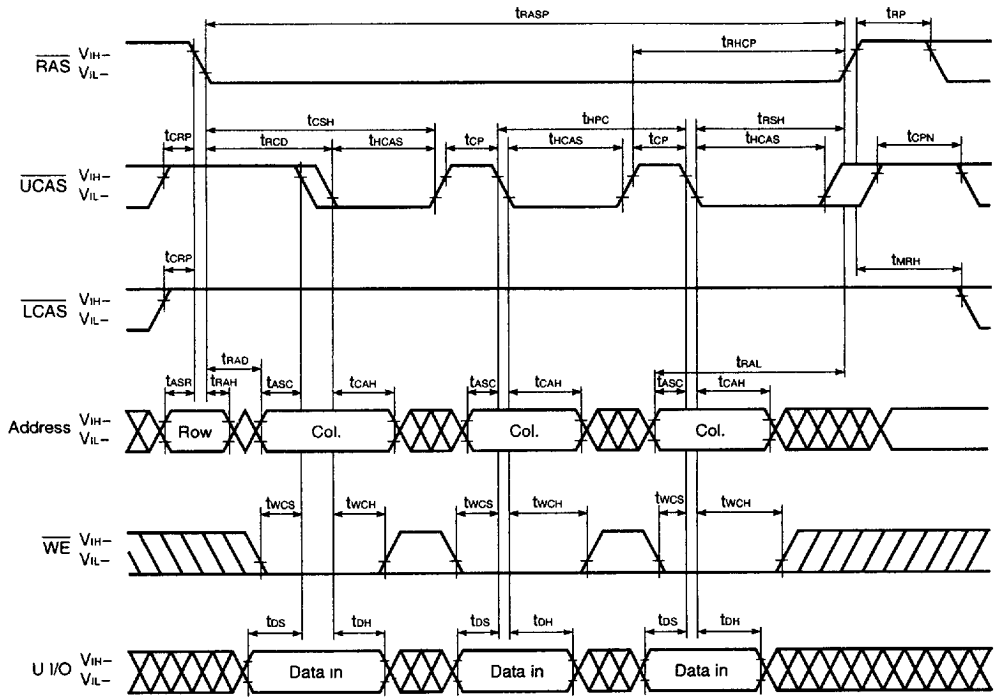
Hyper Page Mode Early Write Cycle



Remark  $\overline{OE}$  : Don't care

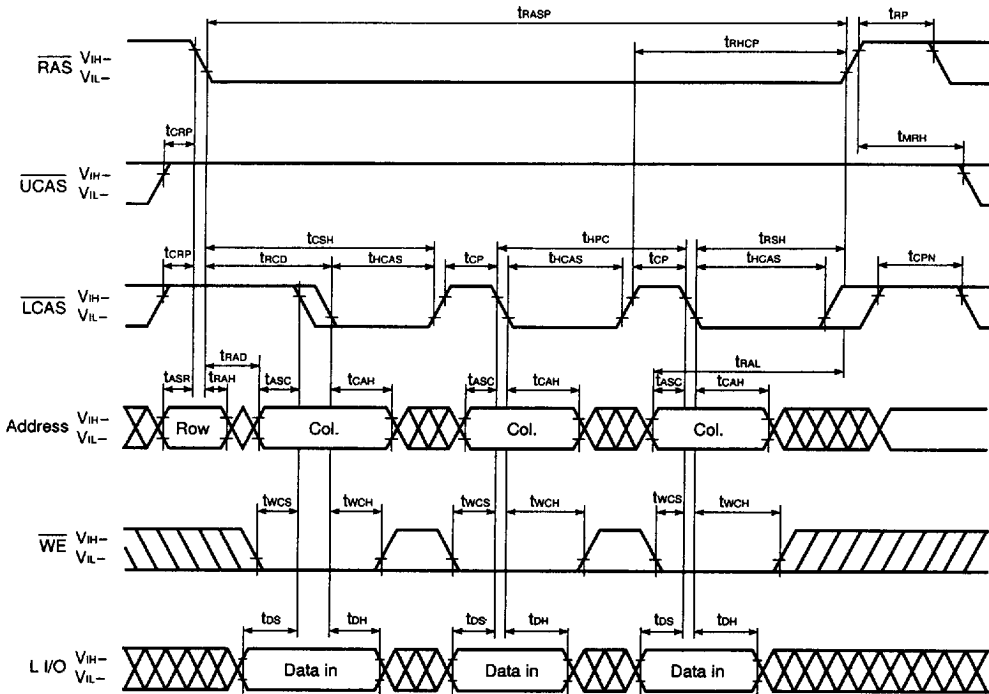


Hyper Page Mode Upper Byte Early Write Cycle



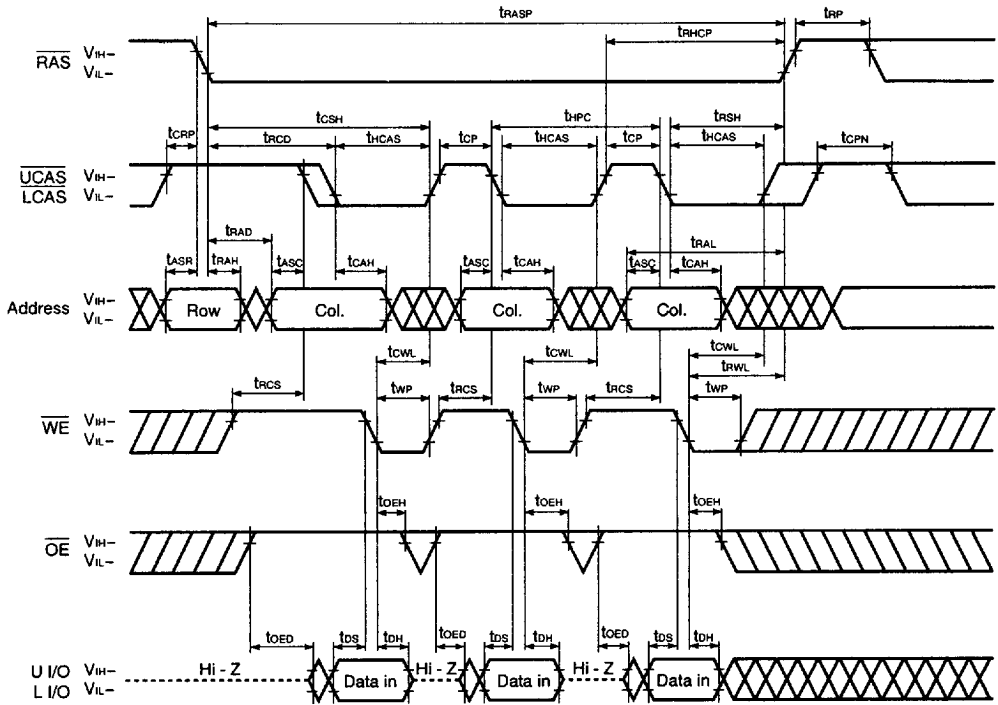
Remark  $\overline{OE}$ , L I/O : Don't care

Hyper Page Mode Lower Byte Early Write Cycle

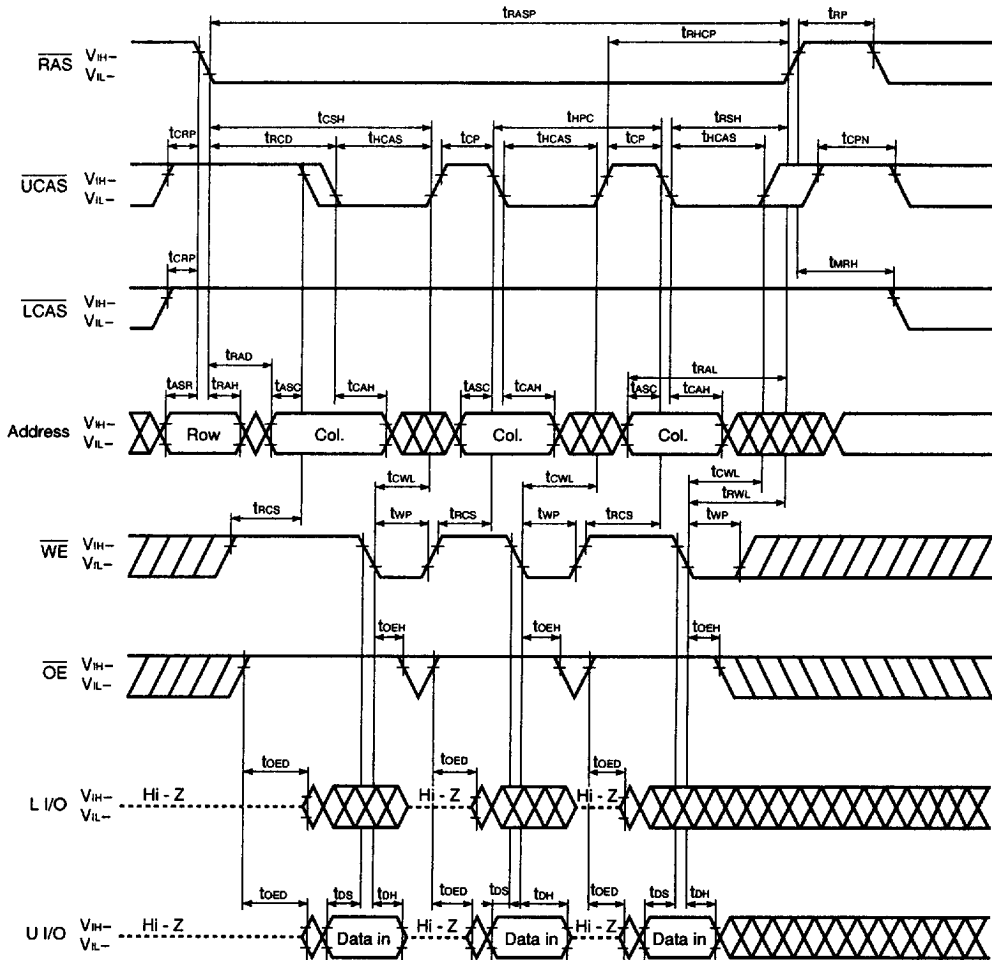


Remark  $\overline{OE}$ , U I/O : Don't care

Hyper Page Mode Late Write Cycle



Hyper Page Mode Upper Byte Late Write Cycle



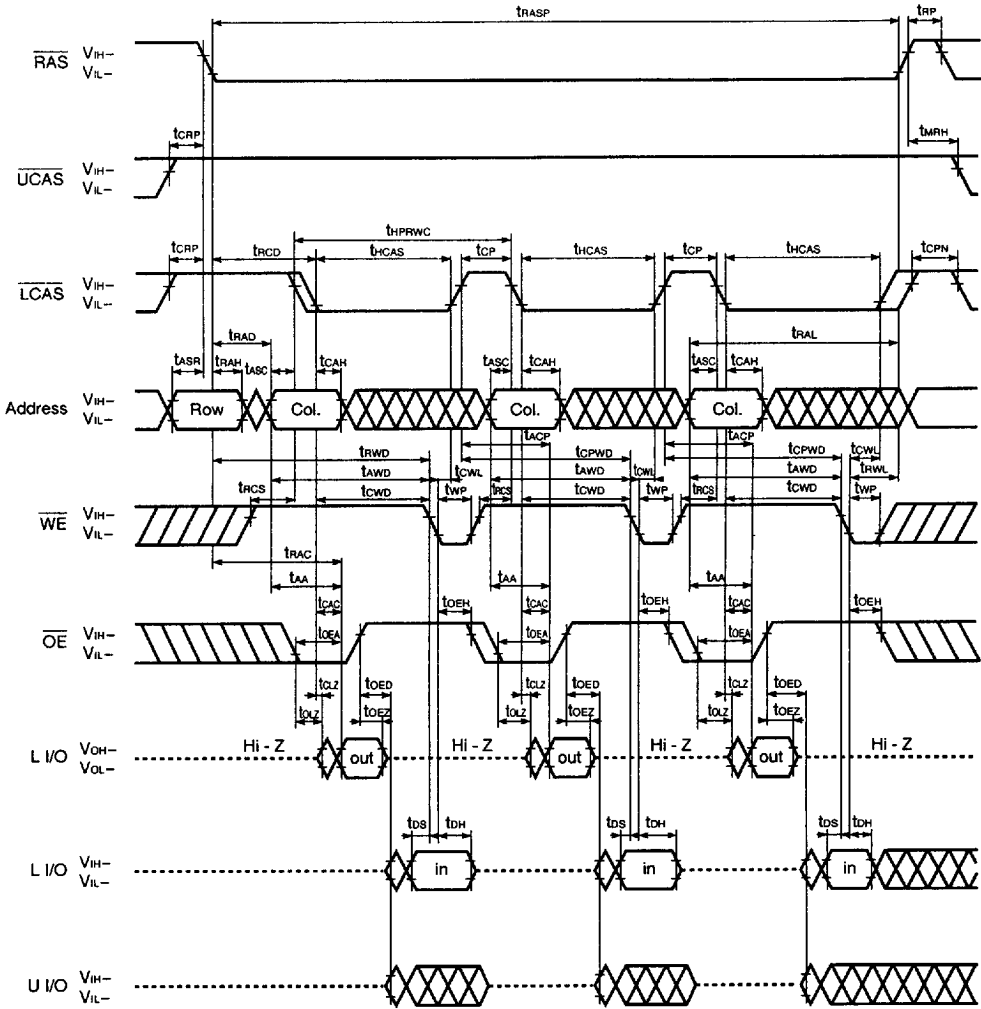
**Remark** In this cycle, the input data to Lower I/O is ineffective.







Hyper Page Mode Lower Byte Read Modify Write Cycle

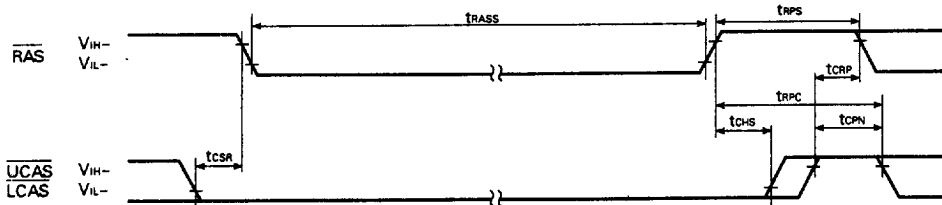


**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.





**CAS Before RAS Self Refresh Cycle (Only for the μPD42S4210A)**



Remark Address,  $\overline{WE}$ ,  $\overline{OE}$  : Don't care L I/O, U I/O : Hi - Z

**Cautions on Use of CAS Before RAS Self Refresh**

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

**(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh**

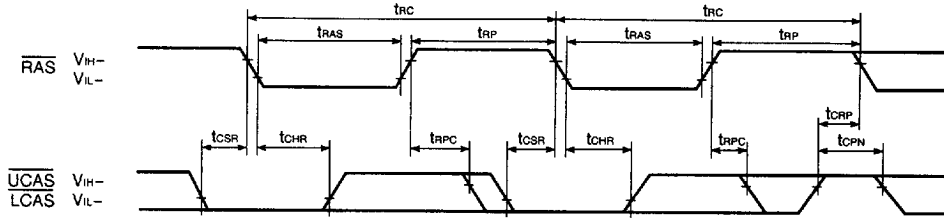
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 512 times within a 8 ms interval just before and after setting CAS before RAS self refresh.

**(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh**

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 512 times within a 8 ms interval just before and after setting CAS before RAS self refresh.

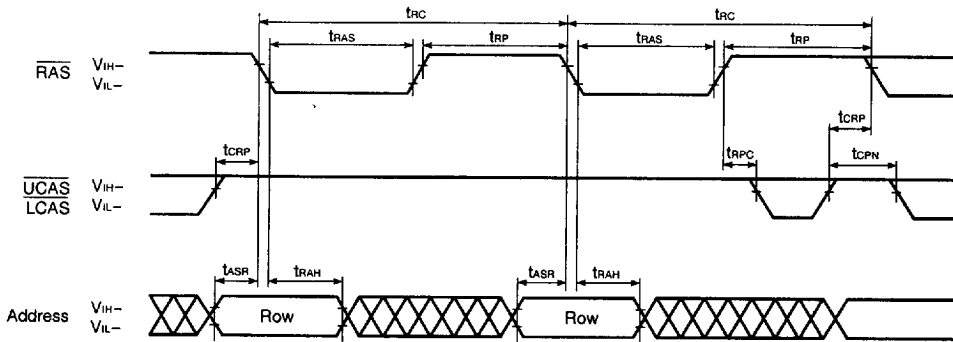
For details, please refer to **How to use DRAM User's Manual**.

**CAS Before RAS Refresh Cycle**



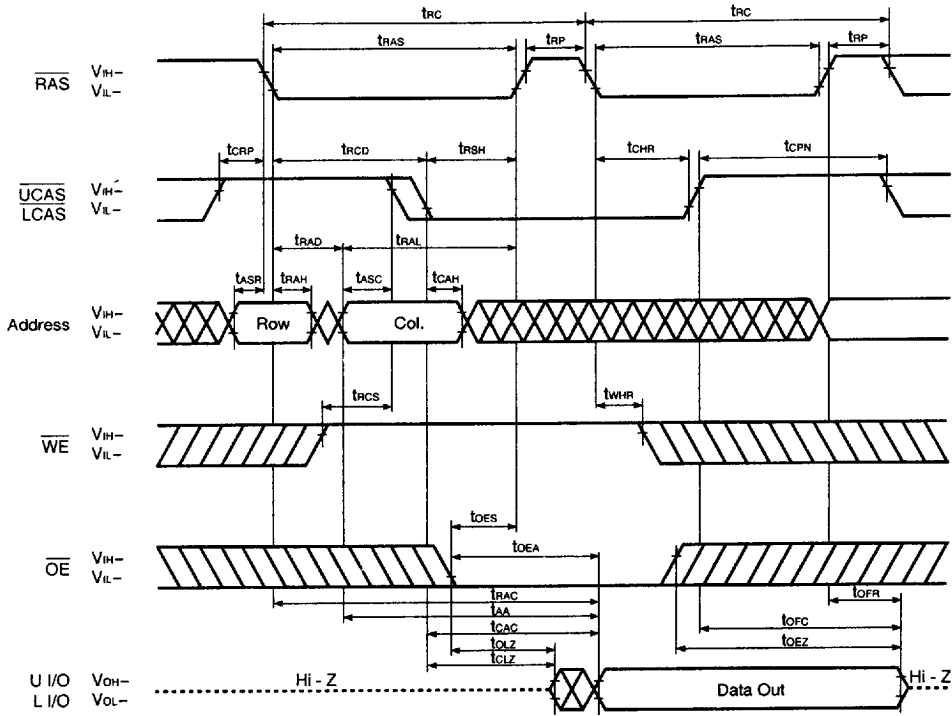
**Remark** Address,  $\overline{WE}$ ,  $\overline{OE}$  : Don't care    L I/O, U I/O : Hi - Z

**RAS Only Refresh Cycle**

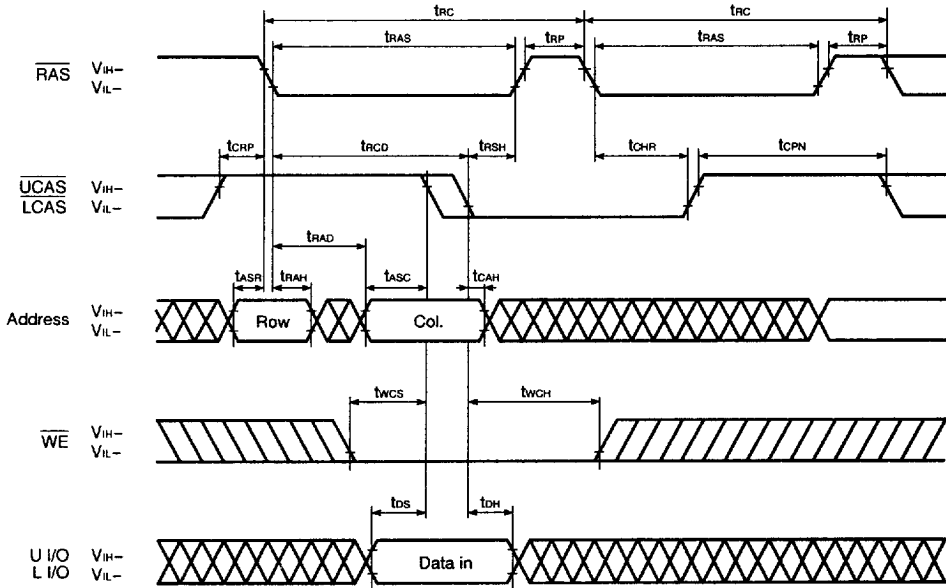


**Remark**  $\overline{WE}$ ,  $\overline{OE}$  : Don't care    L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



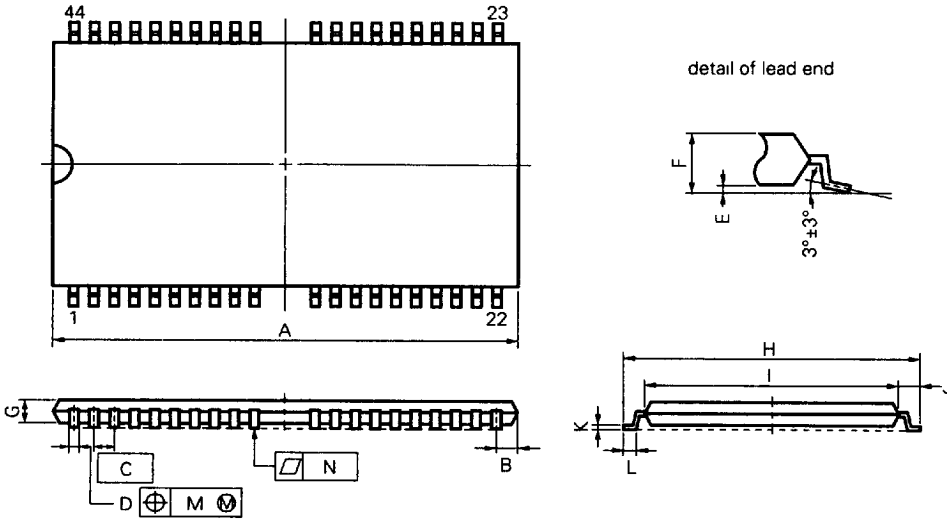
Hidden Refresh Cycle (Write)



Remark  $\overline{OE}$ : Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



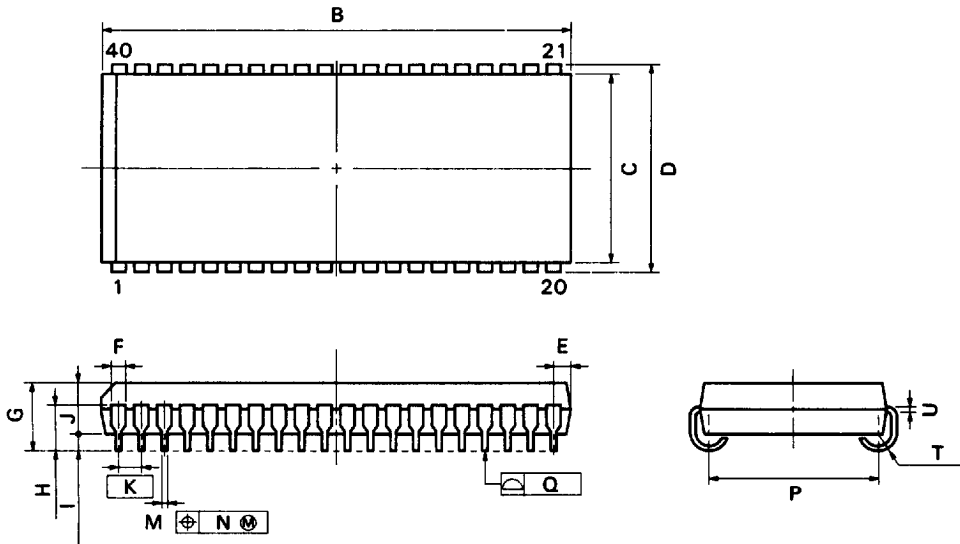
**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S44G5-80-7JF-1

ITEM	MILLIMETERS	INCHES
A	18.81 MAX	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.125 <sup>+0.10</sup> <sub>-0.05</sub>	0.005 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P40LE-400A-1

ITEM	MILLIMETERS	INCHES
B	26.29 <sup>+0.2</sup> <sub>-0.35</sub>	1.035 <sup>+0.008</sup> <sub>-0.014</sub>
C	10.16	0.400
D	11.18 <sup>±0.2</sup>	0.440 <sup>±0.008</sup>
E	1.08 <sup>±0.15</sup>	0.043 <sup>+0.008</sup> <sub>-0.007</sub>
F	0.7	0.028
G	3.5 <sup>±0.2</sup>	0.138 <sup>±0.008</sup>
H	2.4 <sup>±0.2</sup>	0.094 <sup>+0.008</sup> <sub>-0.008</sub>
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 <sup>±0.10</sup>	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	9.4 <sup>±0.20</sup>	0.370 <sup>±0.008</sup>
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 <sup>+0.10</sup> <sub>-0.08</sub>	0.008 <sup>+0.004</sup> <sub>-0.003</sub>

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD42S4210A, 424210A.

**Types of Surface Mount Device**

$\mu$ PD42S4210AG5-XX, 424210AG5-XX : 44-pin Plastic TSOP (II) (400 mil)

$\mu$ PD42S4210ALE-XX, 424210ALE-XX : 40-pin Plastic SOJ (400 mil)