DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD16661A

160-OUTPUT LCD COLUMN (SEGMENT) DRIVER WITH RAM

The μPD16661A is a column (segment) driver containing a RAM capable of full-dot LCD drive. With 160 outputs, this driver has an on-chip display RAM of 160 × 240 × 2 bits. The driver can be combined with the μPD16666A to display from 1/8 VGA to VGA (640 × 480 dots).

The μPD16661A is upwardly compatible with the μPD16661.

FEATURES

- Display RAM incorporated : 160 × 240 × 2 bits
- Logic voltage : 3.0 to 3.6 V
- Duty : 1/240
- Output count : 160 outputs
- Capable of gray scale display : 4 gray scales (frame thinning-out)
- Memory management : packed pixel system
- 8/16-bit data bus

ORDERING INFORMATION

Part Number	Package
μPD16661AN-×××	TCP (TAB)
★ μPD16661AN-051	Standard TCP (OLB : 0.2 mm-pitch, pliable-output leads)

Remark The TCP package is custom made, so contact an NEC sales representative with your requirements.

Document No. S11498EJ3V0DS00 (3rd edition)
Date Published November 1998 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

PIN NAMES

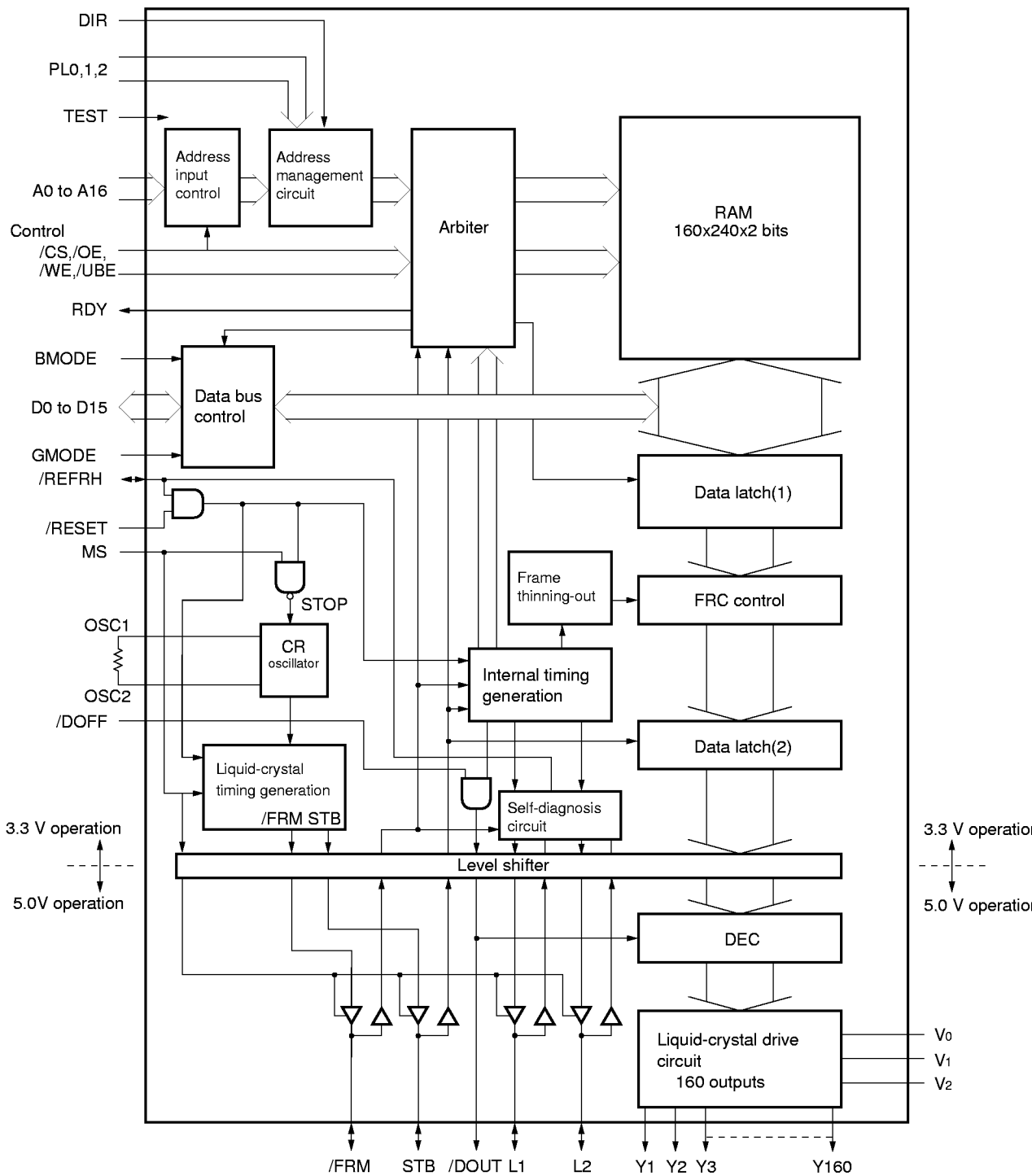
Classification	Pin Name [Note]	I/O	Pad No.	Function
CPU interface (3.3 V)	D0 to D15	I/O		Data bus : 16 bits
	A0 to A16	I		Address bus : 17 bits
	/CS	I		Chip select
	/OE	I		Read signal
	/WE	I		Write signal
	/UBE	I		Upper byte enable
	RDY	O		Ready signal to CPU (Ready state at "H")
Control signals (3.3 V)	PL0	I		Specifies the LSI placement positions (No. 0 to 7)
	PL1	I		Specifies the LSI placement positions (No. 0 to 7)
	PL2	I		Specifies the LSI placement positions (No. 0 to 7)
	DIR	I		Specifies the liquid-crystal panel placement direction
	MS	I		Master/slave selection pin (Master mode at "H")
	BMODE	I		Data bus bit selection pin ("H" = 8 bits, "L" = 16 bits)
	GMODE	I		Gray scale data weight reverse switching (When data = [1,1], "L" = black, "H" = white)
	/REFRH	I/O		Self-diagnosis reset pin (wired-OR connection)
	TEST	I		Test pin ("H" = test mode, on-chip pull-down resistor)
	/RESET	I		Reset signal
	/DOFF	I		Display OFF input signal
	OSC1	–		Oscillator externally-attached resistor pin
	OSC2	–		Oscillator externally-attached resistor pin
	STB	I/O		Column drive signal (MS pin "H" = output, MS pin "L" = input)
	/FRM	I/O		Frame signal (MS pin "H" = output, MS pin "L" = input)
5.0 V	L1	I/O		Row driver drive level selection signal (1st line)
	L2	I/O		Row driver drive level selection signal (2nd line)
	/DOUT	O		Display OFF output signal
Liquid-crystal drive	Y1 to Y160	O		Liquid-crystal drive output
Power supplies	GND	–		Ground (two pins for V_{CC1} system , three pins for V_{CC2} system)
	V_{CC1}	–		5-V power supply
	V_{CC2}	–		3.3-V power supply
	V_0	–		Liquid-crystal drive analog power supply
	V_1	–		Liquid-crystal drive analog power supply
	V_2	–		Liquid-crystal drive analog power supply

Note 3.3-V pin : D0 to D15, A0 to A16, /CS, /OE, /WE, /UBE, RDY, BMODE, GMODE, PL0, PL1, PL2, DIR, OSC1, OSC2, /RESET, /DOFF, TEST, MS

5-V pin : STB, /FRM, L1, L2, /DOUT

★ **Remark** /xxx indicates active low signal.

BLOCK DIAGRAM



1. BLOCK FUNCTIONS

(1) Address management circuit

The address management circuit converts the addresses transferred from the system via A0 to A16 into addresses compatible with the memory map of the on-chip RAM.

This function can be used to address up to VGA size (480 × 640 dots) with 8 of these LSIs, thus making it possible to configure a liquid-crystal display system without difficulty.

(2) Arbiter

The arbiter adjusts the contention between the RAM access from the system and the RAM read on the liquid-crystal drive side.

(3) RAM

Static RAM (single port) of 160 × 240 × 2 bits

(4) Data bus control

The data bus controls the data transfer directions by means of Read/Write from the system.

The mode can be switched from 8 bits to 16 bits by the BMODE pin, and the relation between the display data and the gray scale can be switched by the GMODE pin.

(5) Frame thinning-out control

The frame thinning-out control indicates the four gray scales with three thinning-out frames. The thinning-out method can be changed in units of 9 pixels (3 columns × 3 lines).

(6) Internal timing generation

The internal timing to each block is generated from the /FRM and STB signals.

(7) CR oscillator

In master mode, this oscillator generates the clock that is the reference for the frame frequency. The frame frequency is one 484th (1/484) of this oscillation. For example, if the frame frequency is 80 Hz, an oscillation frequency of 38.72 kHz is necessary. As the CR has a built-in capacitance, adjust the required oscillation frequency with an externally attached resistor.

In slave mode, oscillation is stopped.

(8) Liquid-crystal timing generation

In master mode, /FRM (the frame signal) and STB (the column drive signal strobe) are generated.

(9) FRC control

This circuit realizes the four gray-scale displays.

(10) Data latch (1)

This data latch reads and latches 160-pixel data from the RAM.

(11) Data latch (2)

This data latch synchronizes with the STB signal and latches 160-pixel data.

(12) Level shifter

The level shifter converts the voltage from the operating voltage of the internal circuit (3.3 V) to the voltage of the liquid-crystal drive circuit and row driver interface (5.0 V).

(13) DEC

The DEC decodes the gray scale display data to make it compatible with the liquid-crystal drive voltages V0, V1, and V2.

(14) Liquid-crystal drive circuit

This circuit selects one of the display OFF signal (/DOFF)-compatible liquid-crystal drive power supplies V0, V1, or V2, and generates the liquid-crystal applied voltage.

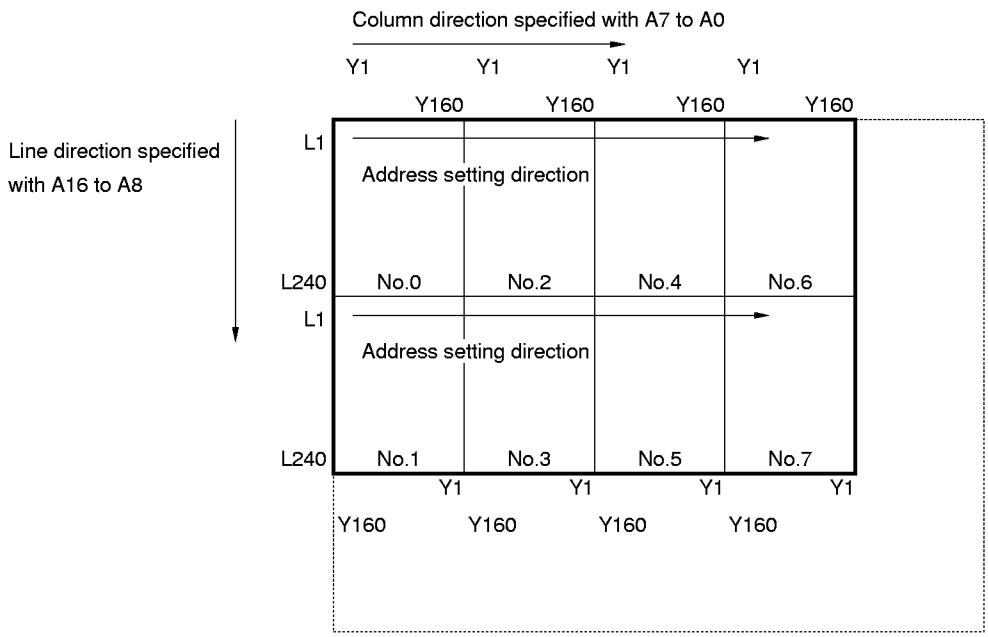
(15) Self-diagnosis circuit

This circuit automatically detects any occurrence of an operation timing lag between the master chip and the slave chip that has been caused by outside noise, and sends a refresh signal to all the column drivers.

2. MEMORY MAP

Address A16 ..... A0						Description
0	0	0	0	0	H	Display data of Nos. 0, 2, 4, and 6
			:			
			:			
0	F	0	0	0	H	Display data of Nos. 1, 3, 5, and 7
			:			
			:			
1	D	F	A	0	H	Unused
			:			
1	F	F	F	F	H	

Address map image diagram (Example of VGA-size configuration)



3. DATA BUSES

The method for lining up byte data on the data bus line is essentially the Little Endian system adopted by NEC and Intel Corp.

3.1 16-bit data bus (BMODE = L)

Byte unit access

The address setting direction → is as shown on the right.

D0 to D7	D8 to D15
00000H	00001H
00002H	00003H
00004H	00005H
:	:
:	:

Word unit access

The address setting direction → is as shown on the right.

D0 to D7	D8 to D15
00000H	
00002H	
00004H	
:	
:	

For access from the system to be performed in word units (16 bits), or byte units (8 bits), /UBE (upper-byte enable) and A0 are used to show whether valid data is in the bytes of either (or both) D0 to D7 or D8 to D15.

/CS	/OE	/WE	/UBE	A0	MODE	I/O	
						D0 to D7	D8 to D15
H	X	X	X	X	Not selected	Hi-z	Hi-z
L	L	H	L	L	Read	Dout	Dout
			L	H		Hi-z	Dout
			H	L		Dout	Hi-z
L	H	L	L	L	Write	Din	Din
			L	H		X	Din
			H	L		Din	X
L	H	H	X	X	Output	Hi-z	Hi-z
L	X	X	H	H	disable	Hi-z	Hi-z

Remark X : Don't care, Hi-z : High impedance

3.2 8-bit data bus (BMODE = H)

The address setting direction → is as shown on the right.

D0 to D7
00000H
00001H
00002H
:
:

/CS	/OE	/WE	MODE	I/O	
				D0 to D7	D8 to D15
H	X	X	Not selected	Hi-z	**Note**
L	L	H	Read	Dout	**Note**
L	H	L	Write	Din	**Note**
L	H	H	Output disable	Hi-z	**Note**

Note When BMODE = H, D8 to D15 and /UBE are pulled down internally, so either leave them open, or connect them to the GND.

Remark X : Don't care, Hi-z : High impedance

4. RELATIONSHIP BETWEEN DATA BITS AND PIXELS

Because the display is in four gray scales, each pixel consists of two bits.

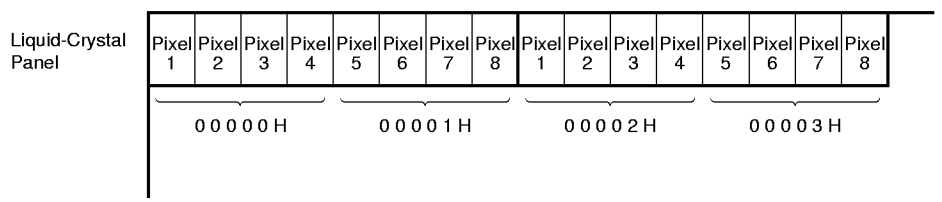
The RAM is configured with four pixels (8 pixels per word) using the packed pixel system.

(1) BMODE = L

In byte unit access (8 bits)

D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15
Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

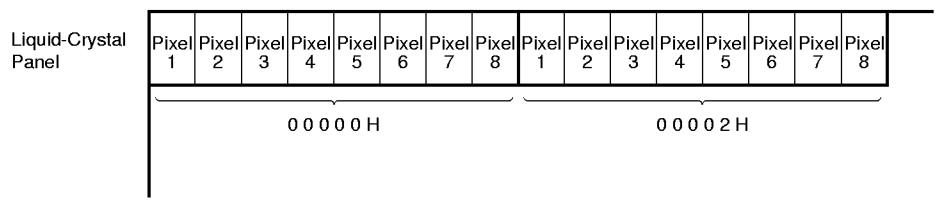
00000H 00001H



In word unit access (16 bits)

D0 D1	D2 D3	D4 D5	D6 D7	D8 D9	D10 D11	D12 D13	D14 D15
Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

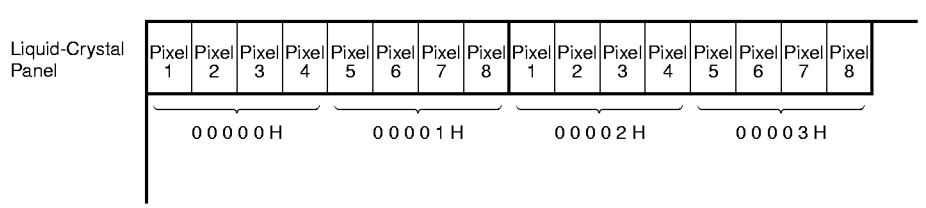
00000H



(2) BMODE = H

D0 D1	D2 D3	D4 D5	D6 D7	D0 D1	D2 D3	D4 D5	D6 D7
Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

00000H 00001H



5. RELATIONSHIP BETWEEN DISPLAY DATA AND GRAY-SCALE LEVEL

(1) GMODE = L

D_n	D_{n+1}	Gray Scale Level	Display State	Liquid-Crystal State
0	0	0		OFF ↓ ON
1	0	1		
0	1	2		
1	1	3		

Display OFF State

(2) GMODE = H

D_n	D_{n+1}	Gray Scale Level	Display State	Liquid-Crystal State
1	1	3		OFF ↓ ON
0	1	2		
1	0	1		
0	0	0		

Display OFF State

6. LSI PLACEMENT AND ADDRESS MANAGEMENT

Addresses can be managed to allow the use of a maximum of eight μPD16661A devices for configuring a liquid-crystal display of up to VGA size (480 × 640 dots).

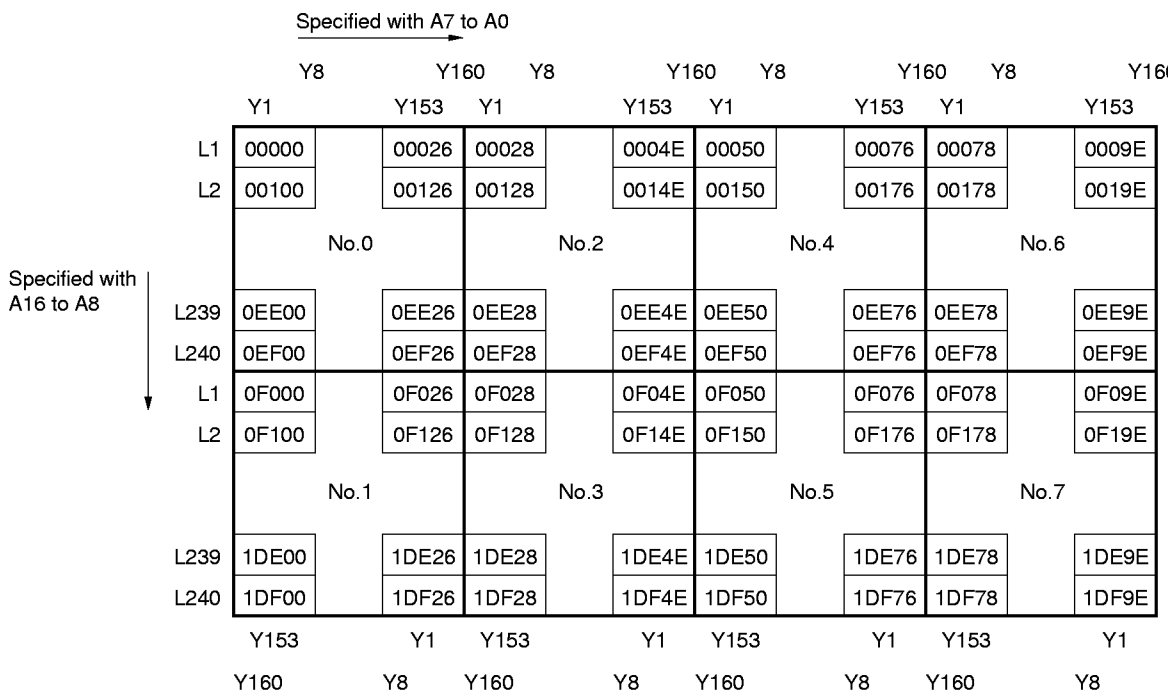
Up to eight of these LSIs can be connected to the same data bus and to the /CS, /WE, and /OE pins, which are shared.

One screen of the liquid-crystal display can be treated as one memory area in the system, so it is not necessary to decode more than one μPD16661A device.

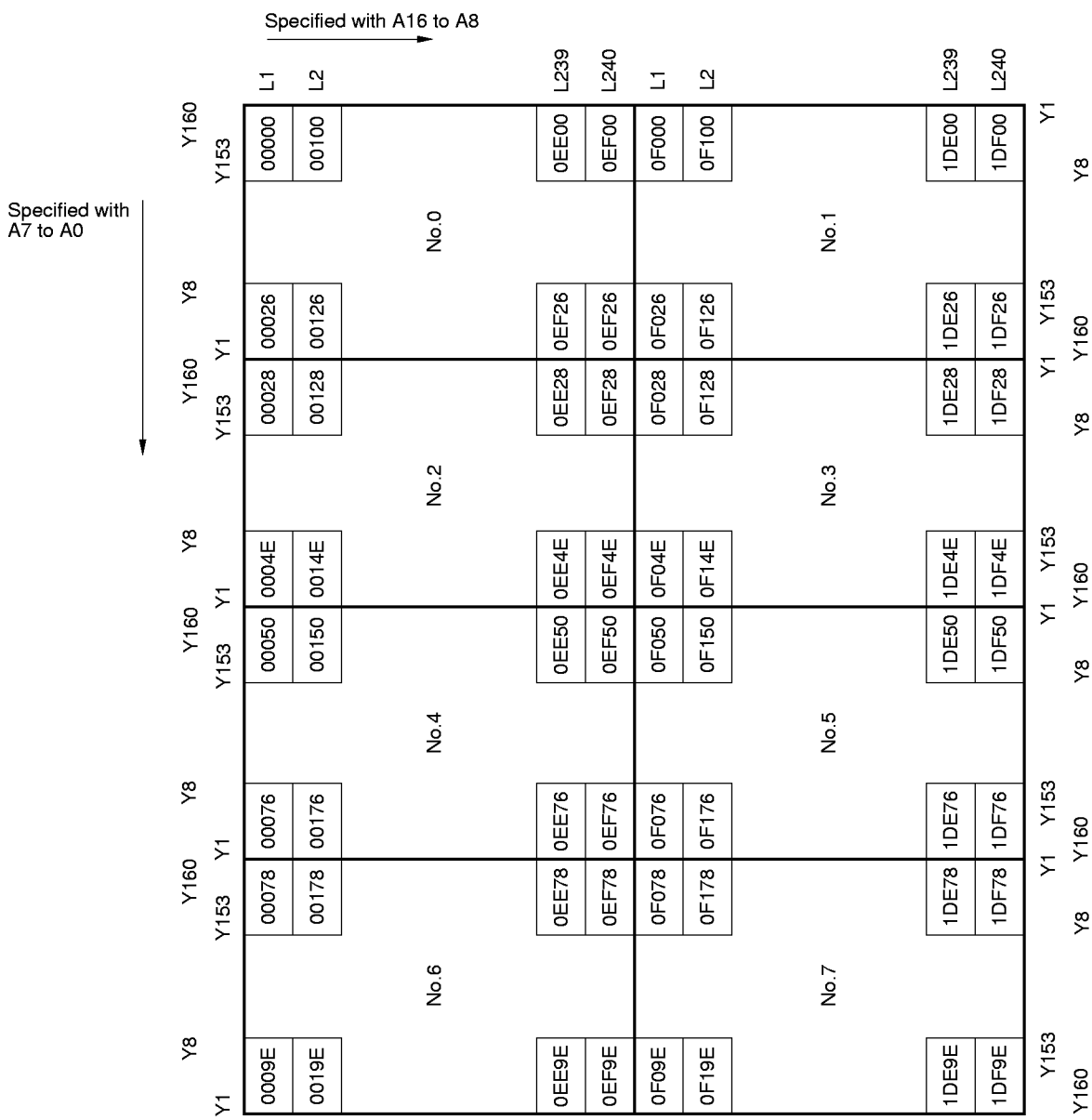
The PL0, PL1, and PL2 pins are used to specify the LSI No. and determine the LSI placement. The DIR pin is used to determine the direction (perpendicular, lateral) of the liquid-crystal display.

PL2	PL1	PL0	LSI No.
0	0	0	No. 0
0	0	1	No. 1
0	1	0	No. 2
0	1	1	No. 3
1	0	0	No. 4
1	0	1	No. 5
1	1	0	No. 6
1	1	1	No. 7

Landscape VGA size address **DIR = "0"**



Portrait VGA size address **DIR = "1"**

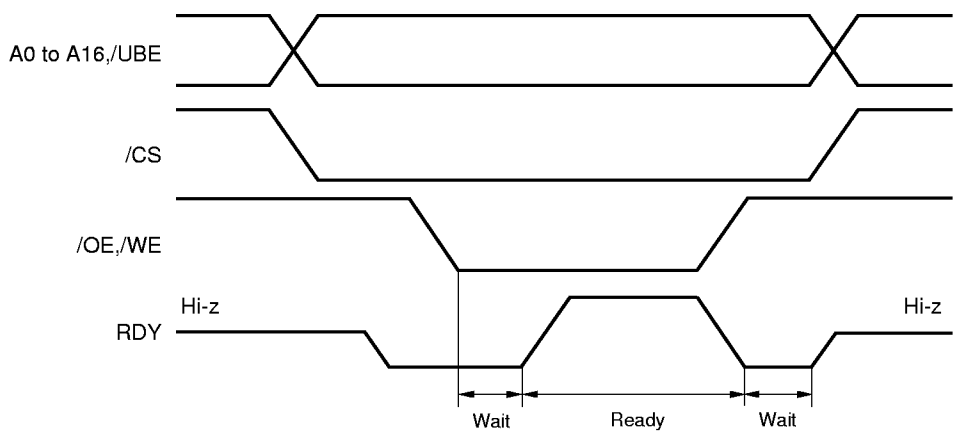


7. CPU INTERFACE

7.1 Function of the RDY (Ready) pin

The on-chip RAM uses a single-port RAM. In order to avoid conflict between accessing from the CPU side and reading on the liquid-crystal drive side, the RDY pin performs a wait operation on the CPU.

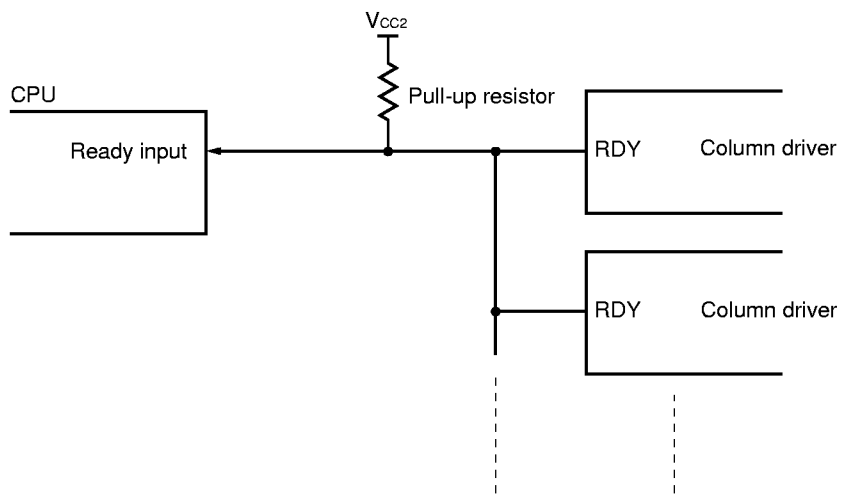
★ **(1) Timing**



(2) Connection of the RDY pin

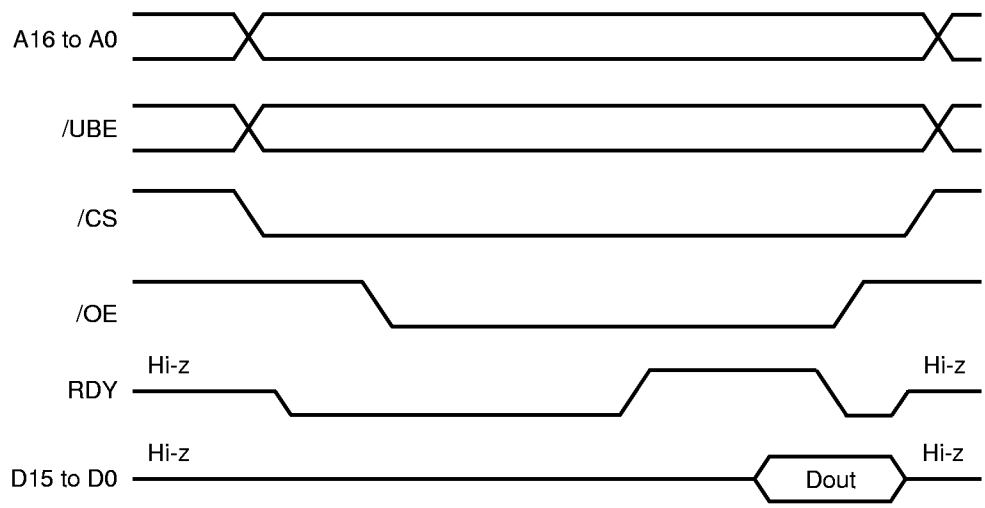
The RDY pin uses a 3-state buffer. Externally attach a pull-up resistor to the RDY pin.

When more than one μPD16661A is used, wired-OR connect each LSI RDY pin.

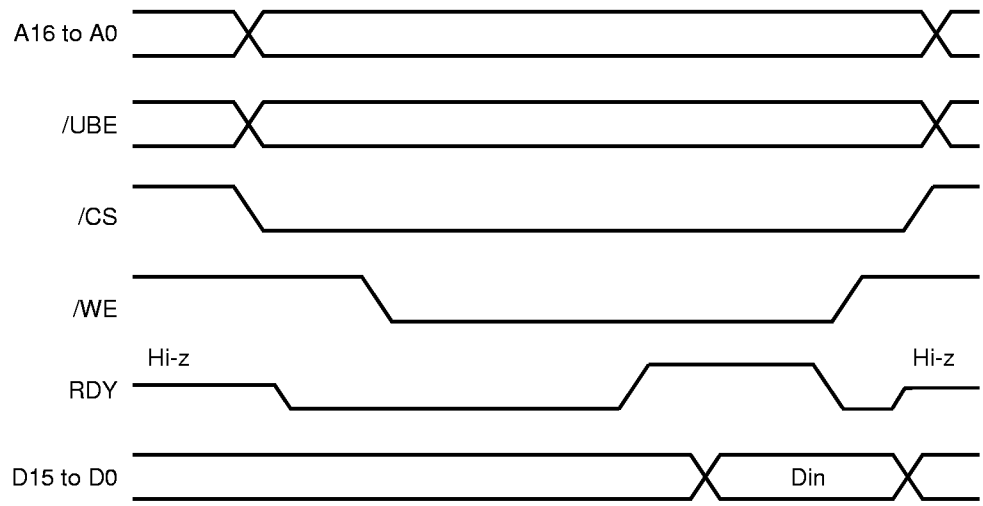


★ **7.2 Access timing**

(1) Display data read timing



(2) Display data write timing

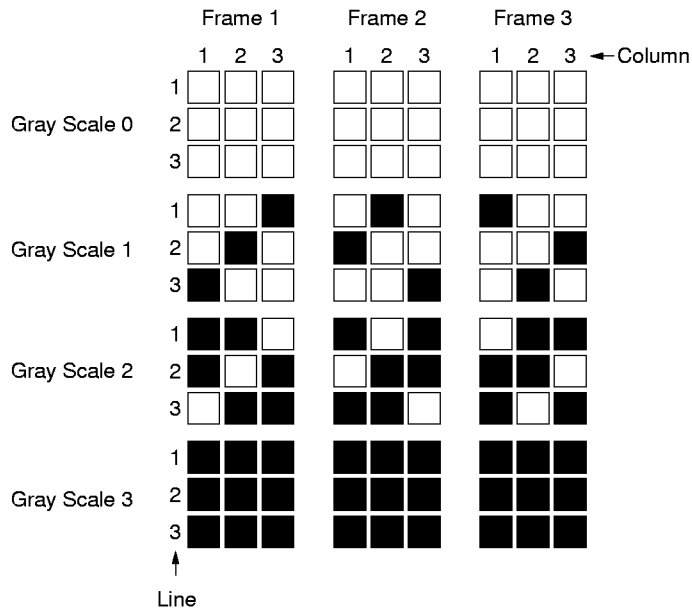


8. GRAY SCALE CONTROL

The four gray scales are expressed in terms of 3 thinning-out frames.

The thinning-out method is changed by 9 pixels: pixel numbers 1, 2, and 3, and line numbers 1, 2, and 3 of the liquid-crystal panel.

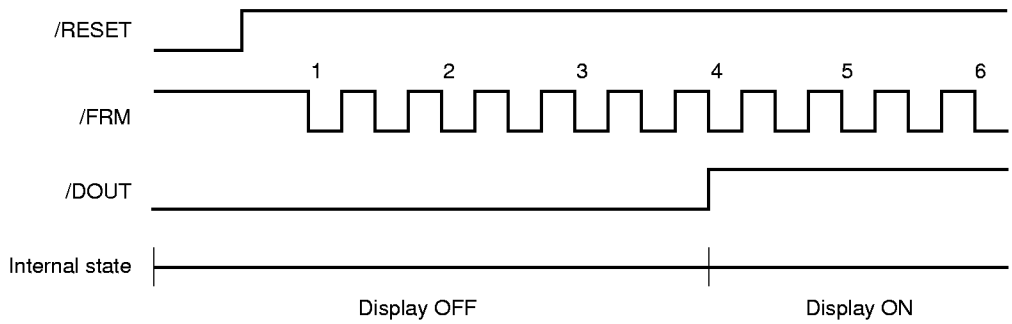
Frame thinning-out method



9. LIQUID-CRYSTAL TIMING GENERATION

9.1 Reset state

In the reset state, the internal counter is zero-cleared.
After the reset is released, the display OFF function operates during the 4-frame cycle, even if the /DOFF pin is at H.

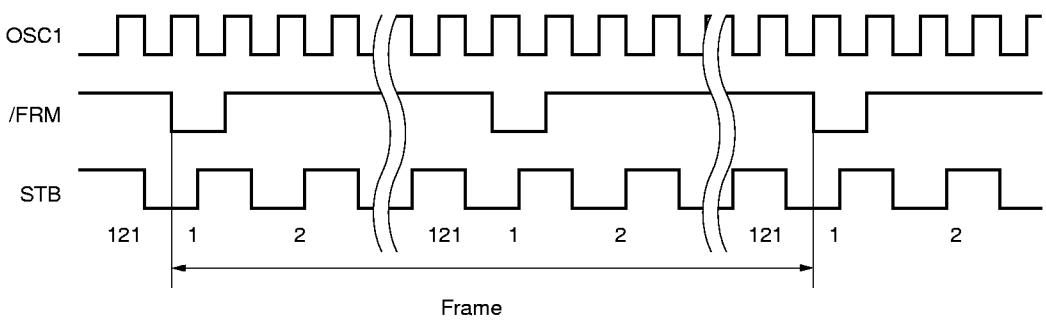


9.2 Liquid-crystal timing generation circuit

When the master mode is set with MS = H, this circuit generates the signals /FRM and STB at a duty ratio timing of 1/240. It also generates L1 and L2, which are the drive voltage selection signals for the row driver.

The /FRM signal is generated twice per frame. The STB signal is generated 121 times per half frame, or 242 times per frame.

Generation of /FRM & STB signals



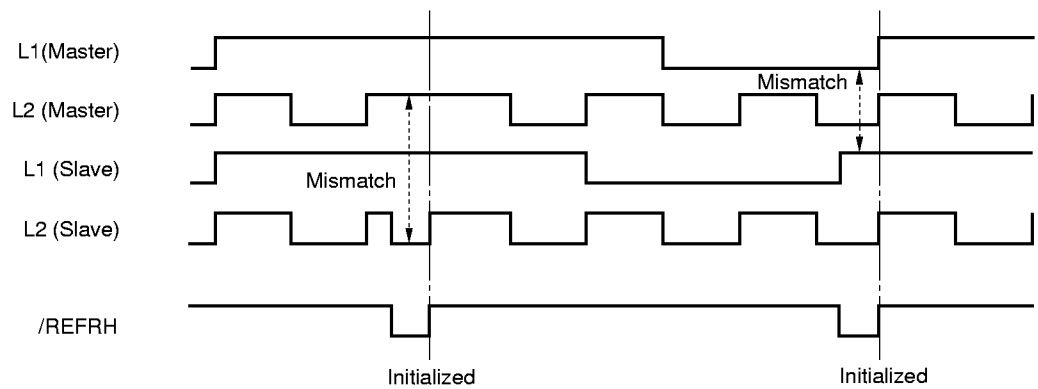
Generation of L1 and L2 signals

STB	1 2 3 4 ···	1 2 3 4 ···	1 2 3 4 ···	1 2 3 4 ···
L1	1 1 1 1 ···	1 1 1 1 ···	0 0 0 0 ···	0 0 0 0 ···
L2	1 0 1 0 ···	0 1 0 1 ···	0 1 0 1 ···	1 0 1 0 ···

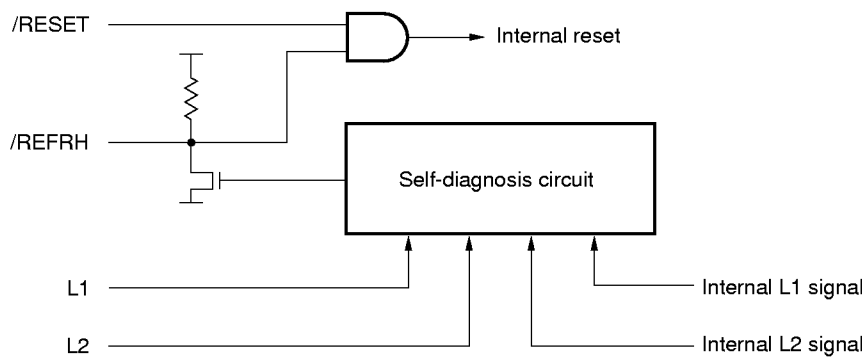
10. SELF-DIAGNOSIS FUNCTION

This is a function to check whether or not there has been a delay in the operation timing of each column driver caused by external noise, etc. The slave chip compares the L1 and L2 signals of the master chip with the L1 and L2 signals generated internally, and if a mismatch is discovered, the slave chip sends a refresh signal to all the column drivers. When the refresh signal is received, the internal reset is activated, and the timing is initialized. At this time, the display turns OFF while /REFRH = L and during the four frame cycle.

The L1 and L2 signals are checked for mismatch at the rising edge of /FRM once every half frame.



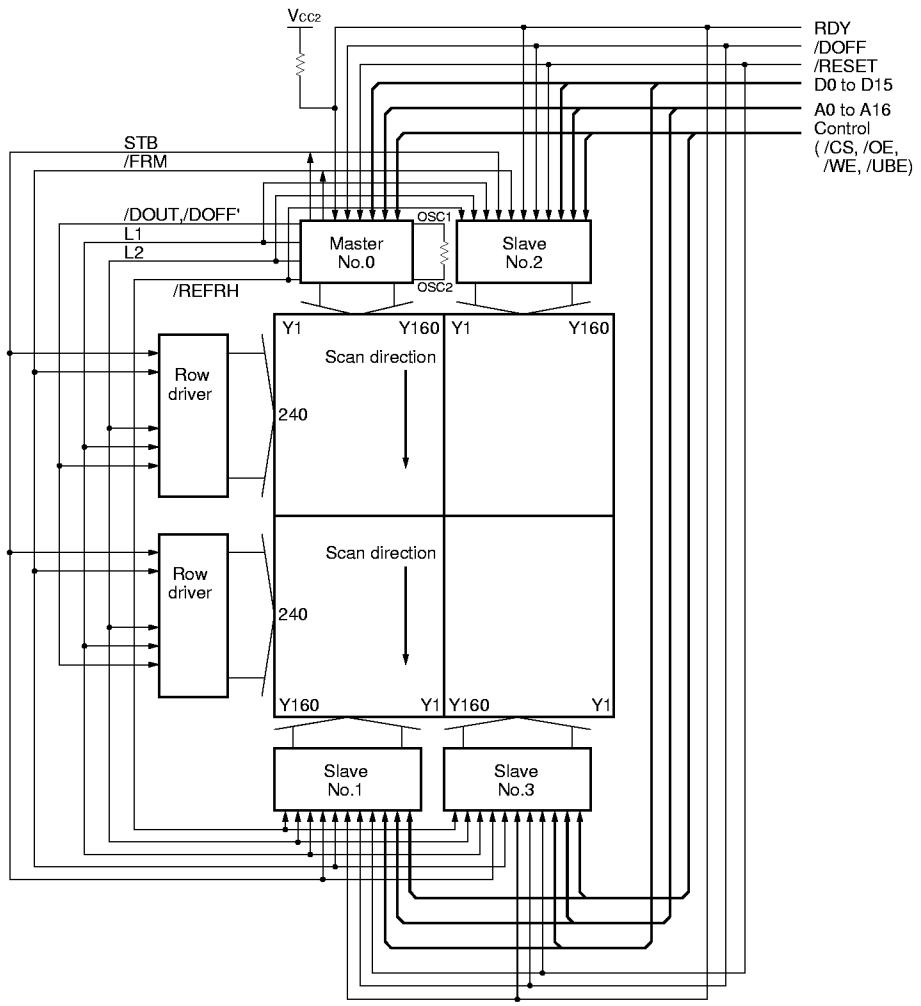
Block configuration diagram (Slave side)



11. SYSTEM CONFIGURATION EXAMPLE

This is an example of the configuration of a liquid-crystal panel of half VGA size (480 × 320, perpendicular) using four μPD16661A devices and two row drivers.

- Each column driver sets the LSI No. with the PL0, PL1, and PL2 pins.
- The DIR pin of each column driver is set to low.
- One of the column drivers only is set to master; all the others are set to slave. Signals are supplied from the master column driver to the slave column drivers and the row drivers.
- The OSC1 and OSC2 pins have an oscillator resistor attached on the master, and are left open on the slaves.
- All the signals from the system side (D0 to D15, A0 to A16, /CS, /OE, /WE, /UBE, RDY, /RESET, /DOFF) are connected in parallel to the column driver. A pull-up resistor is attached to the RDY signal.
- The TEST pin is used to test the LSI, and is left open or connected to the GND when the system is configured.



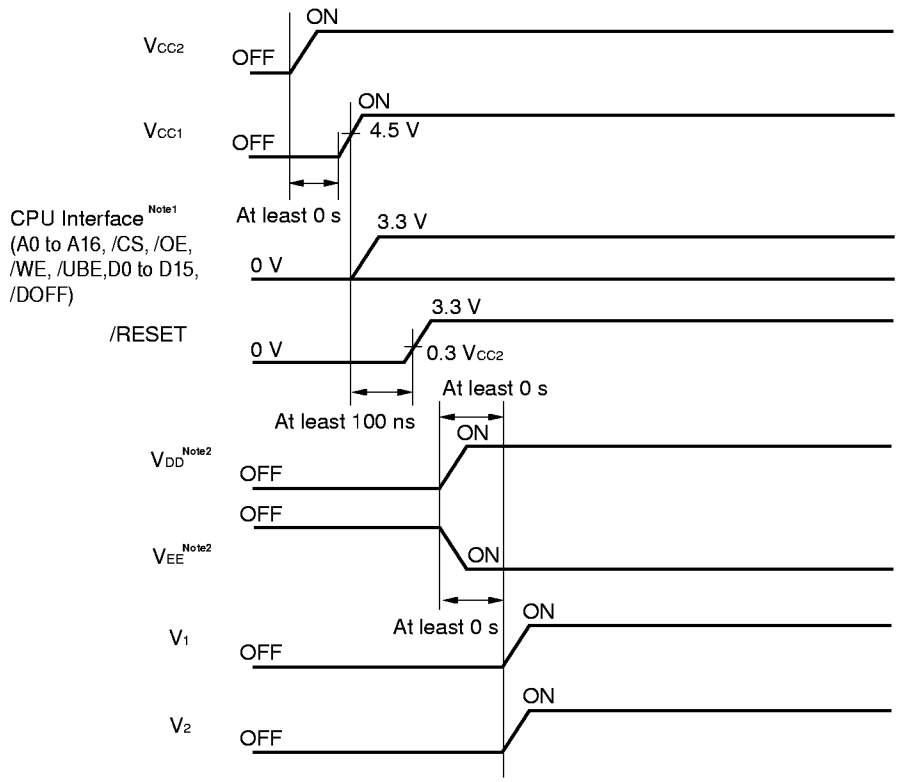
Remark /DOFF' is an input pin of row driver.

★ 12. CHIP SET POWER SUPPLY INPUT SEQUENCE

It is recommended that the power supply be input in the following way.

V_{CC2} → V_{CC1} → input → V_{DD}, V_{EE} → V_1, V_2

Make sure that the LCD drive voltages are input last.



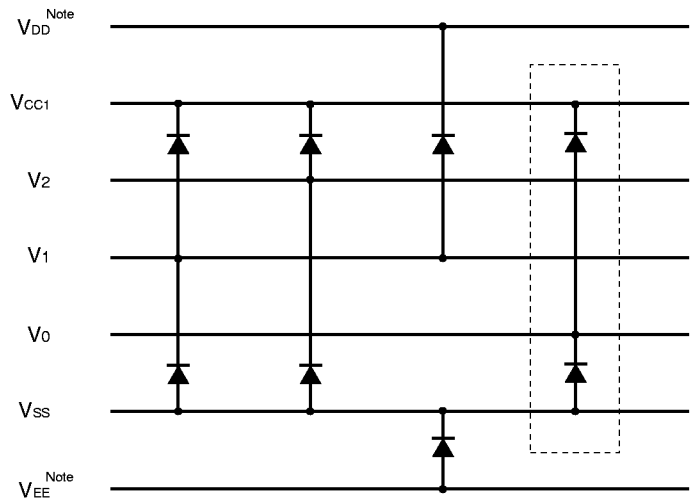
Notes 1. Inputting the selection pins (PL0, PL1, PL2, DIR, MS, BMODE) at the same time as the V_{CC2} pin is unproblematic.

2. It is not necessary to turn ON V_{DD} and V_{EE} at the same time.

V_{DD} and V_{EE} are the liquid-crystal power supplies of the row driver.

Caution Disconnection of the chip set power supply is done in the reverse order of the input sequence.

13. EXAMPLE OF THE CONFIGURATION OF THE MODULE – INTERNAL SCHOTTKY BARRIER DIODE FOR POWER SUPPLY PROTECTION REINFORCEMENT



Configure the diodes that are enclosed in the dotted lines when V0 is not 0 V (GND).

★ **Note** V_{DD} and V_{EE} are the liquid-crystal power supplies of the row driver.

Remark Use the Schottky Barrier Diode at V_f = 0.5 V or less.

14. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage (1)	V_{CC1}	–0.5 to +6.5	V	**Note1**
Supply voltage (2)	V_{CC2}	–0.5 to +4.5	V	**Note2**
Input /Output voltage (1)	$V_{I/O1}$	–0.5 to V_{CC1} + 0.5	V	**Note1**
Input /Output voltage (2)	$V_{I/O2}$	–0.5 to V_{CC2} + 0.5	V	**Note2**
Input/ Output voltage (3)	$V_{I/O3}$	–0.5 to V_{CC1} + 0.5	V	**Note3, Note4**
Operating ambient temperature	T_A	–20 to +70	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes1. 5-V signals (/FRM, STB, /DOUT, L1, L2)

2. 3.3-V signals (MS, DIR, PL0 to PL2, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 to D15, /RESET, OSC1, OSC2, /DOFF, TEST, GMODE, BMODE, /REFRH)

3. Liquid-crystal drive power supplies (V_0, V_1, V_2, Y1 to Y160)

4. Set $V_0 < V_1 < V_2$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended operating range (T_A = –20 to +70 °C, V_0 = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply voltage (1)	V_{CC1}	4.5	5.0	5.5	V	
Supply voltage (2)	V_{CC2}	3.0	3.3	3.6	V	
Input voltage (1)	V_{I1}	0		V_{CC1}	V	**Note1**
Input voltage (2)	V_{I2}	0		V_{CC2}	V	**Note2**
V_1 input voltage	V_1	V_0		V_2	V	
V_2 input voltage	V_2	V_1		V_{CC1}	V	
OSC external resistor	R_{OSC}	300		700	kΩ	

Notes1. 5-V signals (/FRM, STB)

2. 3.3-V signals (MS, DIR, PL0 to PL2, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 toD15, /RESET, OSC1, OSC2, /DOFF, TEST, GMODE, BMODE, /REFRH)

DC Characteristics

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
High-level input voltage (1) V_{CC1}	V_{IH1}	0.7 V_{CC1}			V	**Note1**
Low-level input voltage (1) V_{CC1}	V_{IL1}			0.3 V_{CC1}	V	**Note1**
High-level input voltage (2) V_{CC2}	V_{IH2}	0.7 V_{CC2}			V	**Note2**
Low-level input voltage (2) V_{CC2}	V_{IL2}			0.3 V_{CC2}	V	**Note2**
High-level input voltage (2) V_{CC2}	V_{IH3}	0.8 V_{CC2}			V	**Note4**
Low-level input voltage (2) V_{CC2}	V_{IL3}			0.2 V_{CC2}	V	**Note4**
High-level output voltage (1) V_{CC1}	V_{OH1}	V_{CC1} – 0.4			V	I_{OH} = –1 mA, **Note3**
Low-level output voltage (1) V_{CC1}	V_{OL1}			0.4	V	I_{OL} = 2 mA, **Note3**
High-level output voltage (2) V_{CC1}	V_{OH2}	V_{CC1} – 0.4			V	I_{OH} = –2 mA, **Note1**
Low-level output voltage (2) V_{CC1}	V_{OL2}			0.4	V	I_{OL} = 4 mA, **Note1**
High-level output voltage (3) V_{CC2}	V_{OH3}	V_{CC2} – 0.4			V	I_{OH} = –1 mA, **Note4**
Low-level output voltage (3) V_{CC2}	V_{OL3}			0.4	V	I_{OL} = 2 mA, **Note4**
Input leakage current (1)	I_{I1}			±10	μA	Other than TEST pin, V_I = V_{CC2} or GND
Input leakage current (2)	I_{I2}	10	40	100	μA	Pull-down (TEST pin), V_I = V_{CC2}
Current consumption for display operation (1)	I_{MAS1}			40	μA	Master, V_{CC1}, **Note5**
Current consumption for display operation (2)	I_{MAS2}			150	μA	Master, V_{CC2}, **Note5**
Current consumption for display operation (3)	I_{SLV1}			30	μA	Slave, V_{CC1}, **Note5**
Current consumption for display operation (4)	I_{SLV2}			100	μA	Slave, V_{CC2}, **Note5**
Liquid-crystal driving output ON resistance	R_{ON}		1	2	kΩ	**Note6**

Notes 1. 5-V signals (/FRM, STB,L1,L2)

2. 3.3-V signals (MS, DIR, PL0 to PL2, A0 to A16, /CS, /OE, /WE, /UBE, RDY, D0 to D15, /RESET, /DOFF, TEST, GMODE, BMODE)

3. /DOUT pin

4. D0 to D15, RDY, and OSC2 pins

5. When the frame frequency is 70 Hz, and the output and CPU are without load and access respectively. (D0 to D15, A0 to A16, and /UBE = GND, and /CS, /OE, and /WE = V_{CC2})

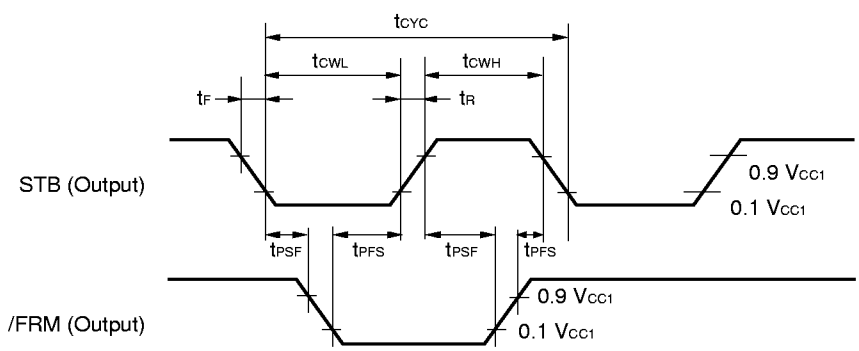
6. This is the resistance value between a Y pin and a V pin (V_0, V_1, or V_2) when the load current (I_{ON} = 100 μA) is passed to a pin of Y1 to Y160.

AC Characteristics 1 Display data transfer timing

Master mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C, Frame frequency : 70 Hz (f_{OSC} = 33.88 kHz), Output load : 100 pF)

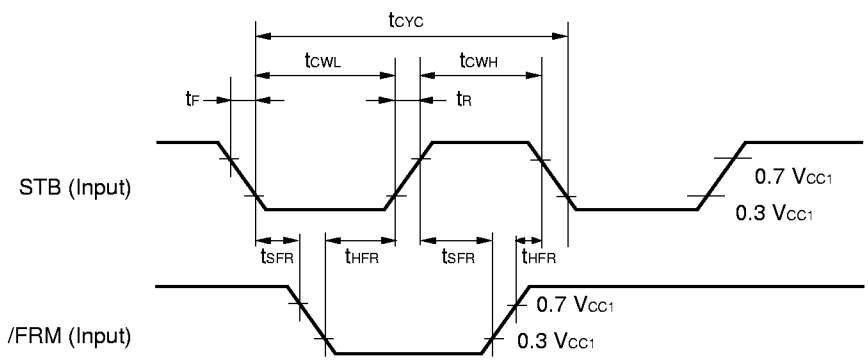
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
STB Clock cycle time	t_{CYC}	58	2/f_{OSC}		μs	
STB High-level width	t_{CWH}	28	1/f_{OSC}		μs	
STB Low-level width	t_{CWL}	28	1/f_{OSC}		μs	
STB Rise time	t_R			100	ns	
STB Fall time	t_F			100	ns	
STB - /FRM Delay time	t_{PSF}	12			μs	
/FRM - STB Delay time	t_{PFS}	12			μs	



Slave mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C)

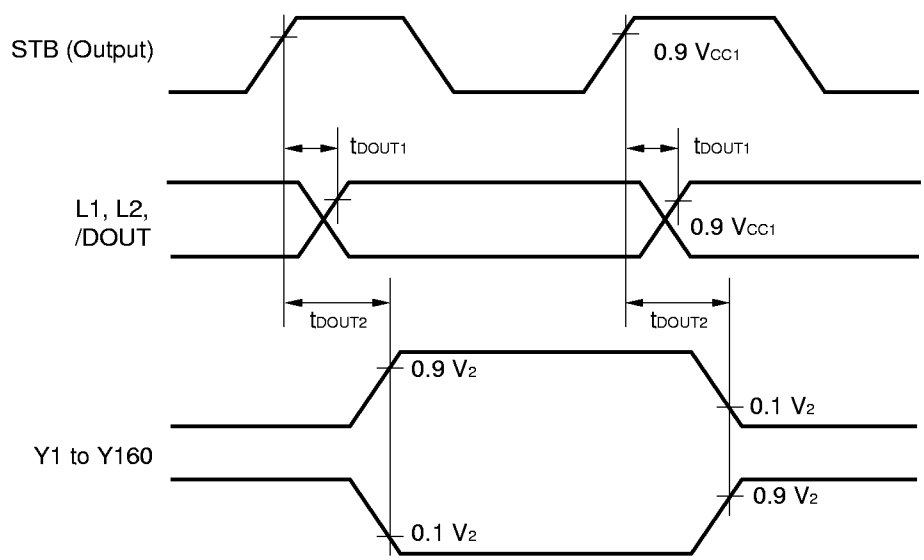
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
STB Clock cycle time	t_{CYC}	10			μs	
STB High-level width	t_{CWH}	4			μs	
STB Low-level width	t_{CWL}	4			μs	
STB Rise time	t_R			150	ns	
STB Fall time	t_F			150	ns	
/FRM Setup time	t_{SFR}	1			μs	
/FRM Hold time	t_{HFR}	1			μs	



Master/Slave common items

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Output delay time (L1, L2, /DOUT)	t_{DOUT1}		50	100	ns	Output without load
Output delay time (Y1 to Y160)	t_{DOUT2}		90	150	ns	Output without load

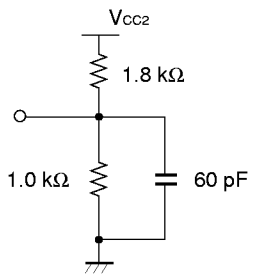


AC Characteristics 2 Graphic access timing

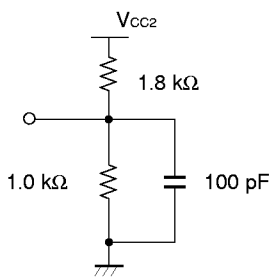
(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C, t_r = t_f = 5 ns, frame frequency : 70 Hz (f_{OSC} = 33.88 kHz))

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
/OE,/WE Recovery time	t_{RY}	30			ns	
Address setup time	t_{AS}	10			ns	
Address hold time	t_{AH}	20			ns	
RDY Output delay time	t_{RYR}			30	ns	C_L = 15 pF
★ RDY Float time	t_{RYZ}			30	ns	**Note3**
★ Wait state time	t_{RYW}			35	ns	**Note1**
Ready state time (Without Contention)	t_{RYF1}		60	100	ns	**Note1**
Ready state time (With Contention)	t_{RYF2}		650	1200	ns	**Note1**
Data access time (Read cycle)	t_{ACS}			100	ns	**Note2**
Data float time (Read cycle)	t_{HZ}			40	ns	**Note3**
/CS-/OE Time (Read cycle)	t_{CSOE}	10			ns	
/OE-/CS Time (Read cycle)	t_{OECS}	20			ns	
Write pulse width (Write cycle)	t_{WP}	50			ns	**Note1**
Data setup time (Write cycle)	t_{DW}	20			ns	
Data hold time (Write cycle)	t_{DH}	20			ns	
/CS-/WE Time (Write cycle)	t_{CSWE}	10			ns	
/WE-/CS Time (Write cycle)	t_{WECS}	20			ns	
Reset pulse width	t_{WRES}	100			ns	
RDY-/OE Time	t_{RDOE}			**Note4**	—	
RDY-/WE Time	t_{RDWE}			**Note4**	—	

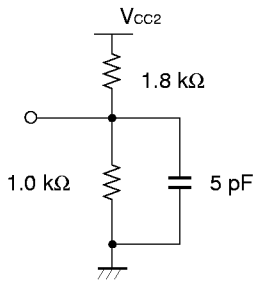
Notes 1. Load circuit



2. Load circuit

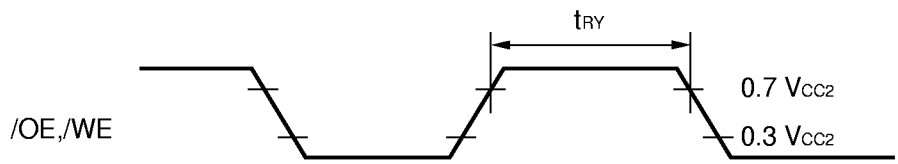


★ **3.** Load circuit

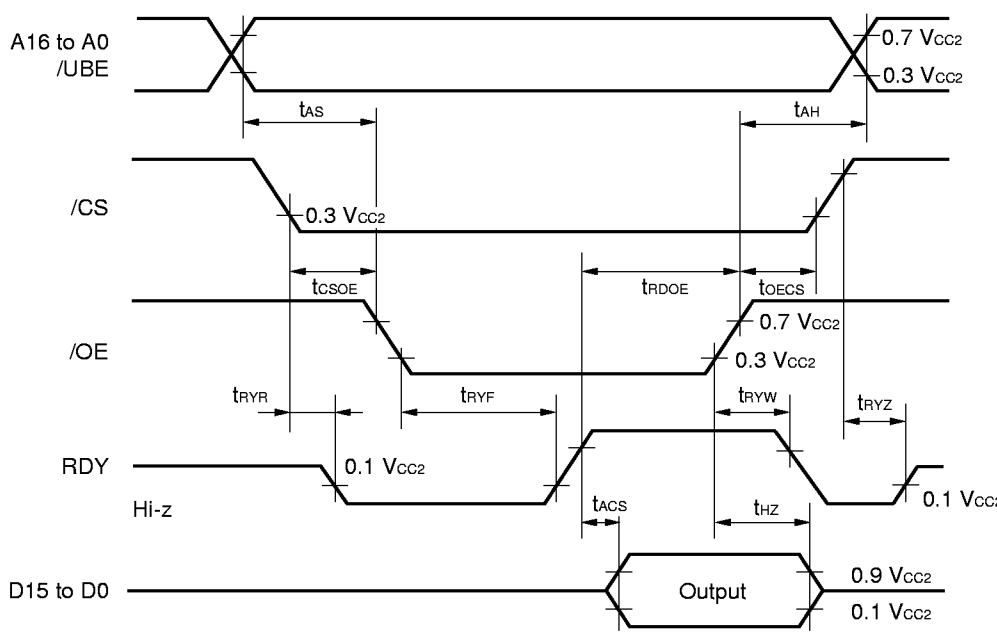


4. The display may be affected if there is a long time from the rise of RDY to the /OE or /WE signals. It is recommended that t_{RDOE} and t_{RDWE} are 1000 ns or less.

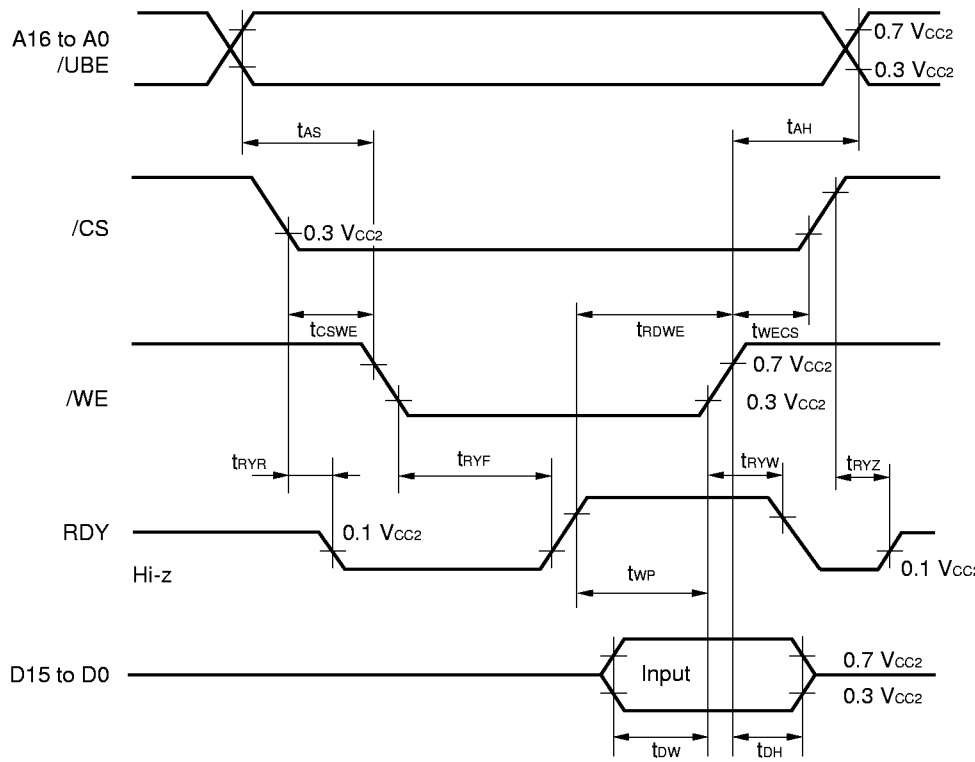
/OE,/WE Recovery time



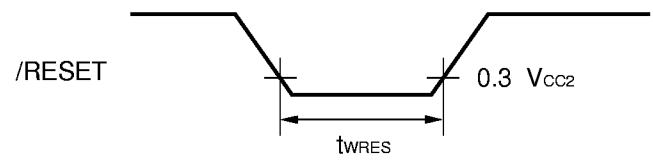
★ **Read cycle**



★ **Write cycle**



★ **Reset pulse width**



AC Characteristics 3 CR Oscillator

(V_{CC2} = 3.0 to 3.6 V, T_A = –20 to +70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Oscillation Frequency	fosc	32	36	40	kHz	External resistor 350 kΩ
Frame Frequency	—	66.1	74.4	82.6	Hz	External resistor 350 kΩ

15. RELATIONSHIP BETWEEN THE OSCILLATION , FRAME , AND STB FREQUENCIES

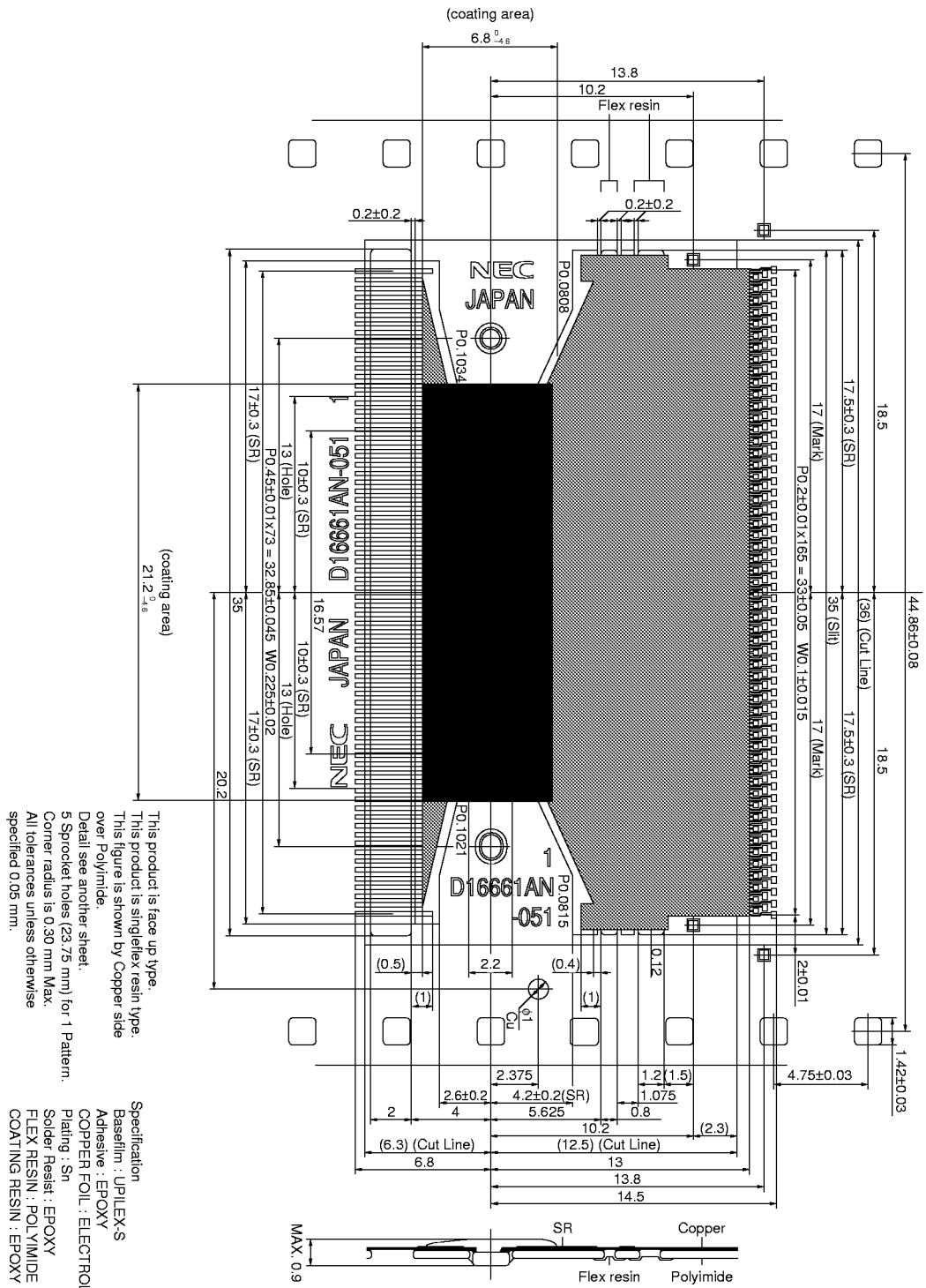
This relationship is as follows:

$$\text{Frame frequency} = \frac{1}{242 \times 2} \times \text{Oscillation frequency}$$

$$\text{STB frequency} = \frac{1}{2} \times \text{Oscillation frequency}$$

★ 16. PACKAGE DRAWING

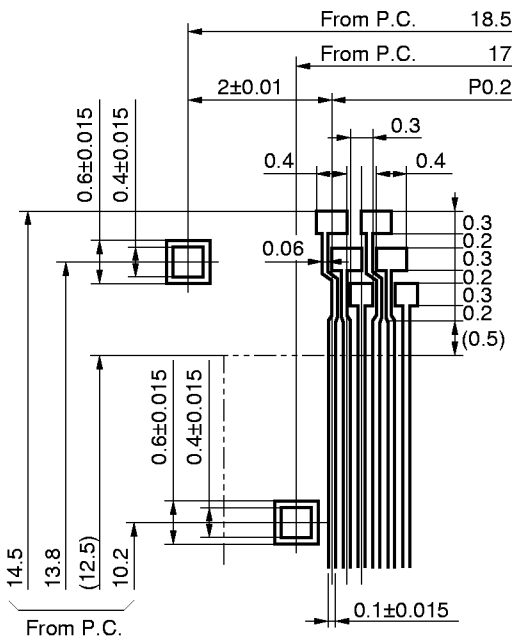
Standard TCP package drawing (μPD16661AN-051)



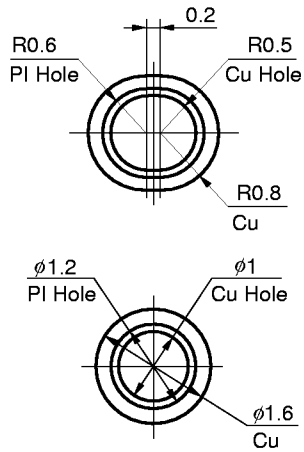
This product is face up type.
This product is singleflex resin type.
This figure is shown by Copper side over Polyimide.
Detail see another sheet.
5 Sprocket holes (23.75 mm) for 1 Pattern.
Corner radius is 0.30 mm Max.
All tolerances unless otherwise specified 0.05 mm.

Specification	
Baseflm : UPILEX-S	75 μm
Adhesive : EPOXY	12 μm
COPPER FOIL : ELECTROLYSIS Cu	25 μm
Plating : Sn	MIN. 0.25 μm
Solder Resist : EPOXY	25 μm
FLEX RESIN : POLYIMIDE	
COATING RESIN : EPOXY	

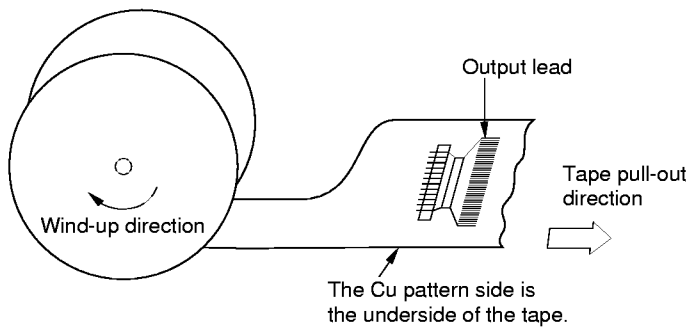
Test pad and alignment mark details (x20)



Alignment hole details (x20)

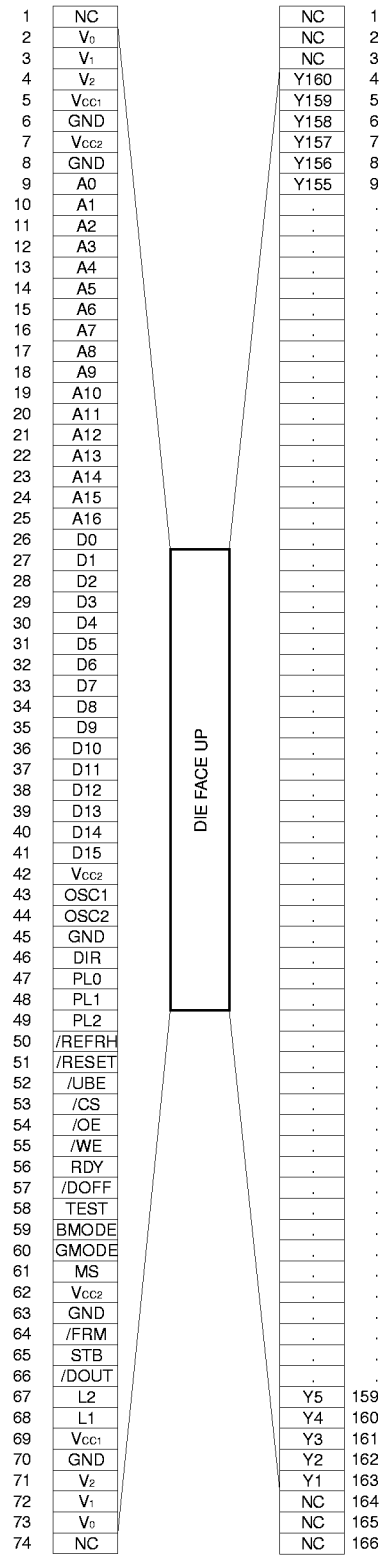


TCP tape winding direction



Standard TCP package drawing (μPD16661AN-051)

Pin connection diagram



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.