PRELIMINARY

1/4 DUTY LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6433B is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6433B is useful for the digital tuning system or others segment type display driver.

■ PACKAGE OUTLINE

NJU6433BFG1

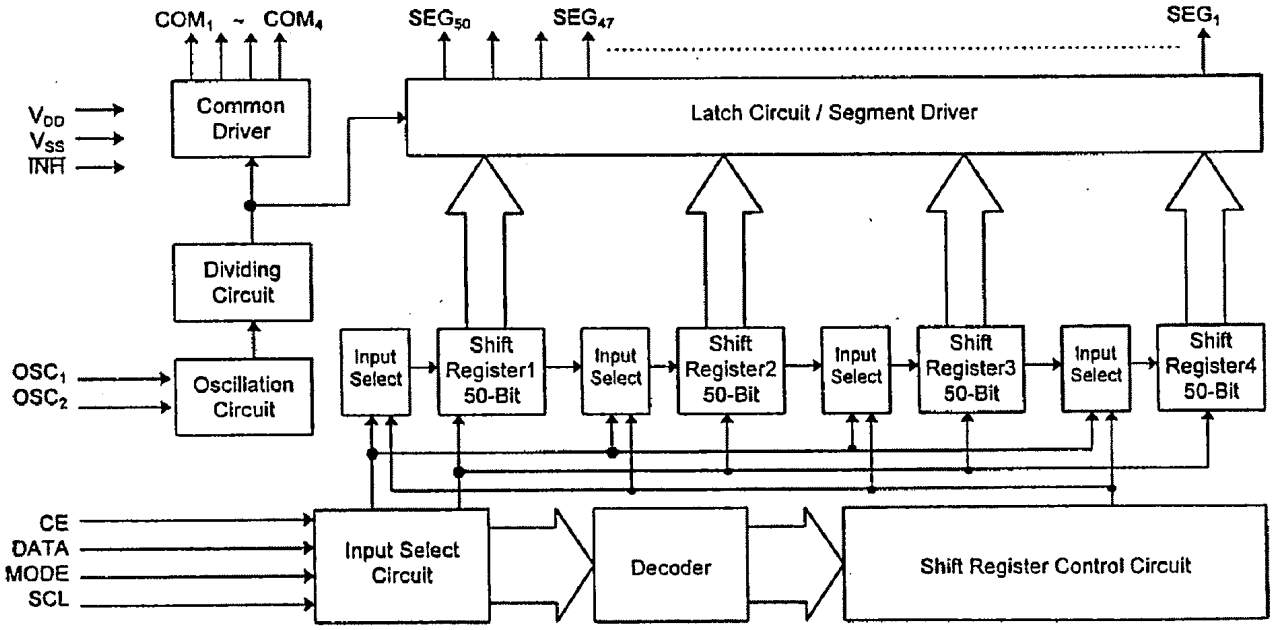
NJU6433BFH1

NJU6433BC/BCH

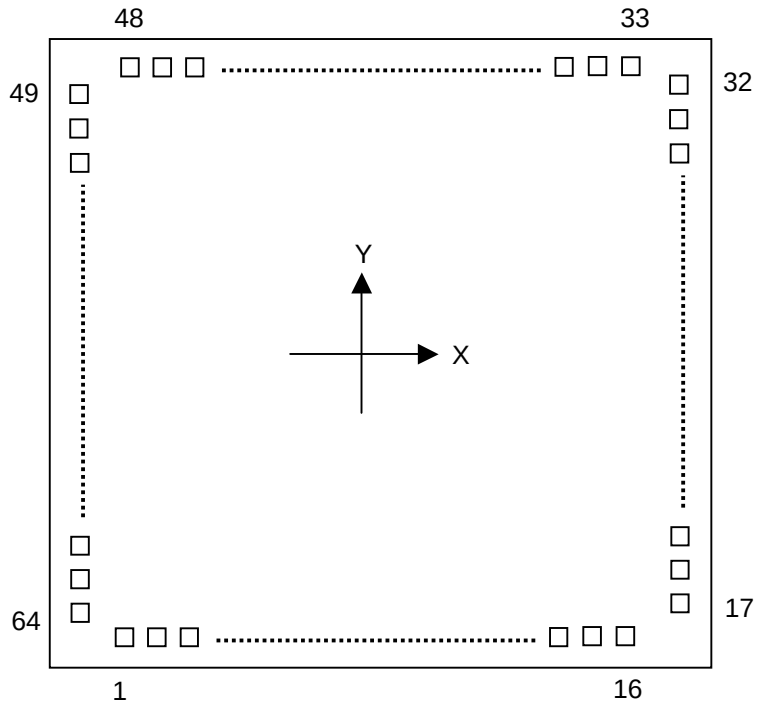
■ FEATURES

- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required)
- Display Off Function (INHb Terminal)
- Operating Voltage 2.4 to 5.5V
- LCD Driving Voltage 6.5V Max.
- Package Outline Bump Chip, Chip, QFP 64-G1, QFP64-H1
- C-MOS Technology

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center : X=0μm, Y=0μm
Chip Size : X=3.20 mm, Y=3.20 mm
Chip Thickness : 400 μm
PAD Size : X=99.2 μm, Y=99.2 μm
PAD Pitch : 171.2 μm
Bump Height : 25 μm

■ PAD COORDINATES

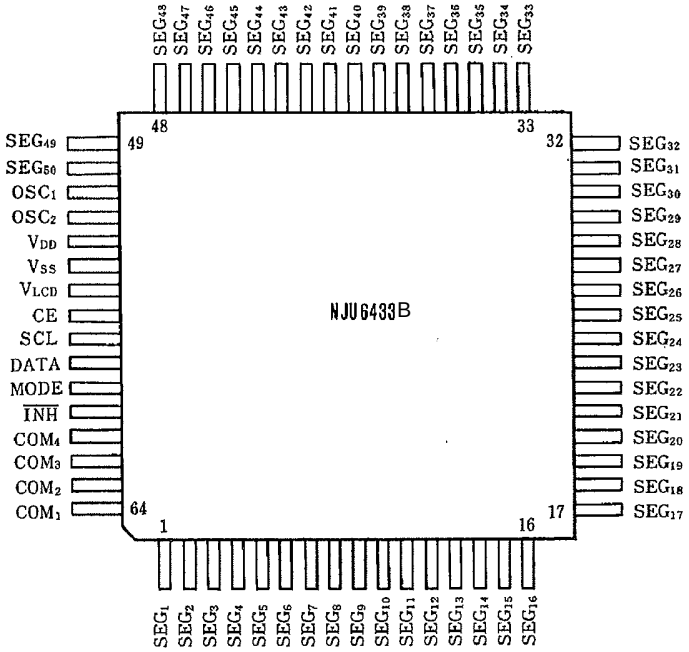
Chip Size 3.20 x 3.20 mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X= μm	Y= μm
1	SEG_1	-1279	-1437
2	SEG_2	-1107	-1437
3	SEG_3	-936	-1437
4	SEG_4	-765	-1437
5	SEG_5	-594	-1437
6	SEG_6	-423	-1437
7	SEG_7	-251	-1437
8	SEG_8	-80	-1437
9	SEG_9	91	-1437
10	SEG_{10}	262	-1437
11	SEG_{11}	433	-1437
12	SEG_{12}	605	-1437
13	SEG_{13}	776	-1437
14	SEG_{14}	947	-1437
15	SEG_{15}	1118	-1437
16	SEG_{16}	1289	-1437
17	SEG_{17}	1437	-1288
18	SEG_{18}	1437	-1117
19	SEG_{19}	1437	-946
20	SEG_{20}	1437	-775
21	SEG_{21}	1437	-603
22	SEG_{22}	1437	-432
23	SEG_{23}	1437	-261
24	SEG_{24}	1437	-90

PAD No.	Terminal	X= μm	Y= μm
25	SEG_{25}	1437	81
26	SEG_{26}	1437	253
27	SEG_{27}	1437	424
28	SEG_{28}	1437	595
29	SEG_{29}	1437	766
30	SEG_{30}	1437	937
31	SEG_{31}	1437	1109
32	SEG_{32}	1437	1280
33	SEG_{33}	1280	1437
34	SEG_{34}	1109	1437
35	SEG_{35}	937	1437
36	SEG_{36}	766	1437
37	SEG_{37}	595	1437
38	SEG_{38}	424	1437
39	SEG_{39}	253	1437
40	SEG_{40}	81	1437
41	SEG_{41}	-90	1437
42	SEG_{42}	-261	1437
43	SEG_{43}	-432	1437
44	SEG_{44}	-603	1437
45	SEG_{45}	-775	1437
46	SEG_{46}	-946	1437
47	SEG_{47}	-1117	1437
48	SEG_{48}	-1288	1437

PAD No.	Terminal	X= μm	Y= μm
49	SEG_{49}	-1437	1280
50	SEG_{50}	-1437	1109
51	OSC_1	-1437	937
52	OSC_2	-1437	766
53	V_{DD}	-1437	595
54	V_{SS}	-1437	424
55	V_{LCD}	-1437	253
56	CE	-1437	81
57	SCL	-1437	-90
58	DATA	-1437	-261
59	MODE	-1437	-432
60	INHX	-1437	-603
61	COM_4	-1437	-775
62	COM_3	-1437	-946
63	COM_2	-1437	-1117
64	COM_1	-1437	-1288

■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
1~50	SEG_1~SEG_{50}	LCD Segment Output Terminals
51 52	OSC_1 OSC_2	Oscillation Terminals : External resistance is connected to these terminals.
53	V_{DD}	Power Supply (+5V)
54	V_{SS}	Power Supply (0V)
55	V_{LCD}	Power Supply for LCD Driving The relation : $1.3V_{DD} \geq \lvert V_{DD} - V_{LCD} \rvert$, $V_{SS} \geq V_{LCD}$ must be maintained.
56	CE	Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch
57	SCL	Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge.
58	DATA	Serial Data Input Terminal Data input timing : SCL clock rise edge
59	MODE	Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (Refer the mode setting table for mode setting contents)
60	INHb	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off
61~64	COM_4~COM_1	LCD Common Output Terminals

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

The oscillation circuit operate by connecting external resistance (capacitance is incorporated). This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(2) Data Input Format

(2-1) Input Data Correspond to Segment Status

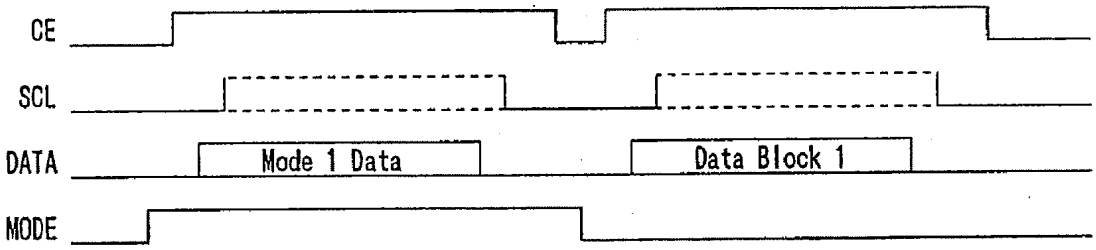
The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data Dxxx	Segment Status
”H”	ON
”L”	OFF

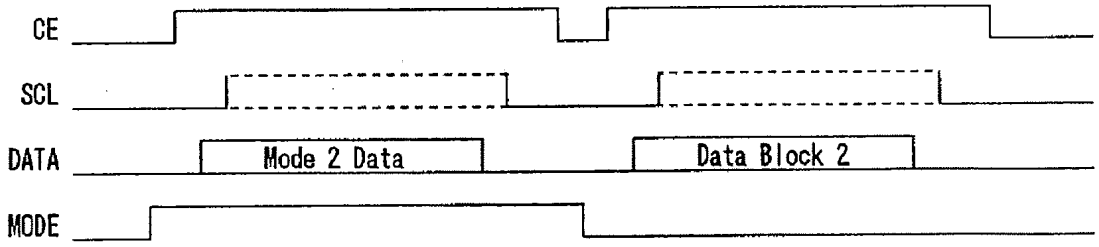
(2-2) Write to Shift-register

Write to shift-register performes Mode setting data writing and LCD display data writing.

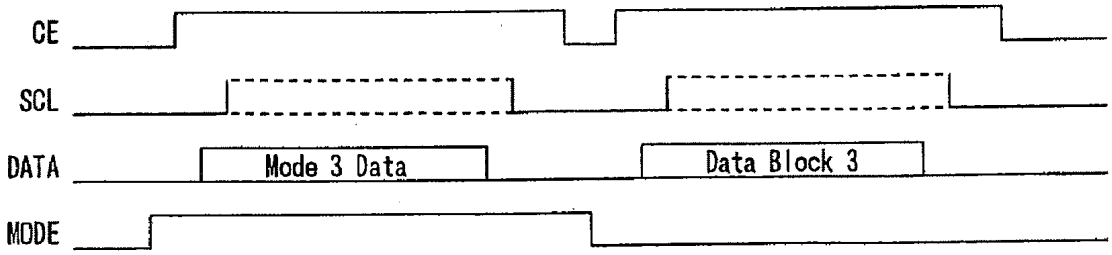
Example 1(Mode 1): Write to Shift-register 1(1 to 50-bit)



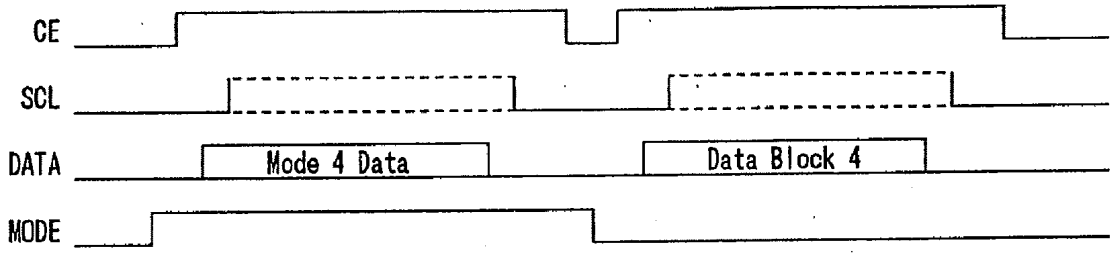
Example 2(Mode 2): Write to Shift-register 2(51 to 100-bit)



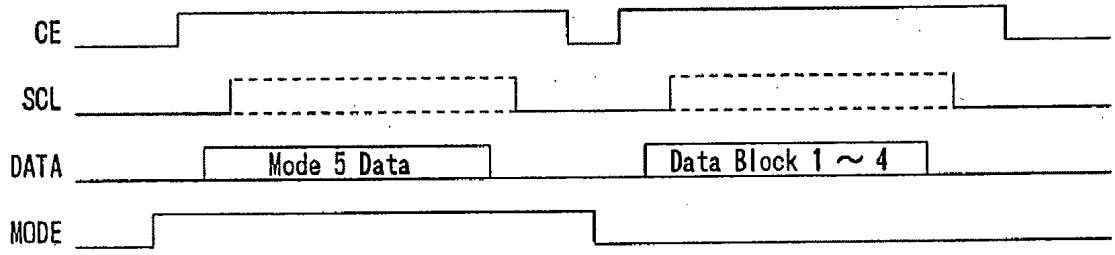
Example 3(Mode 3): Write to Shift-register 3(101 to 150-bit)



Example 4(Mode 4): Write to Shift-register 4(151 to 200-bit)



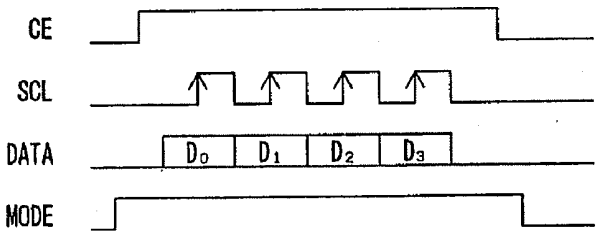
Example 5(Mode 5): Write to Shift-register 5(1 to 200-bit)



(2-3) Mode Setting

Transferd register selection and all clear of the shift register are performed by writing 4-bit code shown below to the decoder in CE ="H" and MODE ="H" state.

<Input Timing Chart>



<Mode Setting Table>

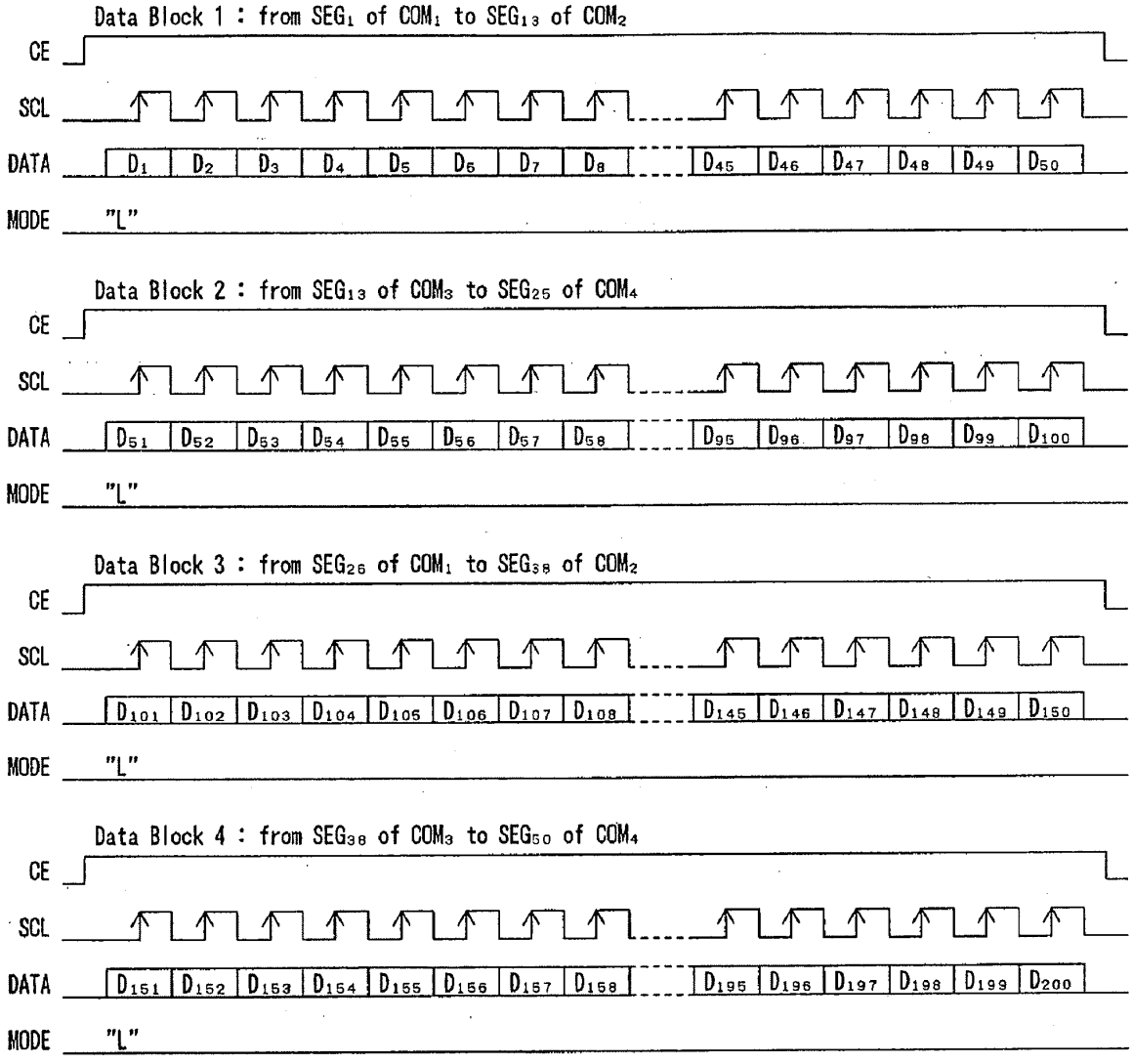
CE Terminal	MODE Terminal	DATA Terminal MODE # Data D_3 D_2 D_1 D_0 (HEX)	Mode Set Up
"H"	"H"	0 0 0 1 (01_H)	Select the shift-register 1
		0 0 1 0 (02_H)	Select the shift-register 2
		0 0 1 1 (03_H)	Select the shift-register 3
		0 1 0 0 (04_H)	Select the shift-register 4
		0 1 0 1 (05_H)	Select the all shift-register (1 to 4)
		1 1 1 1 ($0F_H$)	All shift-register is "L"

Note) The internal decoder is data through type. Therefore, the 8 bits data also can write though only 4 bits data from the CE falling are validated.

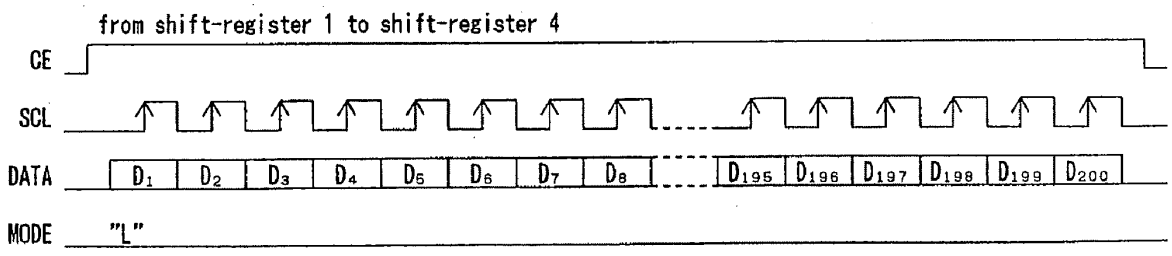
(2-4) Block Data and Whole Data transfer

a. Block Data (50-bit) transfer

In this mode, each 50 bits data block send to the each register.



b. Whole Data (200-bit) transfer



(2-5) Display Data Correspond to Segment and Common Terminals

Mode	Data	Segment	COM_1	COM_2	COM_3	COM_4	Data Block
Mode 1	D_1 D_2 D_3 D_4	SEG_1	○	○	○	○	Data Block 1
	D_5 D_6 D_7 D_8	SEG_2	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{45} D_{46} D_{47} D_{48}	SEG_{12}	○	○	○	○	
	D_{49} D_{50}	SEG_{13}	○	○			
Mode 2	D_{51} D_{52}	SEG_{13}			○	○	Data Block 2
	D_{53} D_{54} D_{55} D_{56}	SEG_{14}	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{97} D_{98} D_{99} D_{100}	SEG_{25}	○	○	○	○	
Mode 3	D_{101} D_{102} D_{103} D_{104}	SEG_{26}	○	○	○	○	Data Block 3
	D_{105} D_{106} D_{107} D_{108}	SEG_{27}	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{145} D_{146} D_{147} D_{148}	SEG_{37}	○	○	○	○	
	D_{149} D_{150}	SEG_{38}	○	○			
Mode 4	D_{151} D_{152}	SEG_{38}			○	○	Data Block 4
	D_{153} D_{154} D_{155} D_{156}	SEG_{39}	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D_{197} D_{198} D_{199} D_{200}	SEG_{50}	○	○	○	○	

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Operating Voltage (1)	V_{DD}	-0.3~+7.0	V	
Operating Voltage (2)	V_{LCD}	V_{DD}-6.5~V_{SS}	V	1
Input Voltage (1)	$V_{I(1)}$	-0.3~+7.0	V	2
Input Voltage (2)	$V_{I(2)}$	-0.3~V_{DD}+0.3	V	3
Output Voltage	V_O	-0.3~V_{DD}+0.3	V	3
Output Current (1)	$I_{O(1)}$	100	uA	4
Output Current (2)	$I_{O(2)}$	1.0	mA	5
Power Dissipation	P_D	300	mW	
Operating Temperature	T_{opr}	-30~+85	°C	
Storage Temperature	T_{stg}	-40~+125	°C	

Note 1) V_{DD} x 1.3 ≥ $|V_{DD}-V_{LCD}|$, $V_{SS} \geq V_{LCD}$
Note 2) CE, SCL, DATA, MODE, INHb Terminals
Note 3) OSC_1, OSC_2 Terminals
Note 4) SEG_1~SEG_{50} Terminals
Note 5) COM_1~COM_4 Terminals

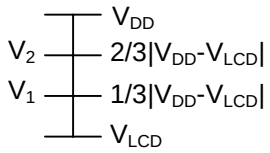
■ ELECTRICAL CHARACTERISTICS

- DC Characteristics

(Ta= 25°C, V_{DD}=5.0V, V_{SS}=0V, V_{LCD}=V_{DD}-6.5V)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	V_{DD}	V_{DD} Terminal		2.4	5.0	5.5	V	
Operating Voltage (2)	V_{LCD}	V_{LCD} Terminal		V_{SS}		V_{DD}-6.5	V	1
"H" Input Voltage	V_{IH}	CE, SCL, DATA, MODE, INHb		0.7V_{DD}		V_{DD}	V	
"L" Input Voltage	V_{IL}			V_{SS}		0.3V_{DD}	V	
"H" Input Current	V_{IH}	CE,SCL, DATA,MODE, INHb	V_I=V_{DD}			5	uA	
"L" Input Current	V_{IL}		V_I=V_{SS}			5	uA	
"H" Output Voltage (1)	$V_{OH(1)}$	SEG_1~SEG_{50}	I_O=-10uA	V_{DD}-1.0			V	
"L" Output Voltage (1)	$V_{OL(1)}$		I_O=+10uA			V_{LCD}+1.0	V	
Middle Level Voltage 1/3(1)	$V_{MS1/3}$	SEG_1~SEG_{50}	I_O=±10uA	V_1-1.0	V_1	V_1+1.0	V	2
Middle Level Voltage 2/3(1)	$V_{MS2/3}$		I_O=±10uA	V_2-1.0	V_2	V_2+1.0	V	
"H" Output Voltage (2)	$V_{OH(2)}$	COM_1~COM_4	I_O=-100uA	V_{DD}-0.6			V	
"L" Output Voltage (2)	$V_{OL(2)}$		I_O=+100uA			V_{LCD}+0.6	V	
Middle Level Voltage 1/3(2)	$V_{MC1/3}$	COM_1~COM_4	I_O=±100uA	V_1-0.6	V_1	V_1+0.6	V	2
Middle Level Voltage 2/3(2)	$V_{MC2/3}$		I_O=±100uA	V_2-0.6	V_2	V_2+0.6	V	
Oscillating Frequency Range	f_{OSC}	OSC_1, OSC_2 Terminals		25		200	kHz	
Oscillating Frequency	f_{OSC}	OSC_1, OSC_2, R=140kΩ		115	130	145	kHz	
Operating Current (1)	I_{DD}	V_{DD} Terminal			50	80	uA	
Operating Current (2)	I_{LCD}	V_{LCD} Terminal			15	25	uA	
Hysteresis Voltage	V_H	CE, SCL, DATA, MODE, INHb		0.3			V	

Note 1) The relation : V_{DD} x 1.3 ≥ $|V_{DD}-V_{LCD}|$, $V_{SS} \geq V_{LCD}$ must be maintained.
Note 2) V_1=1/3$|V_{DD}-V_{LCD}|$, V_2=2/3$|V_{DD}-V_{LCD}|$

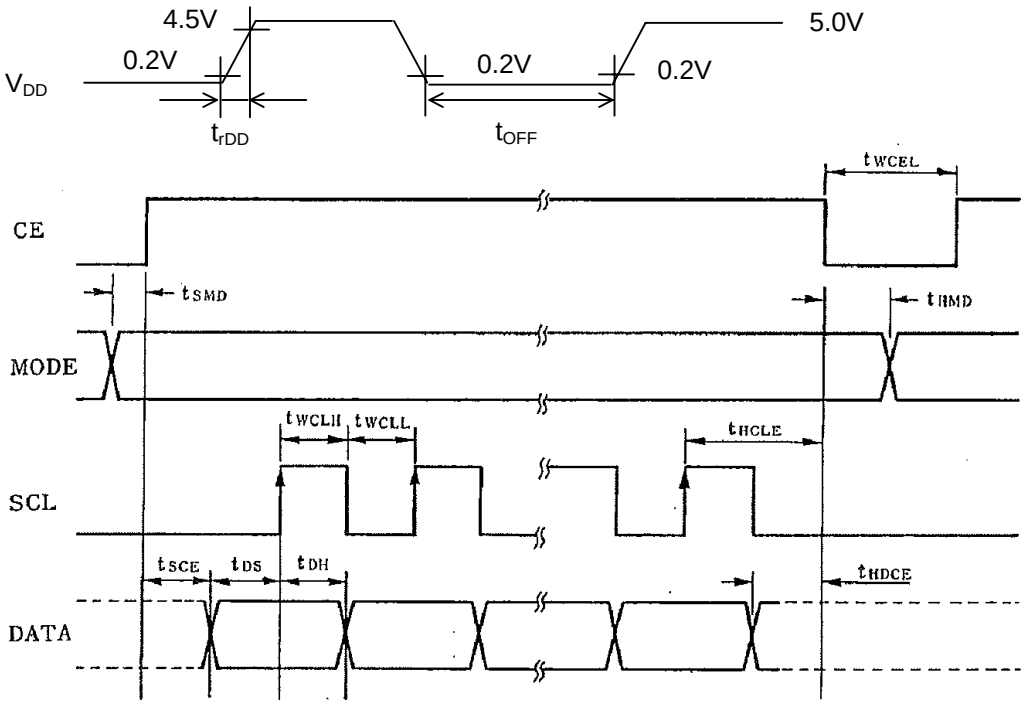


- AC Characteristics

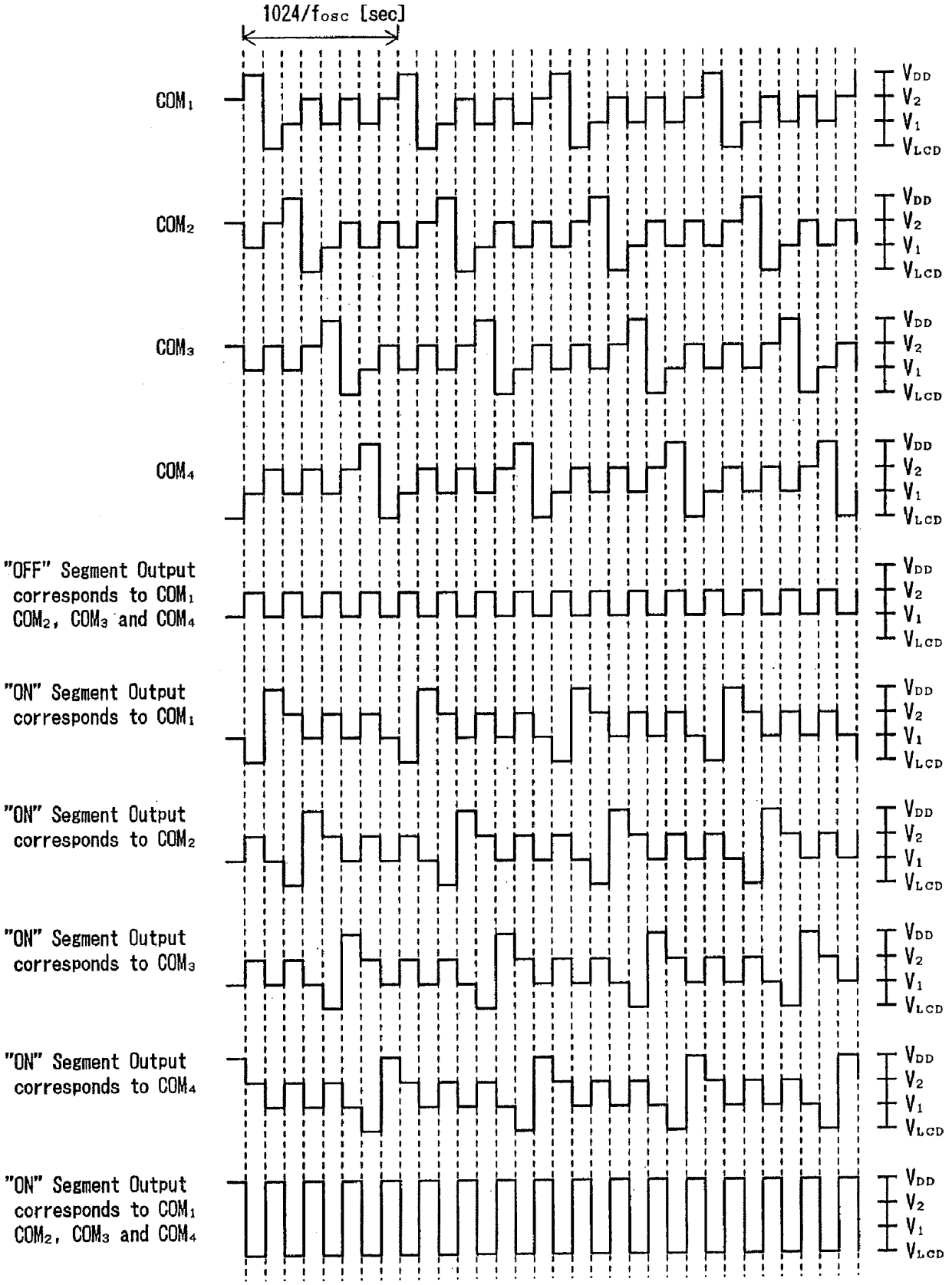
(Ta= 25°C, V_{DD}=5.0V, V_{SS}=0V, V_{LCD}=V_{DD}-6.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL	0.25			us
"H" Clock Pulse Width	t_{WCLH}	SCL	0.25			us
DATA Set-up Time	t_{DS}	SCL, DATA	0.25			us
DATA Hold Time	t_{DH}	SCL, DATA	0.25			us
CE Set-up Time	t_{SCE}	CE, DATA	1.0			us
CE Hold Time (1)	t_{HDCE}	CE, DATA	1.0			us
CE Hold Time (2)	t_{HCLE}	CE, SCL T	1.25			us
MODE Set-up Time	t_{SMD}	MODE, CE	0.25			us
MODE Hold Time	t_{HMD}	MODE, CE	0.25			us
"L" Chip Enable Pulse Width	t_{WCEL}	CE	4.0			us
Power Supply Rise Time	t_{rDD}	V_{DD}	0.1		10	ms
Power Supply OFF Time	t_{OFF}	V_{DD}	1			ms

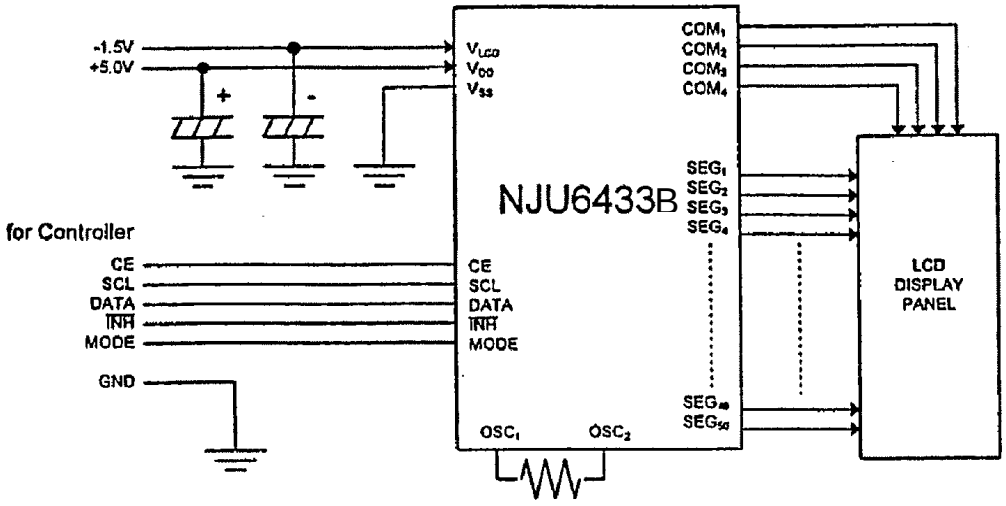
- Input Timing Characteristics



- LCD Driving Waveform(1/4DUTY · 1/3BIAS)



■ APPLICATION CIRCUIT



Note) The internal display data is undefined when V_{DD} is just turned on.
To avoid the meaningless display, please keep the INHb terminal at "L" until proper display data has been transferred.
In order to set the initial condition, 200-bit blank data or the first 200-bit data to be displayed should be transferred.