



3.3V CMOS 18-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHR16825

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCHR16825:

- Balanced Output Drivers: $\pm 12\text{mA}$
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit buffer/driver is built using advanced dual metal CMOS technology. The ALVCHR16825 improves the performance and density of 3-state memory address drivers, clockdrivers, and bus-oriented receivers and transmitters. The device can be used as two 9-bit buffers or one 18-bit buffer, and provides true data.

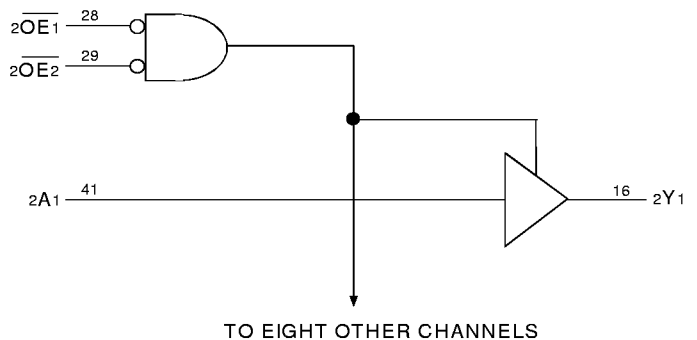
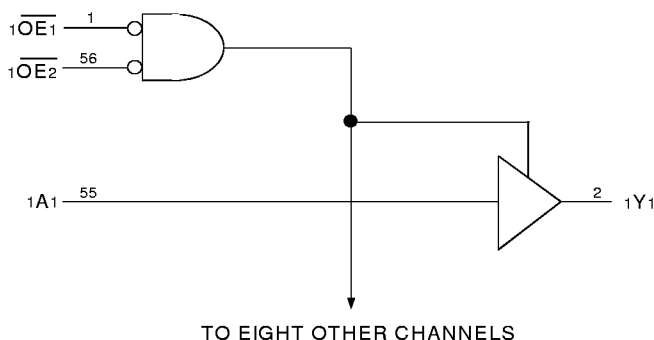
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{\text{OE}}1$ or $\overline{\text{OE}}2$) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver.

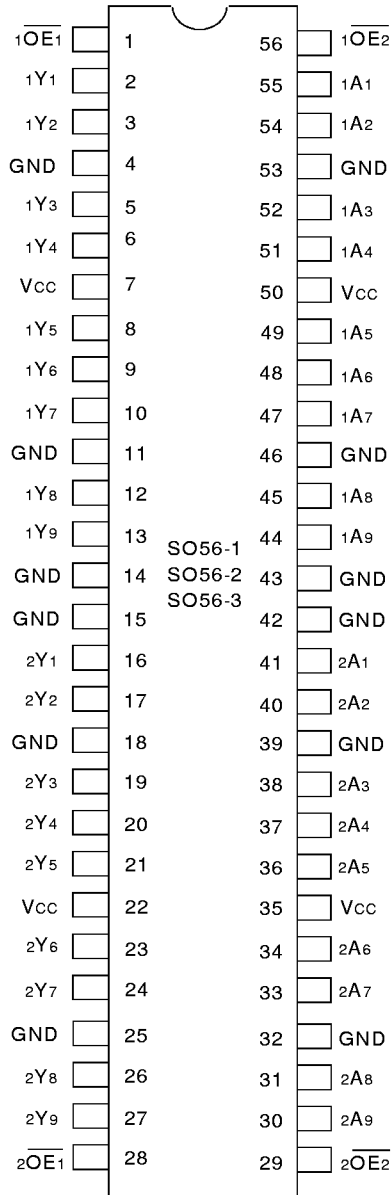
The ALVCHR16825 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

The ALVCHR16825 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



**SSOP/
TSSOP/TVSOP
TOP VIEW**

PIN DESCRIPTION

Pin Names	Description
$\overline{xOE_x}$	Output Enable Inputs (Active LOW)
xAx	Data Inputs ⁽¹⁾
xYx	3-State Outputs

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING ⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage Temperature	- 65 to + 150	°C
I_{OUT}	DC Output Current	- 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC} .

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (each 9-bit section) ⁽¹⁾

Inputs			Output
$\overline{xOE_1}$	$\overline{xOE_2}$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40° C to +85° C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	VI = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	VI = GND	—	—	± 5	
IoZH IoZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = VCC	—	—	± 10	μA
			VO = GND	—	—	± 10	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

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NOTE:

1. Typical values are at VCC = 3.3V, +25° C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	VI = 2.0V	– 75	—	—	μA
			VI = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	VI = 1.7V	– 45	—	—	μA
			VI = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	VI = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.

2. Typical values are at VCC = 3.3V, +25° C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -4mA	1.9	—	
			IOH = -6mA	1.7	—	
		VCC = 2.7V	IOH = -4mA	2.2	—	
			IOH = -8mA	2	—	
		VCC = 3.0V	IOH = -6mA	2.4	—	
			IOH = -12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	—	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	1	5	—	4.4	1	3.8	ns
tPZH tPZL	Output Enable Time xOEx to xYx	1	6.8	—	6.2	1	5.1	ns
tPHZ tPLZ	Output Disable Time xOEx to xYx	1.9	6.1	—	5.2	1.3	4.7	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

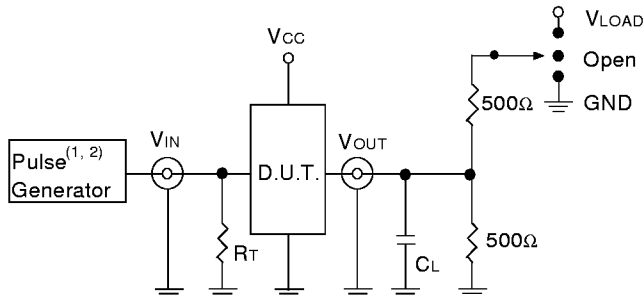
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	Vcc(1)= 3.3V±0.3V	Vcc(1)= 2.7V	Vcc(2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

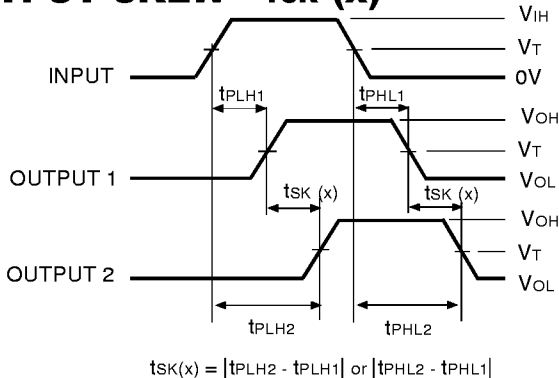
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

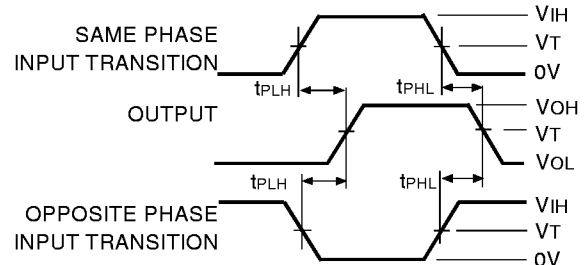


ALVC Link

NOTES:

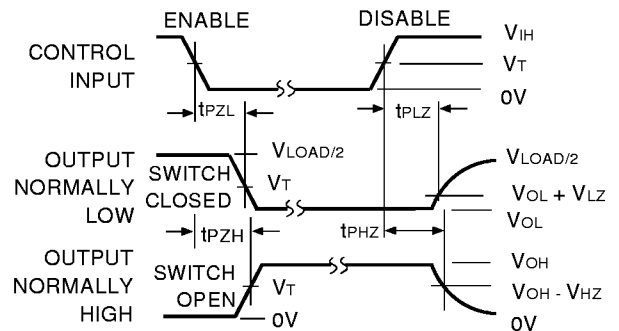
1. For t_{SK(o)} OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK(b)} OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

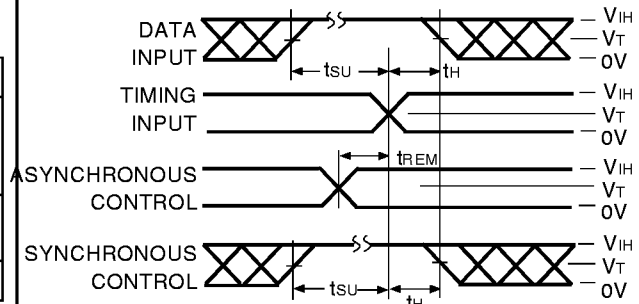


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NOTE:

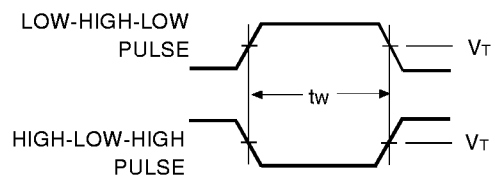
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					825		18-Bit Buffer/Driver with 3-State Outputs
				R16			Double-Density with Resistors, $\pm 12\text{mA}$
			H				Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

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