2 M x 8-Bit Dynamic RAM (2 k-refresh)

HYB 5117800AJ-50/-60/-70/-80

Preliminary Information

- 2097152 words by 8-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  - $\overline{RAS}$ access time:
    - 50 ns (-50 version)
    - 60 ns (-60 version)
    - 70 ns (-70 version)
    - 80 ns (-80 version)
  - Cycle time:
    - 95 ns (-50 version)
    - 110 ns (-60 version)
    - 130 ns (-70 version)
    - 150 ns (-80 version)
  - $\overline{CAS}$ access time:
    - 15 ns (-50,-60 version)
    - 20 ns (-70,-80 version)
- Fast page mode cycle time
  - 35 ns (-50 version)
  - 40 ns (-60 version)
  - 45 ns (-70 version)
  - 50 ns (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  - max. 660 active mW (-50 version)
  - max. 605 active mW (-60 version)
  - max. 550 active mW (-70 version)
  - max. 495 active mW (-80 version)
  - 11 mW standby (TTL)
  - 5.5. mW standby (MOS)
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, test mode
- Fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 2048 refresh cycles/ 32 ms
- Plastic Package: P-SOJ-28-3 400 mil

The HYB 5117800AJ is the new generation dynamic RAM organized as 2097152 words by 8-bits. The HYB 5117800AJ utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 5117800AJ to be packaged in a standard SOJ 28 400 mil plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

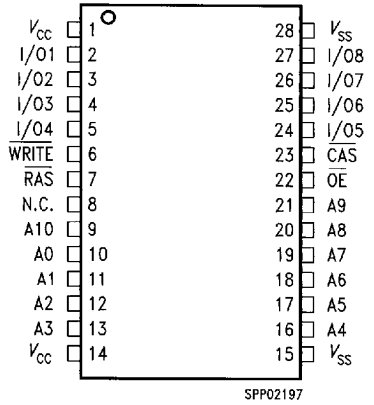
Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 5117800AJ-50	Q67100-Q888	P-SOJ-28-3 400 mil	DRAM (access time 50 ns)
HYB 5117800AJ-60	Q67100-Q889	P-SOJ-28-3 400 mil	DRAM (access time 60 ns)
HYB 5117800AJ-70	Q67100-Q890	P-SOJ-28-3 400 mil	DRAM (access time 70 ns)
HYB 5117800AJ-80	Q67100-Q891	P-SOJ-28-3 400 mil	DRAM (access time 80 ns)

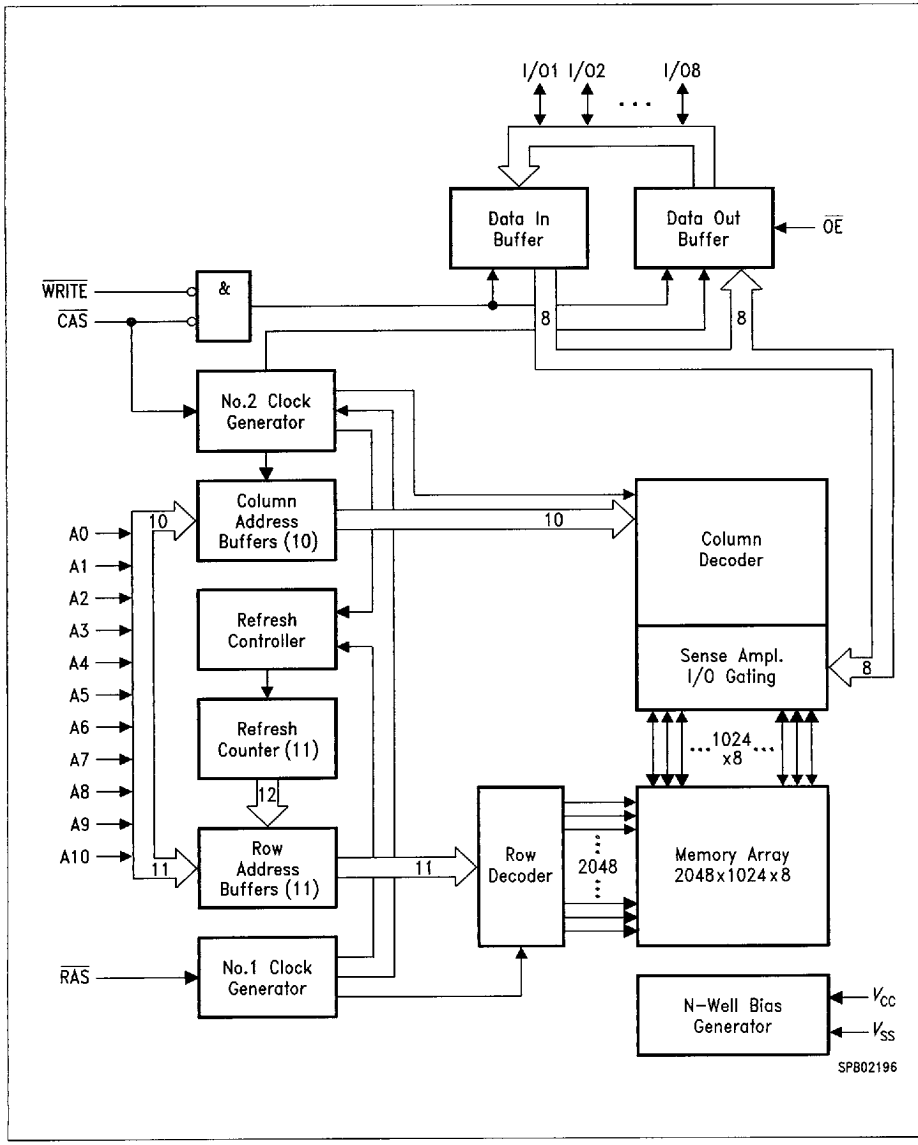
Pin Names

A0-A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

P-SOJ-28-3 (400mil)



Pin Configuration



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (Vcc+0.5,7.0) V
Power supply voltage ..... – 1.0V to 7.0 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current,any input (0 V ≤ V_{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ Vcc + 0.3V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
-50 ns version		–	120	mA	2) 3) 4)
-60 ns version		–	110	mA	2) 3) 4)
-70 ns version		–	100	mA	2) 3) 4)
-80 ns version		–	90	mA	2) 3) 4)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles:	I_{CC3}				
-50 ns version		–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
-80 ns version		–	90	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)					

Notes see page 283.

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version	I_{CC4}	–	90	mA	2) 3) 4)
-60 ns version		–	80	mA	2) 3) 4)
-70 ns version		–	70	mA	2) 3) 4)
-80 ns version		–	65	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	120	mA	2) 4)
-60 ns version		–	110	mA	2) 4)
-70 ns version		–	100	mA	2) 4)
-80 ns version		–	90	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)					

Notes see page 283.

AC Characteristics [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values								Unit
		-50		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	95	–	110	–	130	–	150	–	ns
Read-write cycle time	t_{RWC}	135	–	150	–	180	–	200	–	ns
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns
Fast page mode read-write cycle time	t_{PRWC}	75	–	80	–	95	–	100	–	ns
Access time from $\overline{RAS}$ [7) 12)]	t_{RAC}	–	50	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$ [7) 12)]	t_{CAC}	–	15	–	15	–	20	–	20	ns
Access time from column address [7) 13)]	t_{AA}	–	25	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge [7)]	t_{CPA}	–	30	–	35	–	40	–	45	ns
$\overline{CAS}$ to output in low-Z [7)]	t_{CLZ}	0	–	0	–	0	–	0	–	ns
Output buffer turn-off delay [8)]	t_{OFF}	0	15	0	15	0	20	0	20	ns
Transition time (rise and fall) [6)]	t_T	3	50	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	35	–	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	80	10k	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	70	200k	80	200k	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	30	–	35	–	40	–	45	–	ns
$\overline{CAS}$ precharge to $\overline{WE}$ (FPMR RMW)	t_{CPWD}	50	–	55	–	65	–	70	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15		15	–	20	–	20	-	ns
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	80	–	ns

Notes see page 283.

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values								Unit
		-50		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	15	10k	20	10k	20	10k	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [12]	t_{RCD}	20	35	20	45	20	50	20	60	
$\overline{RAS}$ to column address delay time [13]	t_{RAD}	15	25	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	10	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	10	–	15	–	15	–	15	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read command hold time [9]	t_{RCH}	0	–	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [9]	t_{RRH}	0	–	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	15	–	ns

Notes see page 283.

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values								Unit
		-50		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	min.	max.	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	15	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	15	–	20	–	20	–	ns
Data setup time [10]	t_{DS}	0	–	0	–	0	–	0	–	ns
Data hold time [10]	t_{DH}	10	–	15	–	15	–	15	–	ns
Refresh period	t_{REF}	–	32	–	32	–	32	–	32	ms
Write command setup time [11]	t_{WCS}	0	–	0	–	0	–	0	–	ns
$\overline{CAS}$ to $\overline{WRITE}$ delay time [11]	t_{CWD}	35	–	35	–	45	–	45	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ delay time [11]	t_{RWD}	70	–	80	–	95	–	105	–	ns
Column address to $\overline{WRITE}$ delay time [11]	t_{AWD}	45	–	50	–	60	–	65	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30	–	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	35	–	40	–	40	–	40	–	ns
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	10	–	10	–	ns
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	10	–	10	–	ns

Notes see page 283.

AC Characteristics (cont'd) [5]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values								Unit
		-50		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	min.	max.	
Write to $\overline{RAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRP}	10	–	10	–	10	–	10	–	ns
Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{WRH}	10	–	10	–	10	–	10	–	ns
$\overline{OE}$ command hold time	t_{OEH}	15	–	15	–	20	–	20	–	ns
$\overline{OE}$ access time	t_{OEA}	–	15	–	15	–	20	–	20	ns
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	20	ns
Data to $\overline{CAS}$ low delay [15]	t_{DZC}	0	–	0	–	0	–	0	–	ns
Data to $\overline{OE}$ low delay [15]	t_{DZO}	0	–	0	–	0	–	0	–	ns
$\overline{CAS}$ high to data delay [16]	t_{CDD}	15	–	15	–	20	–	20	–	ns
$\overline{OE}$ high to data delay [16]	t_{ODD}	15	–	15	–	20	–	20	–	ns

Notes see page 283.

Capacitance

T_A = 0 to 25 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O8)	C_{IO}	–	7	pF

Notes for pages 277 to 282:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a fast page mode cycle (t_{PC}).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

7) Measured with a load equivalent to 2 TTL loads and 100 pF.

8) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

9) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.

11) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$, $t_{AWD} \geq t_{AWD\ (min.)}$ and $t_{CPWD} \geq t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.

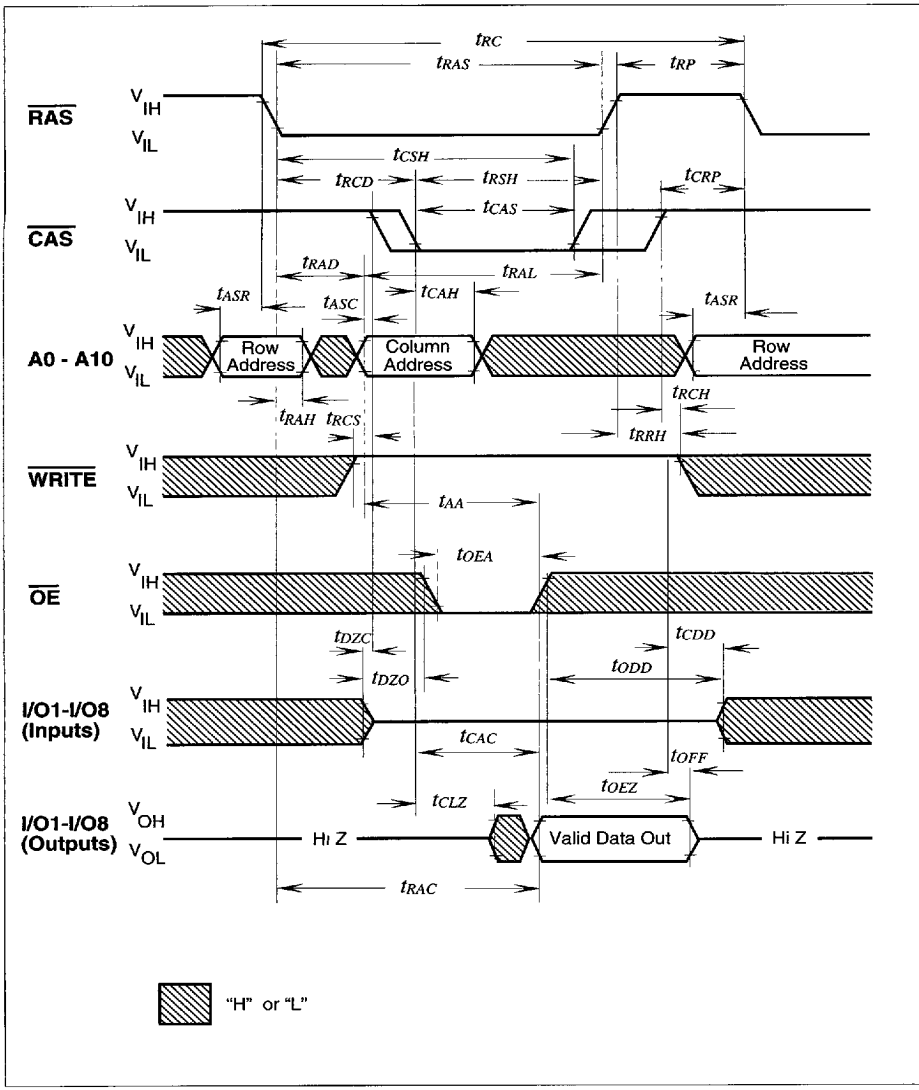
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.

14) AC measurements assume $t_T = 5$ ns.

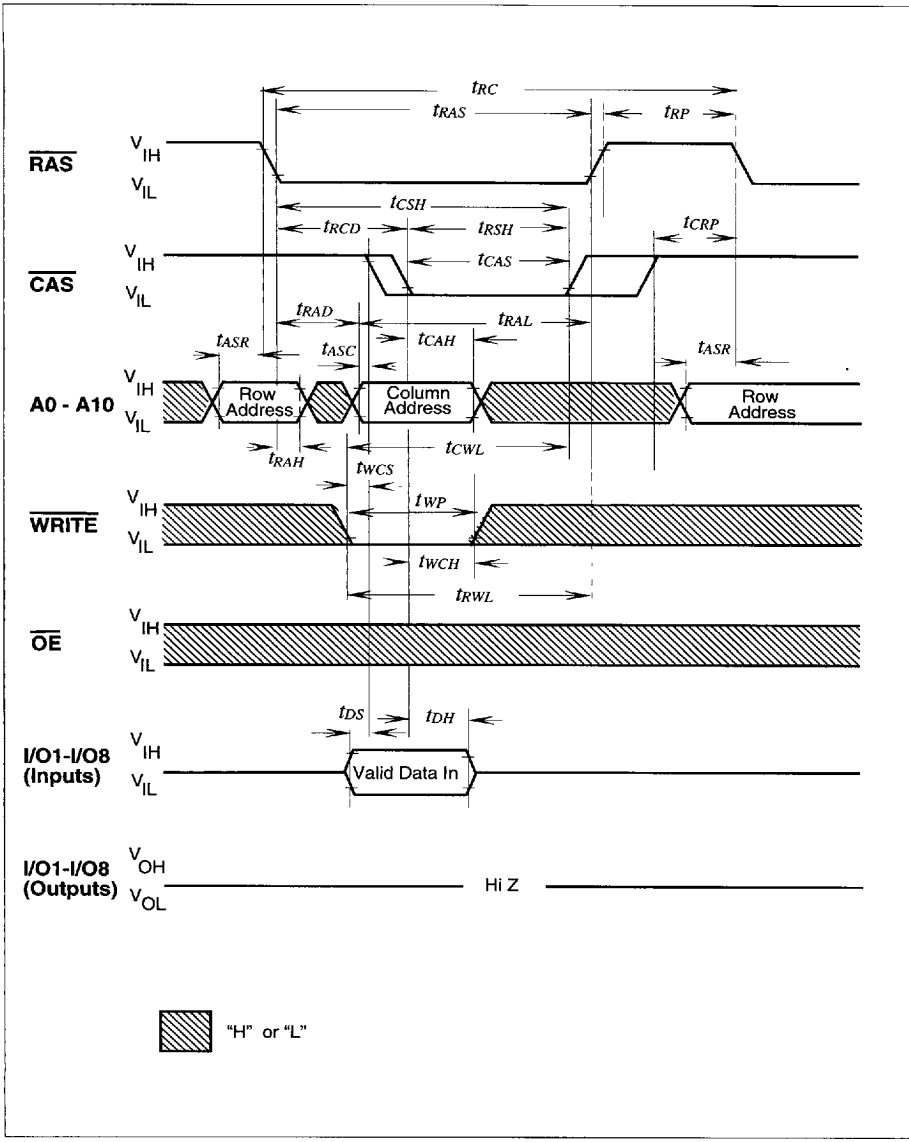
15) Either t_{DZC} or t_{DZO} must be satisfied.

16) Either t_{CDD} or t_{ODD} must be satisfied.

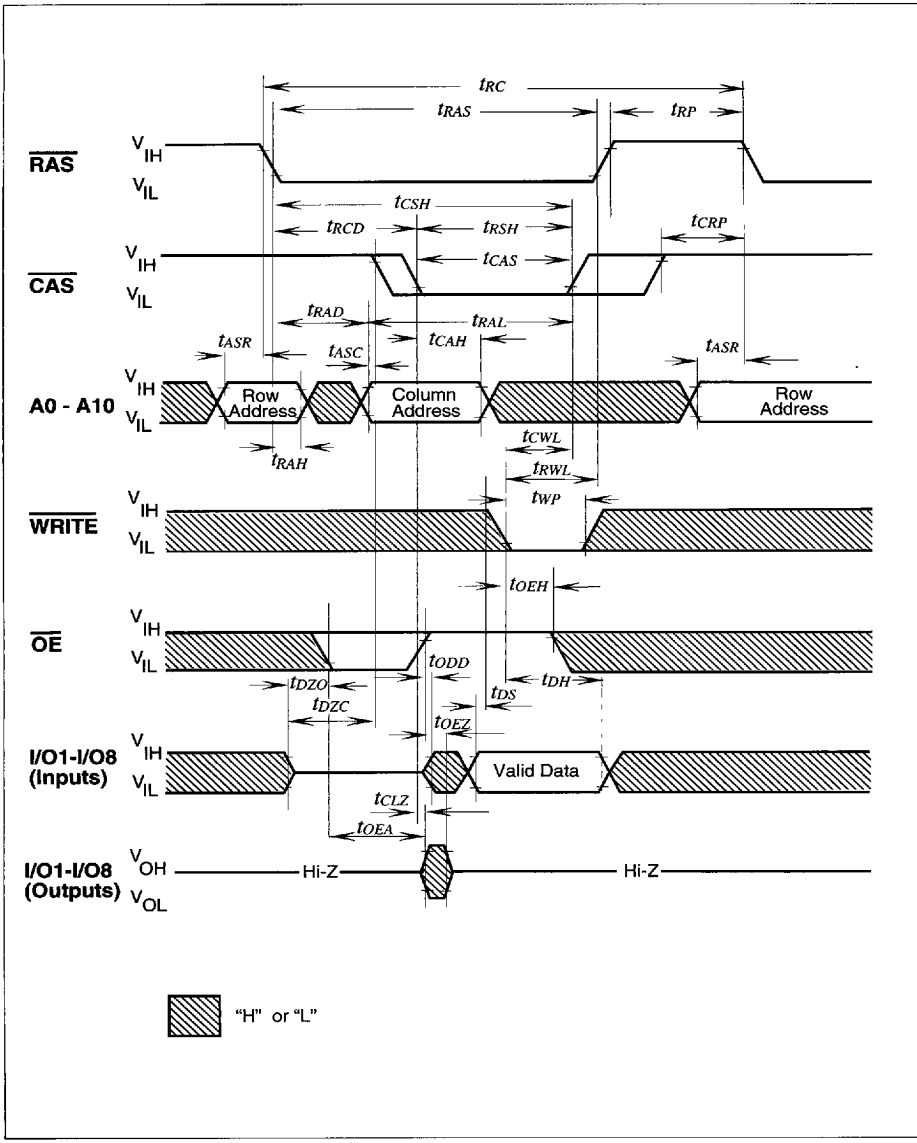
Waveforms



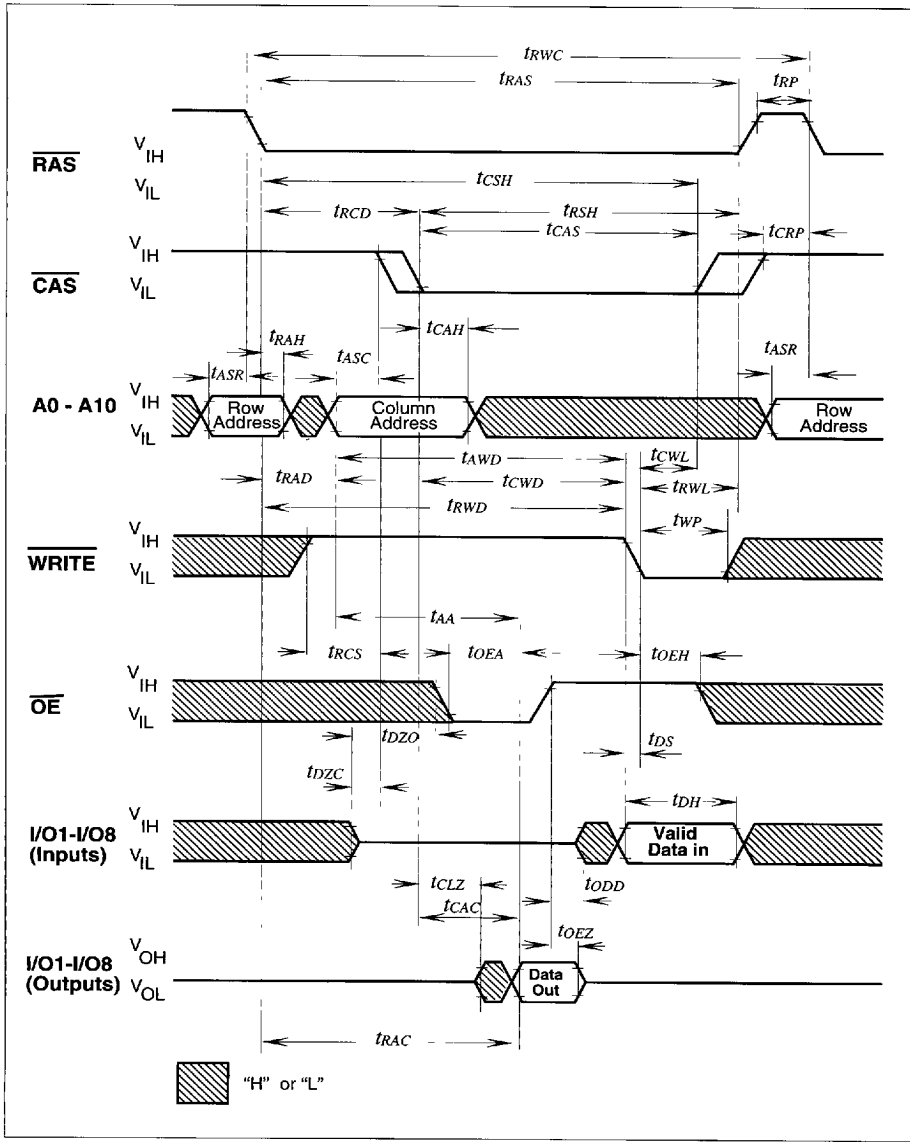
Read Cycle



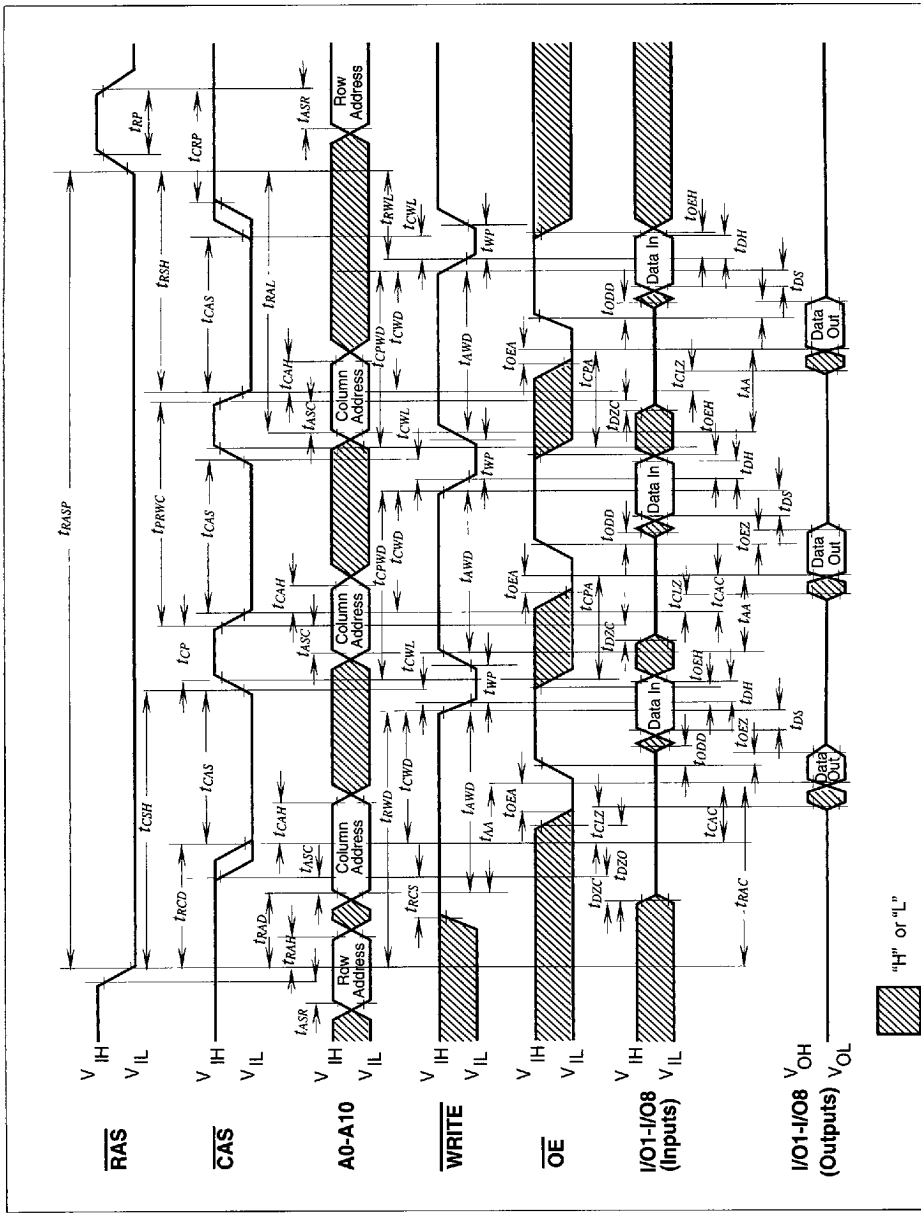
Write Cycle (Early Write)



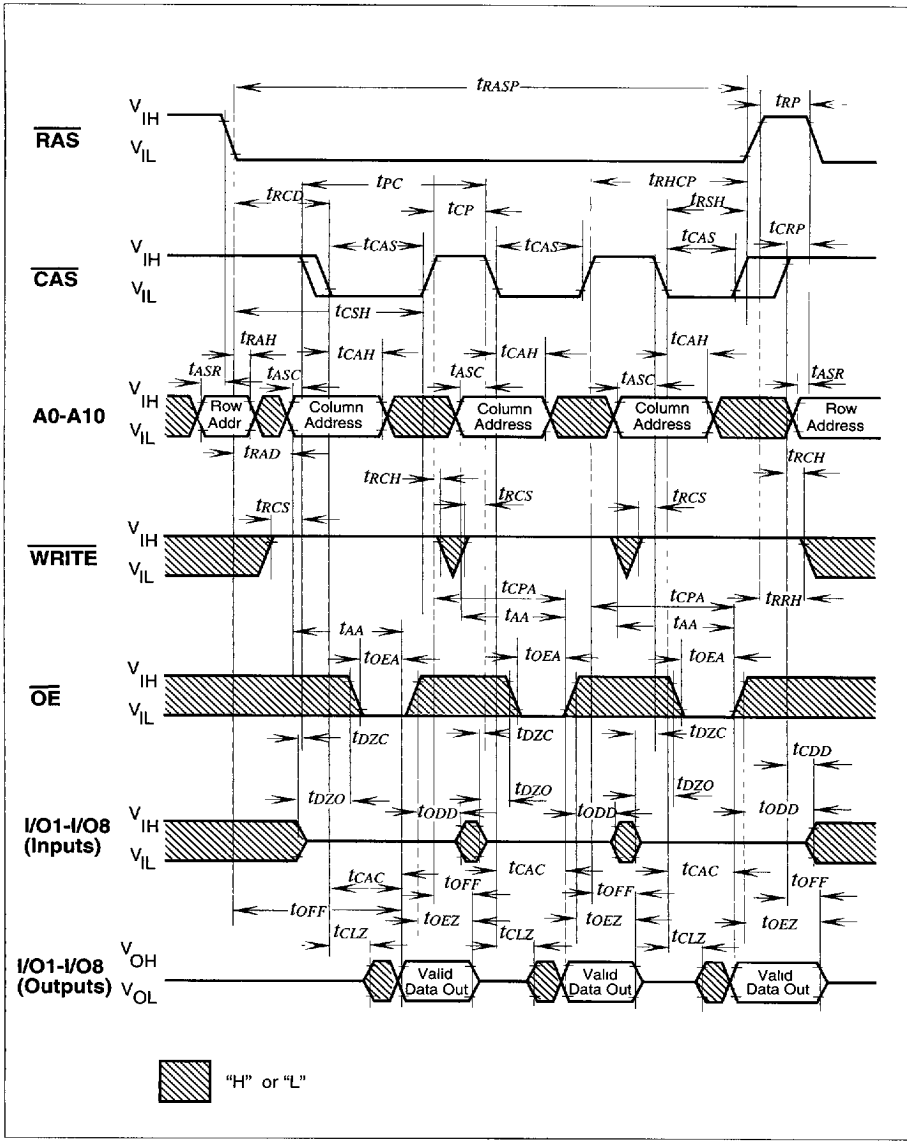
Write Cycle (OE Controlled Write)



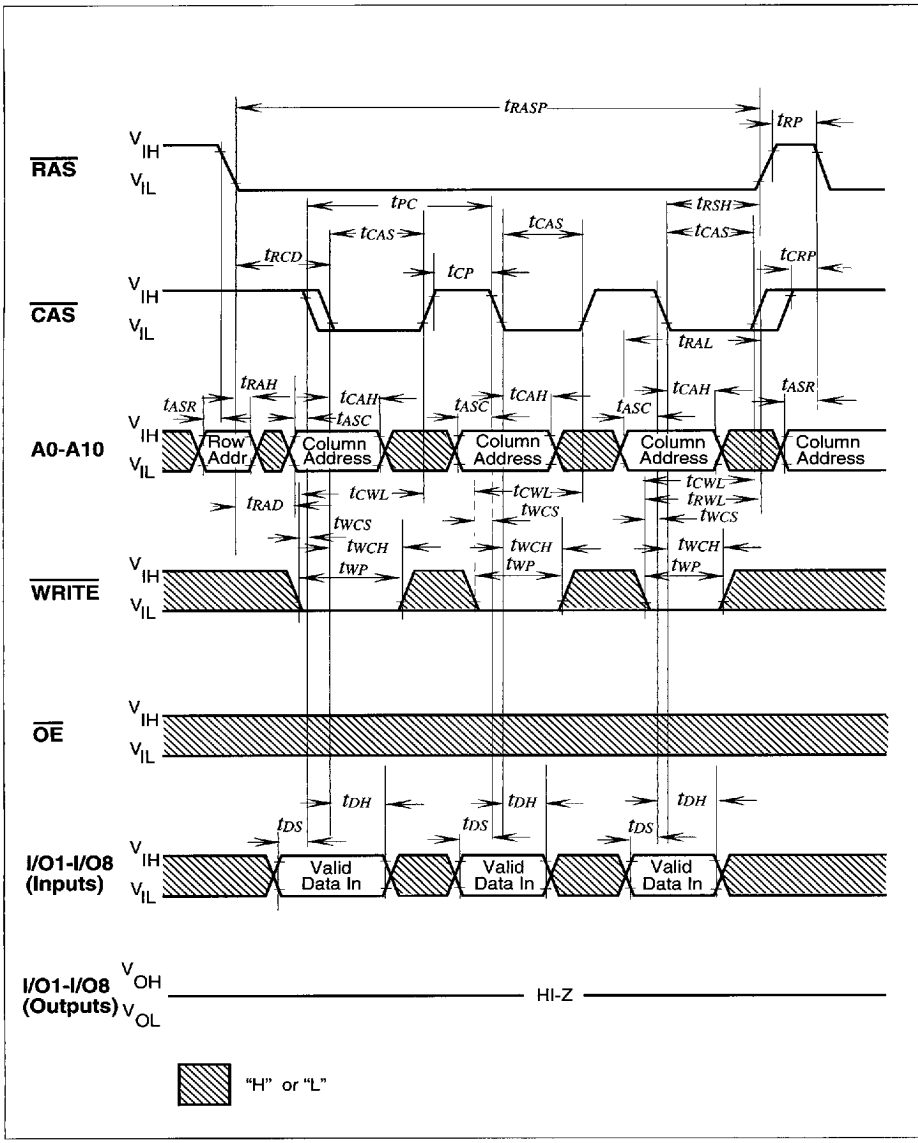
Read-Write (Read-Modify-Write) Cycle



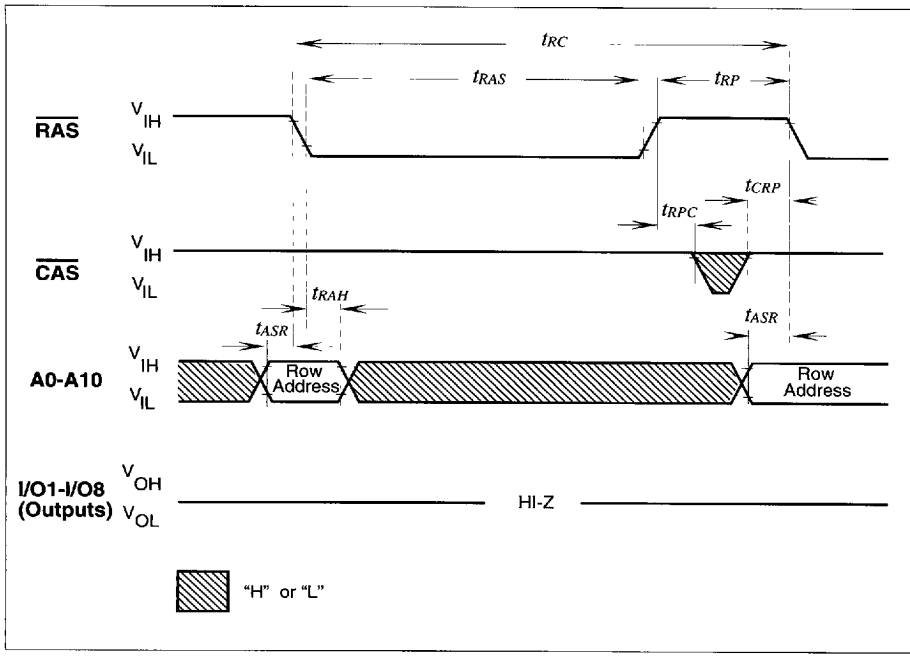
Fast Page Mode Read-Modify-Write Cycle



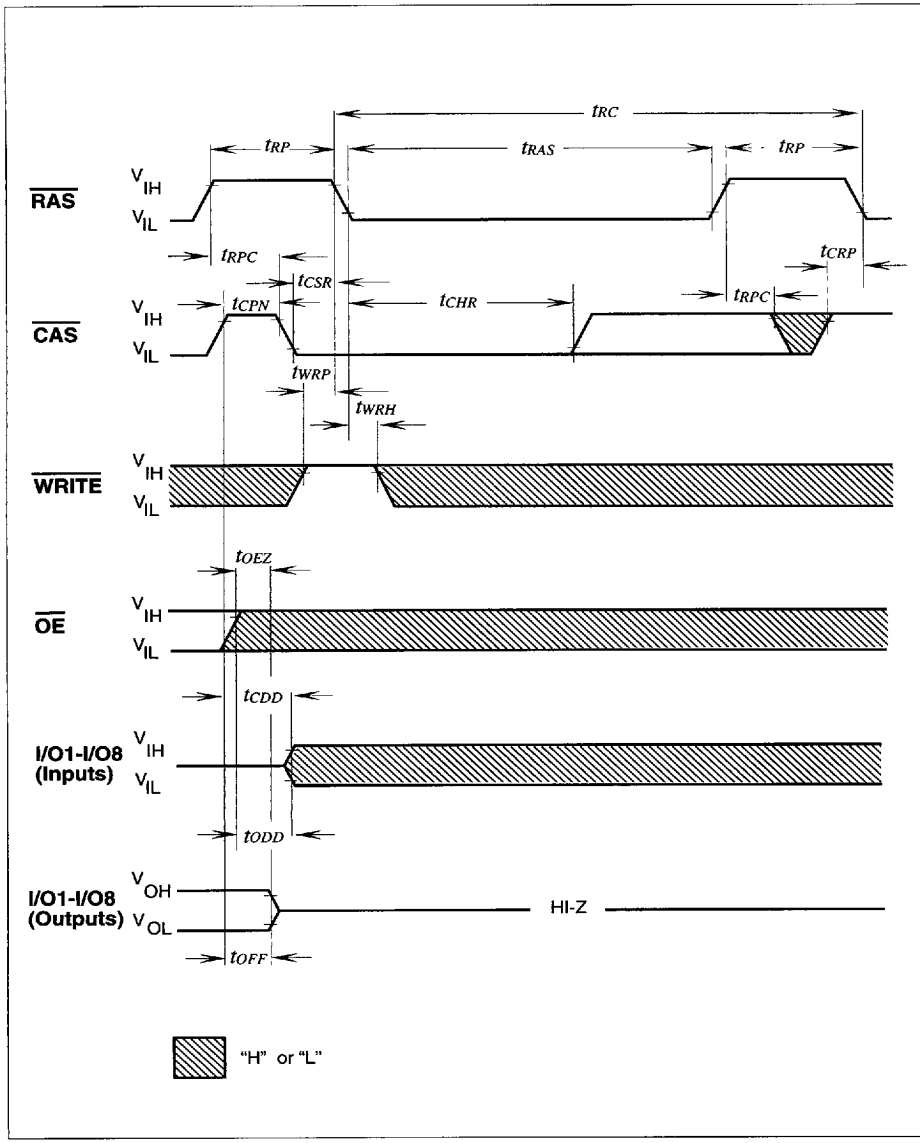
Fast Page Mode Read Cycle



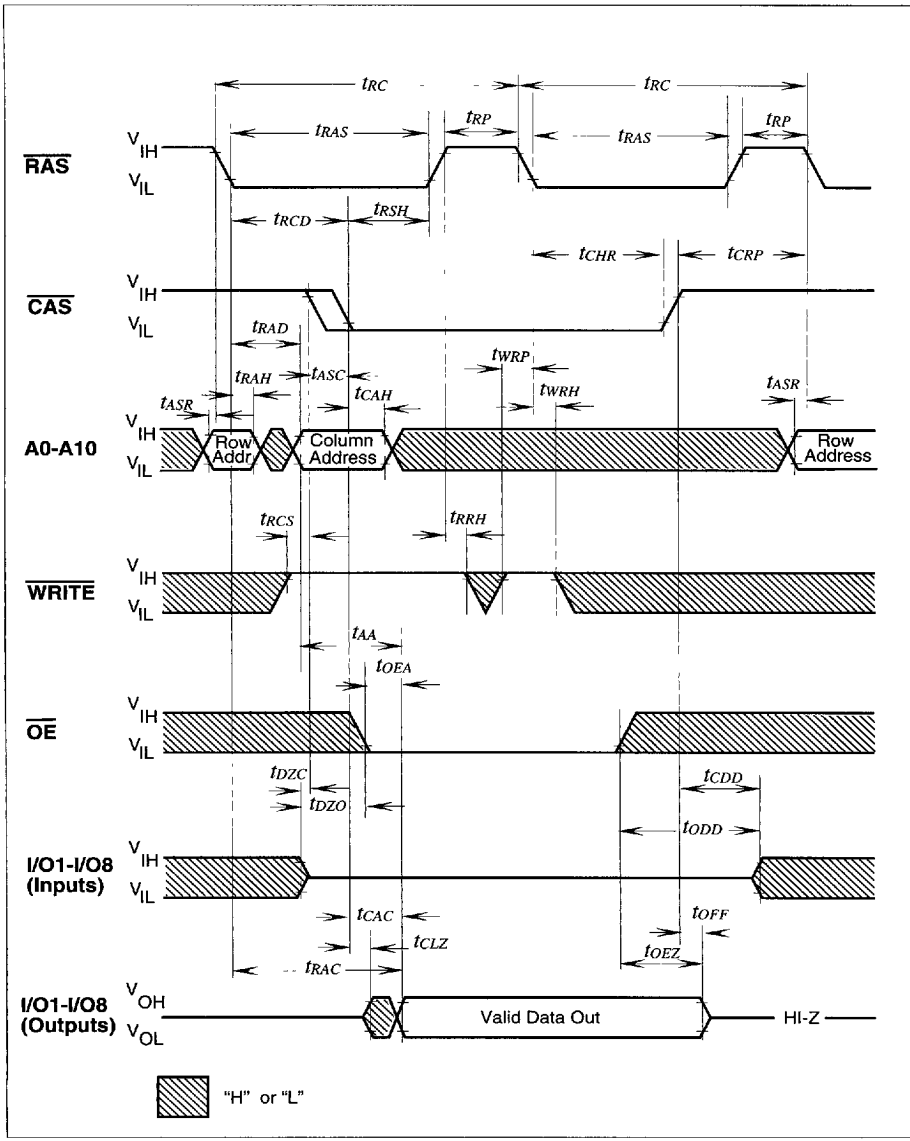
Fast Page Mode Early Write Cycle



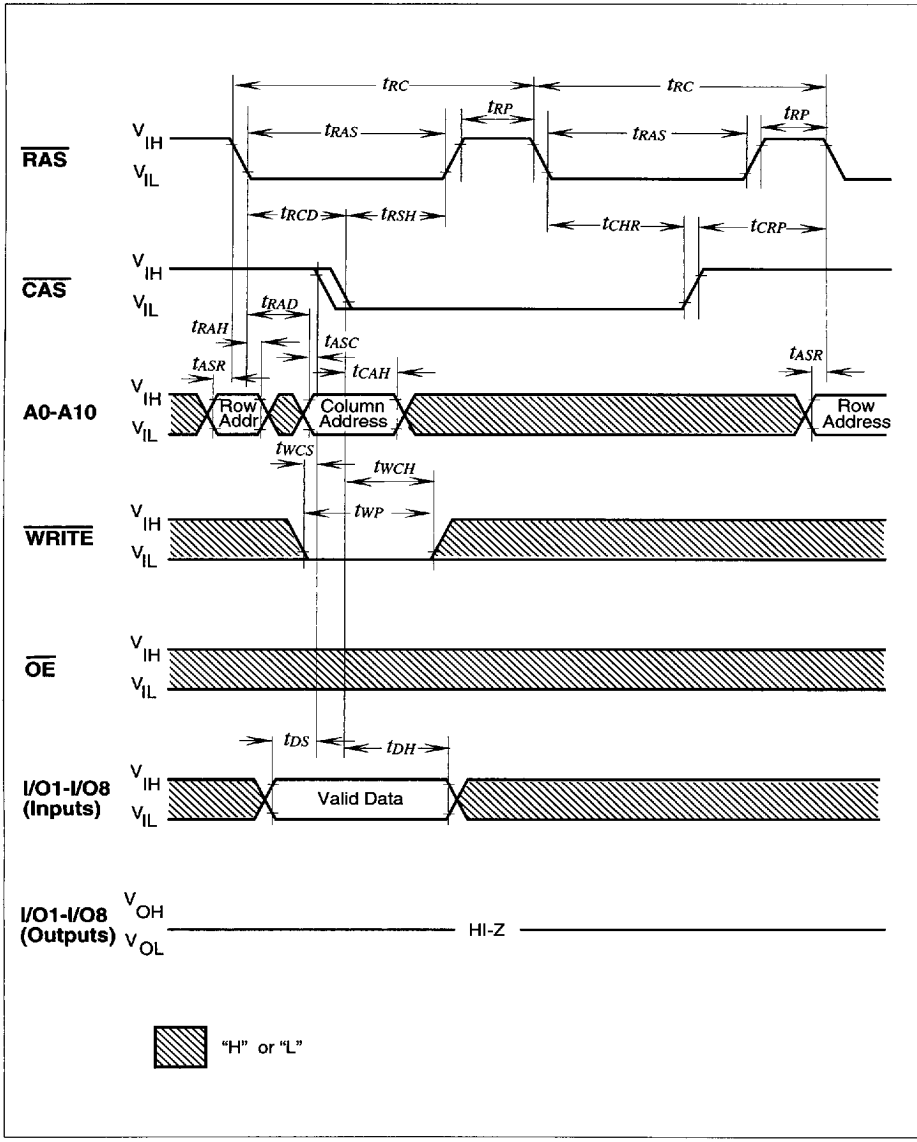
RAS-Only Refresh Cycle



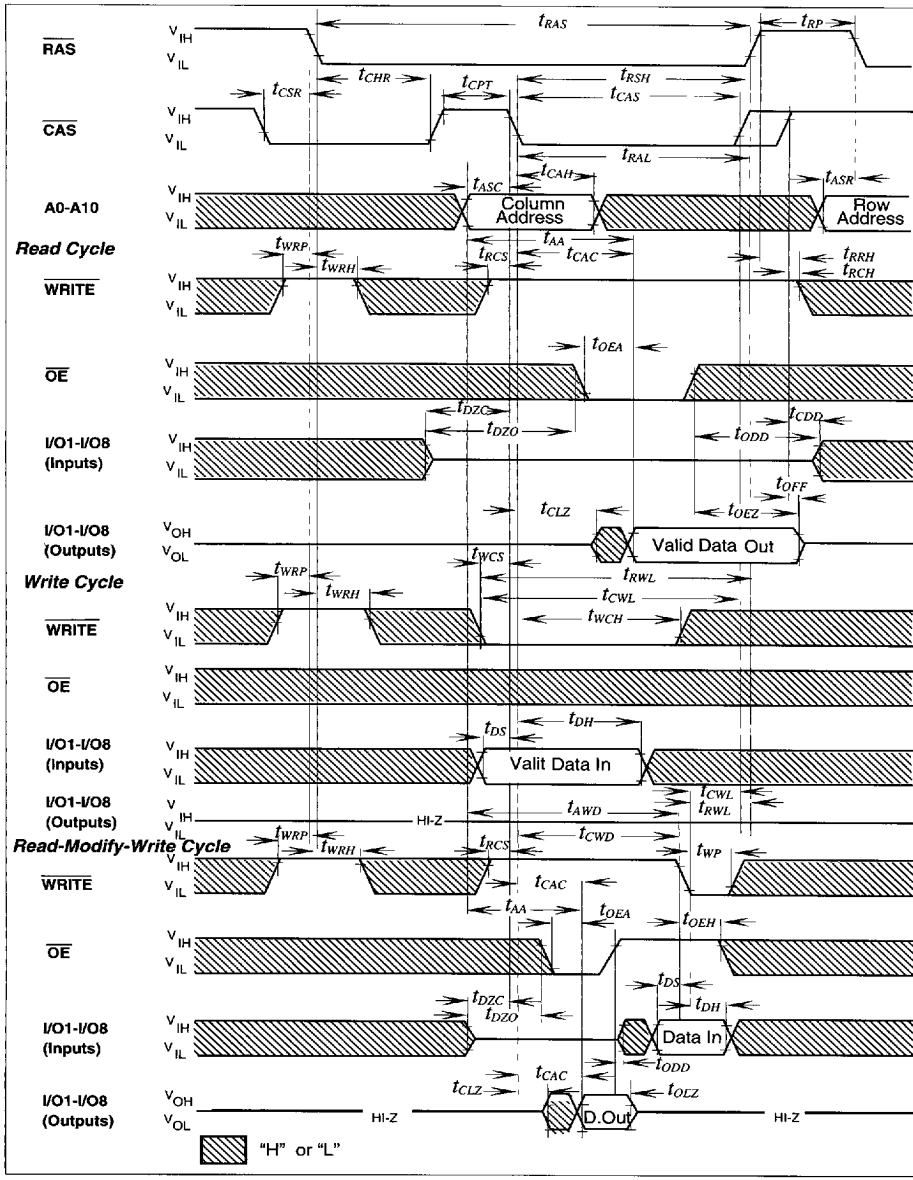
CAS-Before-RAS Refresh Cycle



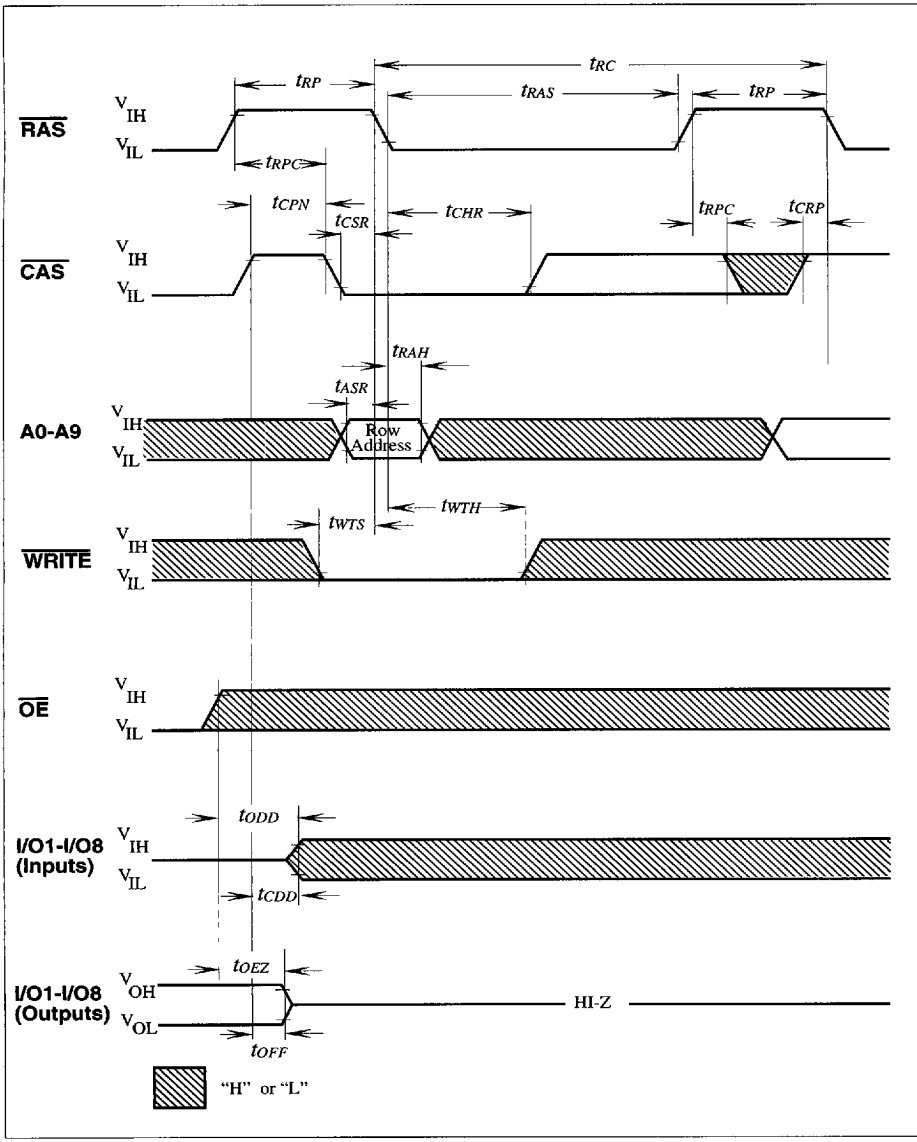
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry

Test Mode

As the HYB 5117800AJ is organized internally as 1 M x 16-bits, a test mode cycle using 2:1 compression can be used to improve test time. Note that in the 2 M x 8 version the test time is reduced by 1/2 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WRITE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cylces.

Row addresses A0 through A9 have to kept high to perform a testmode entry cycle. All other addresses are don't care.