National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC411A-X REV 0A0

Original Creation Date: 02/11/99
Last Update Date: 11/04/99
Last Major Revision Date: 05/06/99

High-Speed Video Op Amp with Disable

General Description

The Comlinear CLC411 combines a state-of-the-art complementary bipolar process with Comlinear's patented current-feedback architecture to provide a very high-speed op amp operating from ±15V supplies. Drawing only 11mA quiescent current, the CLC411 provides a 200MHz small signal bandwidth and a 2300V/us slew rate while delivering a continuos 70mA current output with ±4.5V output swing. The CLC411's high-speed performance includes a 15ns settling time to 0.1%(2V step) and a 2.3ns rise and fall time (6V step).

The CLC411 is designed to meet the requirements of professional broadcast video systems including composite video and high definition television. The CLC411 exceeds the HDTV standard for gain flatness to 30MHz with it's ±0.05dB flat frequency response and exceeds composite video standards with its very low differential gain and phase errors of 0.02%, 0.03Degrees. The CLC411 is the op amp of choice for all video systems requiring upward compatibility from NTSC and PAL to HDTV.

The CLC411 features a very fast disable/enable (10ns/55ns) allowing the multiplexing of high-speed signals onto an analog bus through the common output connections of multiple CLC411's. Using the same signal source to drive disable/enable pins is easy since "break-before-make" is guaranteed.

Industry Part Number

CLC411A

NS Part Numbers

CLC411AJ-QML

Prime Die

UB1590C

Controlling Document

5962-9456601MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 200MHz small signal bandwidth (1Vpp)
- ±0.05dB gain flatness to 30MHz
- 0.02%, 0.03Degrees differential gain, phase
- 2300V/us slew rate
- 10ns disable to high-impedance output
- 70mA continuous output current
- ±4.5V output swing into 100 Ohm load
- ±4.0V input voltage range

Applications

- HDTV amplifier
- Video line driver
- High-speed analog bus driver
- Video signal multiplexer
- DAC output buffer

(Absolute Maximum Ratings)

Supply Voltage (Vs) (Note 1)	±18 V dc
Output current (Iout)	125 mA
Maximum Power dissipation (Pd) (Note 2)	1.34W
Junction temperature (Tj)	+175C
Lead temperature (soldering, 10 seconds)	+300C
Differential input voltage (Vid)	±15 V
Common mode input voltage (Vcm)	±Vs
Storage temperature range	-65C to +150C
Thermal Resistance	
ThetaJA	
Ceramic DIP (Still Air)	97 C/W
Ceramic DIP (500LF/Min Air Flow)	59 C/W
ThetaJC	20 C/W
Package Weight (typical)	
Ceramic DIP	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±15Vdc
Gain Range (Av)	±10 to ±1000V/V
Ambient Operating Temperature Range (TA)	-55 C to +125 C

Electrical Characteristics

Static and dc tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iib	Input bias current				0	30	uA	1
					-20	20	uA	2
					0	65	uA	3
-Iib	Input bias current				-30	30	uA	1, 2
					-40	40	uA	3
Vio	Input offset voltage				-9	9	mV	1
					-14	14	mV	2
					-13	13	mV	3
+Dib	Average input bias current drift	Ta = +125C, -55C	1		-250	250	nA/C	2
			1		-400	400	nA/C	3
-Dib	Average input bias current drift	Ta = +125C, -55C	1		-150	150	nA/C	2
			1		-200	200	nA/C	3
DVio	Average input offset voltage drift	Ta = +125C, -55C	1		-50	50	uV/C	2, 3
Icc	Supply current	No load				12	mA	1, 2
						14	mA	3
Iccd	Supply current	Disable				3.5	mA	1
						4.5	mA	2, 3
PSRR	Power supply rejection ratio	+Vs = +4.5 V to +5.0 V, -Vs = -4.5 V to -5.0 V			50		dB	1
					48		dB	2, 3
CMRR	Common mode rejection ration	Vcm = ±1 V	1		46		dB	4
			1		44		dB	5, 6

Electrical Characteristics

Frequeuncy domain tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small signal bandwith	-3 dB bandwidth, Vout < 1.0 Vpp			150		MHz	4
			2		110		MHz	5
			2		150		MHz	6
LSBW	Large signal bandwith	-3 dB bandwidth, Vout < 6.0 Vpp	1		50		MHz	4, 6
			1		40		MHz	5
GFPH	Gain flatness peaking high	0.1 MHz to 200 MHz, Vout ≤ 1.0 Vpp				0.5	dB	4
			2			0.6	dB	5, 6
GFPL	Gain flatness peaking low	0.1 MHz to 30 MHz, Vout ≤ 1.0 Vpp				0.2	dB	4
			2			0.3	dB	5
			2			0.2	dB	6
GFRL	Gain flatness rolloff Low	0.1 MHz to 30 MHz, Vout ≤ 1.0 Vpp				0.2	dB	4
			2			0.4	dB	5
			2			0.2	dB	6
GFRH	Gain flatness rolloff High	0.1 MHz to 60 MHz, Vout ≤ 1.0 Vpp				0.4	dB	4
			2			0.7	dB	5, 6
LPD	Linear phase deviation	0.1 MHz to 60 MHz, Vout ≤ 1.0 Vpp	1			1.0	Deg	4, 5, 6

Distortion and noise tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

HD2	Second harmonic distortion	2 Vpp at 20 MHz				-35	dBc	4
			2			-35	dBc	5, 6
HD3	Third harmonic distortion	2 Vpp at 20 MHz				-42	dBc	4
			2			-35	dBc	5
			2			-42	dBc	6

Electrical Characteristics

Timing tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ts	Settling time	2 V step at 0.1% of the fixed value	1			18	ns	9
			1			23	ns	10, 11
OS	Overshoot	2.0 V step	1			10	%	9
			1			15	5	10, 11

Miscellaneous performance tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

Rin	Input Resistance		1		750		kOhms	1
			1		1000		kOhms	2
			1		250		kOhms	3
Cin	Input capacitance		1			3	pF	1, 2, 3
Vout	Output voltage range	No load, Ta = +25C	1		-4.5	4.5	V	1
Voutl	Output voltage range	Rl = 100Ohms, Ta = +25C	1		-4.0	4.0	V	1
CMIR	Common mode input voltage range	Ta = +25C	1		-3.5	3.5	V	1
Iout	Output current		1		50		mA	1
			1		40		mA	2
			1		30		mA	3

Disable and enable tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15 V dc, Av = +2, Rl = 100 Ohms, Rf = 300 Ohms, Rg = 300 Ohms, -55C ≤ Ta ≤ +125 C (note 3)

Toff	Disable time	To > 50 dB attenuation at 10 MHz	1			30	ns	9, 11
			1			60	ns	10
Vdis	Voltage at /DIS pin to disable		1			3.0	V	1, 2, 3
Ven	Voltage at /DIS pin to enable		1		6.5		V	1, 2
			1		7.0		V	3
OSD	Off isolation	At 10 MHz	1			55	dB	4, 5, 6

Note 1: If not tested, shall be guaranteed to the limits specified.
Note 2: Group A testing only.

(Continued)

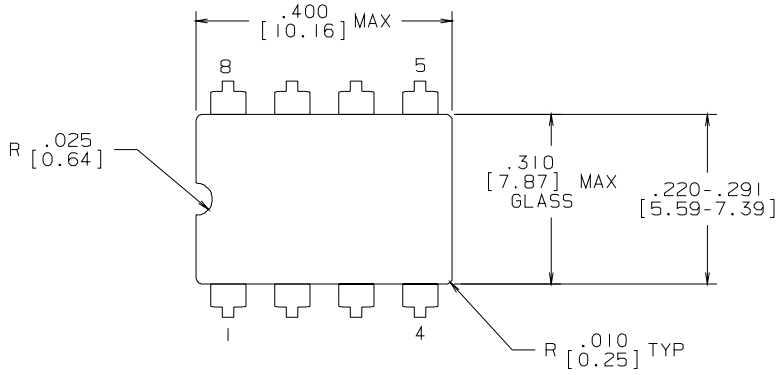
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

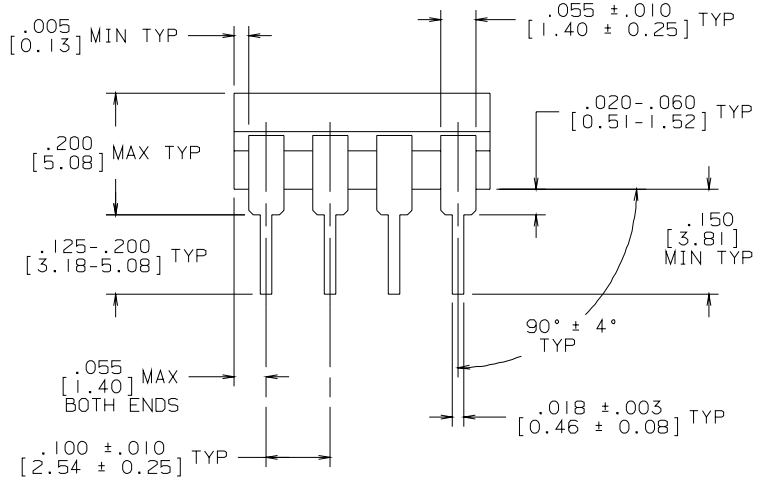
Graphics and Diagrams

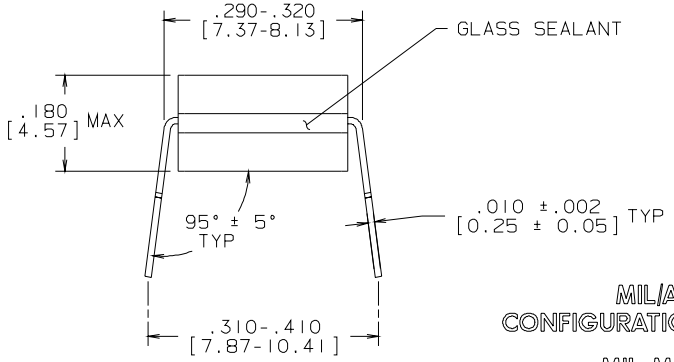
GRAPHICS#	DESCRIPTION
07087HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000417A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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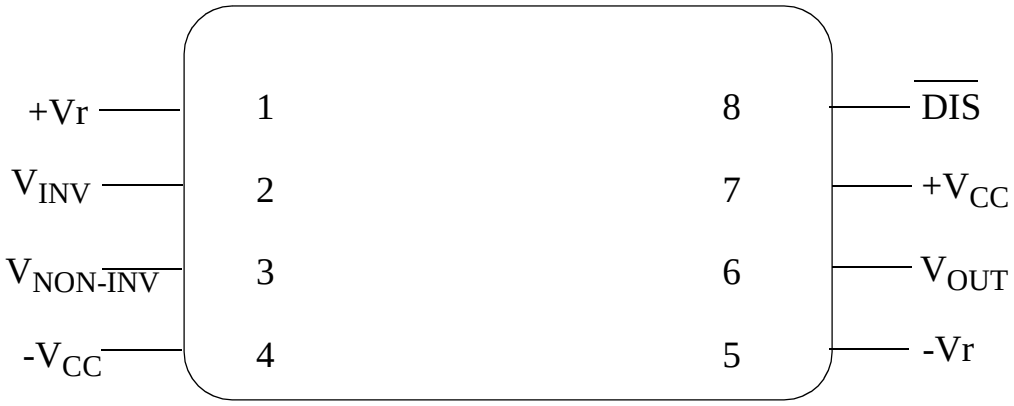
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC411J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000417A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003592	11/04/99	Shaw Mead	Initial MDS Release