



Am29030™ and Am29035™

RISC Microprocessors with 8-Kbyte/4-Kbyte Instruction Cache

Am29030 MICROPROCESSOR DISTINCTIVE CHARACTERISTICS

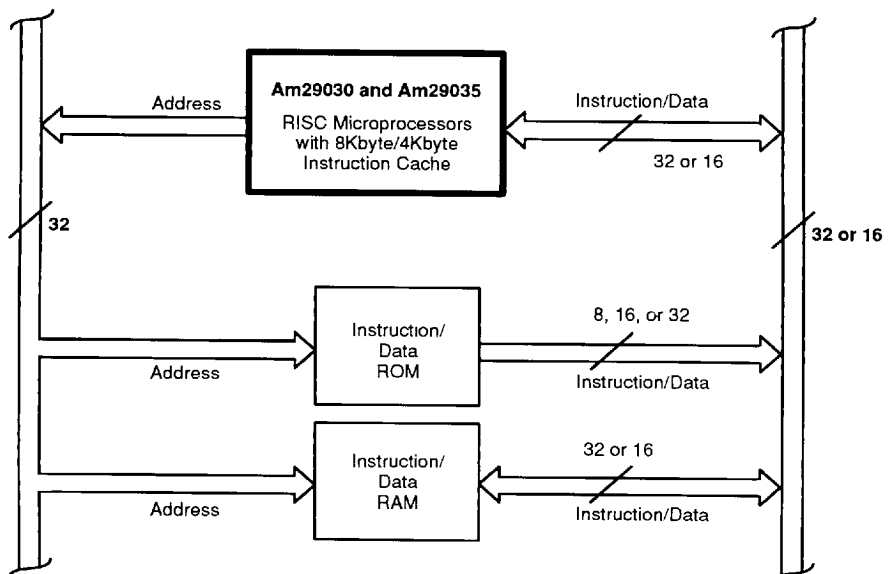
- Full 32-bit architecture
- 26 million instructions per second (MIPS) sustained at 33 MHz
- 8-Kbyte, two-way set-associative instruction cache
- 33- and 25-MHz operating frequencies
- Scalable Clocking™ technology
- Programmable 16- or 32-bit data bus width
- CMOS technology/TTL-compatible
- 4-Gbyte virtual address space with demand paging
- Streamlined system interface for simplified, high-frequency operation
- Burst-mode and page-mode access support
- 8-, 16-, or 32-bit ROM interface
- 64-entry Memory Management Unit on-chip
- Fully pipelined
- On-chip timer facility
- 192 general-purpose registers
- Three-address instruction architecture
- Master/slave chip/output checking
- Software compatible with Am29005™ and Am29000™ microprocessors
- Advanced debugging support
- IEEE Std. 1149.1–1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture implementation

Am29035 MICROPROCESSOR DISTINCTIVE CHARACTERISTICS

The Am29035 microprocessor is similar to the Am29030 microprocessor except for the following differences:

- 4-Kbyte, direct-mapped instruction cache
- 16-MHz operating frequency
- 12 million instructions per second (MIPS) sustained at 16 MHz

SIMPLIFIED BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am29030 and Am29035 RISC microprocessors are high-performance, general-purpose, 32-bit microprocessors implemented in CMOS technology. Through high circuit densities and a high degree of on-chip integration, the Am29030 and Am29035 microprocessors are capable of operating at high internal frequencies while providing the designer with a simple streamlined external interface.

The Am29030 and Am29035 microprocessors were designed to meet the common requirements of embedded applications such as laser beam printers, graphics processors, X terminals and servers, Application Program Interface (API) accelerators, and scanners. The Am29030 and Am29035 microprocessors are

well suited for these applications since they provide high performance at low cost, and offer the designer complete design flexibility. Coupled with hardware and software development tools from AMD® and AMD's Fusion29KSM partners, no design is ever far from the marketplace.

The Am29030 microprocessor is available in a 145-lead pin-grid-array (PGA) package and a 144-pin cerquad package. The PGA has 111 signal pins, 26 power and ground pins, 7 reserved pins, and 1 alignment/ground pin. The cerquad has 111 signal pins, 30 power and ground pins, and 3 reserved pins.

The Am29035 microprocessor is available in a 144-pin cerquad package.

29K™ Family Development Support Products

Contact your local AMD representative for information on the complete set of development support tools.

Software development products on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- EZ-030, an Am29030 microprocessor-based evaluation board kit

RELATED AMD PRODUCTS

29K Family Devices

Device	Description
Am29000™	Streamlined Instruction Microprocessor
Am29005™	Low-cost Streamlined Instruction Microprocessor
Am29050™	Streamlined Instruction Microprocessor with On-chip Floating Point
Am29200™	RISC Microcontroller
Am29205™	Low-cost RISC Microcontroller

Third-Party Development Support Products

The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs.

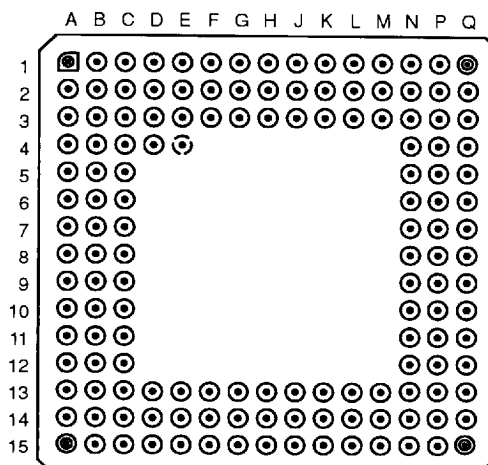
Products and solutions available through AMD's Fusion29K partners include:

- Silicon products
- Software generation and debug tools
- Hardware development tools
- Board level products
- Laser printer solutions
- Multiuser, kernel, and real-time operating systems
- Graphics solutions
- Networking and communications solutions
- Manufacturing support
- Custom support

CONNECTION DIAGRAM

145-Lead PGA

Bottom View



 Pin Number E-4 is defined for emulator access and is not a physical pin on the package (see the Am29030 and Am29035 Microprocessors User's Manual, order #15723, Signal Description section).

Note: Pinout observed from pin side of package (pins facing viewer).

PGA PIN DESIGNATION

(Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A-1	ID4	C-8	GND	H-14	MEMCLK	N-12	Vcc
A-2	ID0	C-9	Vcc	H-15	DIV2	N-13	A1
A-3	TRST	C-10	GND	J-1	ID21	N-14	ERLYA
A-4	TDI	C-11	Vcc	J-2	ID22	N-15	ERR
A-5	TCK	C-12	STAT1	J-3	GND	P-1	ID31
A-6	TEST	C-13	WBC	J-13	INCLK	P-2	A30
A-7	I/O	C-14	HIT	J-14	PWRCLK	P-3	A27
A-8	IO/MEM	C-15	INTR0	J-15	BREQ	P-4	A24
A-9	BWE0	D-1	ID12	K-1	ID23	P-5	A22
A-10	BWE2	D-2	ID11	K-2	ID24	P-6	A20
A-11	SUP/US	D-3	ID9	K-3	Vcc	P-7	A18
A-12	OPT0	D-4	GND	K-13	GND	P-8	A15
A-13	OPT2	D-13	DI	K-14	REQ	P-9	A13
A-14	MPGM1	D-14	INTR1	K-15	BURST	P-10	A10
A-15	STAT2	D-15	INTR2	L-1	ID25	P-11	A8
B-1	ID7	E-1	ID14	L-2	ID26	P-12	A6
B-2	ID6	E-2	ID13	L-3	Vcc	P-13	A4
B-3	ID3	E-3	GND	L-13	Vcc	P-14	A2
B-4	ID1	E-13	GND	L-14	BGRT	P-15	A0
B-5	TDO	E-14	INTR3	L-15	PGMODE	Q-1	A31
B-6	TMS	E-15	TRAP1	M-1	ID27	Q-2	A29
B-7	R/W	F-1	ID16	M-2	ID28	Q-3	A25
B-8	WARN	F-2	ID15	M-3	NC	Q-4	A23
B-9	BWE1	F-3	NC	M-13	GND	Q-5	A21
B-10	BWE3	F-13	Vcc	M-14	RDN	Q-6	A19
B-11	LOCK	F-14	RESET	M-15	RDY	Q-7	A17
B-12	OPT1	F-15	TRAP0	N-1	ID29	Q-8	A16
B-13	MPGM0	G-1	ID18	N-2	ID30	Q-9	A14
B-14	STAT0	G-2	ID17	N-3	NC	Q-10	A12
B-15	MSERR	G-3	Vcc	N-4	A28	Q-11	A11
C-1	ID10	G-13	Vcc	N-5	A26	Q-12	A9
C-2	ID8	G-14	CNTL0	N-6	GND	Q-13	A7
C-3	NC*	G-15	CNTL1	N-7	Vcc	Q-14	A5
C-4	ID5	H-1	ID20	N-8	GND	Q-15	A3
C-5	ID2	H-2	ID19	N-9	GND		
C-6	Vcc	H-3	GND	N-10	GND		
C-7	GND	H-13	GND	N-11	Vcc		

Notes:

- *1. NC = No connection internally.
2. Pin Number D-4 is the alignment/ground pin and must be electrically connected to ground.
3. Pin Number E-4 is defined for emulator access and is not a physical pin on the package (see Am29030 and Am29035 Microprocessors User's Manual, Signal Description section).

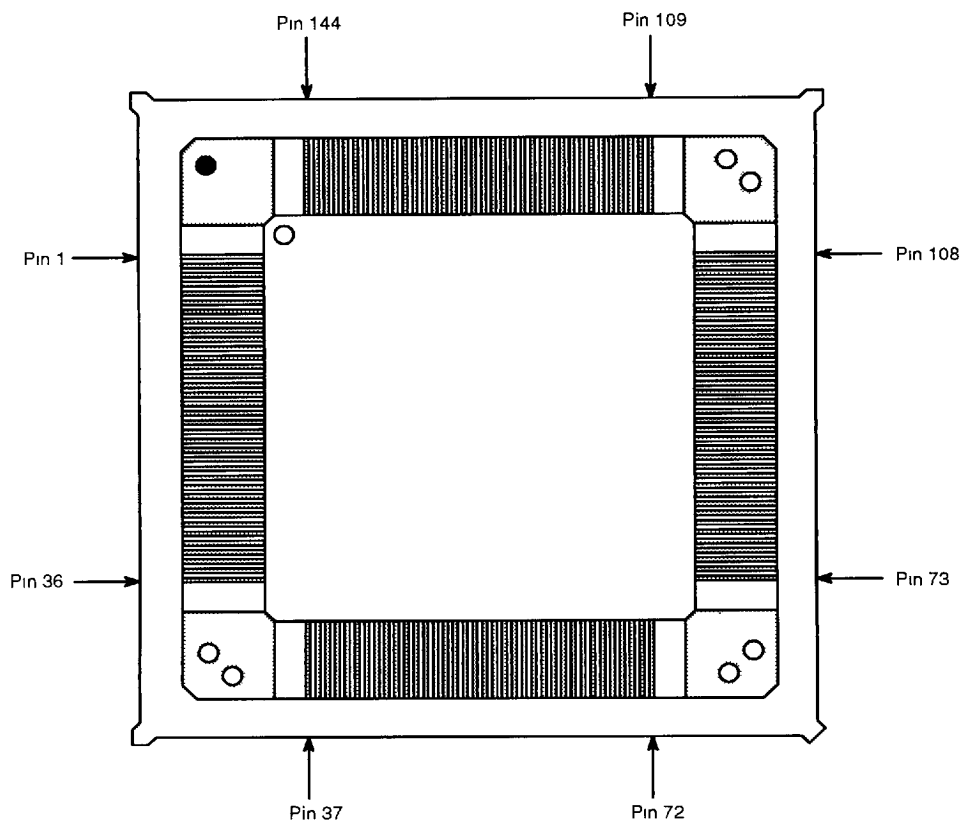
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
P-15	A0	B-10	BWE3	F-1	ID16	C-12	STAT1
N-13	A1	G-14	CNTL0	G-2	ID17	A-15	STAT2
P-14	A2	G-15	CNTL1	G-1	ID18	A-11	SUP/US
Q-15	A3	H-15	DIV2	H-2	ID19	A-5	TCK
P-13	A4	N-14	ERLYA	H-1	ID20	A-4	TDI
Q-14	A5	N-15	ERR	J-1	ID21	B-5	TDO
P-12	A6	C-7	GND	J-2	ID22	A-6	TEST
Q-13	A7	C-8	GND	K-1	ID23	B-6	TMS
P-11	A8	C-10	GND	K-2	ID24	F-15	TRAP0
Q-12	A9	D-4	GND	L-1	ID25	E-15	TRAP1
P-10	A10	E-3	GND	L-2	ID26	A-3	TRST
Q-11	A11	E-13	GND	M-1	ID27	C-6	Vcc
Q-10	A12	H-3	GND	M-2	ID28	C-9	Vcc
P-9	A13	H-13	GND	N-1	ID29	C-11	Vcc
Q-9	A14	J-3	GND	N-2	ID30	F-13	Vcc
P-8	A15	K-13	GND	P-1	ID31	G-3	Vcc
Q-8	A16	M-13	GND	J-13	INCLK	G-13	Vcc
Q-7	A17	N-6	GND	C-15	INTR0	K-3	Vcc
P-7	A18	N-8	GND	D-14	INTR1	L-3	Vcc
Q-6	A19	N-9	GND	D-15	INTR2	L-13	Vcc
P-6	A20	N-10	GND	E-14	INTR3	N-7	Vcc
Q-5	A21	A-7	I/D	A-8	IO/MEM	N-11	Vcc
P-5	A22	A-2	ID0	B-11	LOCK	N-12	Vcc
Q-4	A23	B-4	ID1	H-14	MEMCLK	B-8	WARN
P-4	A24	C-5	ID2	B-13	MPGM0		
Q-3	A25	B-3	ID3	A-14	MPGM1		
N-5	A26	A-1	ID4	B-15	MSERR		
P-3	A27	C-4	ID5	A-12	OPT0		
N-4	A28	B-2	ID6	B-12	OPT1		
Q-2	A29	B-1	ID7	A-13	OPT2		
P-2	A30	C-2	ID8	L-15	PGMODE		
Q-1	A31	D-3	ID9	J-14	PWRCLK		
L-14	BGRT	C-1	ID10	M-14	RDN		
J-15	BREQ	D-2	ID11	M-15	RDY		
K-15	BURST	D-1	ID12	F-14	RESET		
A-9	BWE0	E-2	ID13	K-14	REQ		
B-9	BWE1	E-1	ID14	B-7	R/W		
A10	BWE2	F-2	ID15	B-14	STAT0		
						RESERVED*	
						D-13	DI
						C-14	HIT
						C-13	WBC

- *1. These following signals are reserved for future processor implementations. To maintain compatibility with future processor implementations, these pins should be connected to V_{CC} by individual pull-up resistors.
2. Pin Number D-4 is the alignment/ground pin and must be electrically connected to ground.
3. Pin Number E-4 is defined for emulator access and is not a physical pin on the package (see Am29030 and Am29035 Microprocessors User's Manual, Signal Description section).

CONNECTION DIAGRAM

144-Lead Cerquad

Top View



CERQUAD PIN DESIGNATION**(Sorted by Pin No.)**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	37	V _{CC}	73	V _{CC}	109	A1
2	GND	38	GND	74	GND	110	A0
3	MSERR	39	ID5	75	A29	111	ERLYA
4	STAT2	40	ID6	76	A28	112	ERR
5	STAT1	41	ID7	77	A27	113	RDN
6	STAT0	42	ID8	78	A26	114	RDY
7	MPGM1	43	ID9	79	A25	115	BGRT
8	MPGM0	44	ID10	80	A24	116	GND
9	OPT2	45	ID11	81	A23	117	V _{CC}
10	OPT1	46	ID12	82	A22	118	PGMODE
11	OPT0	47	ID13	83	A21	119	BURST
12	LOCK	48	ID14	84	A20	120	REQ
13	SUP/US	49	ID15	85	A19	121	BREQ
14	BWE3	50	V _{CC}	86	A18	122	GND
15	BWE2	51	GND	87	A17	123	INCLK
16	BWE1	52	ID16	88	A16	124	V _{CC}
17	BWE0	53	ID17	89	V _{CC}	125	PWRCLK
18	V _{CC}	54	ID18	90	GND	126	MEMCLK
19	GND	55	ID19	91	V _{CC}	127	GND
20	WARN	56	ID20	92	GND	128	V _{CC}
21	IO/MEM	57	ID21	93	A15	129	GND
22	I/D	58	ID22	94	A14	130	DIV2
23	GND	59	ID23	95	A13	131	CNTL0
24	V _{CC}	60	GND	96	A12	132	CNTL1
25	R/W	61	V _{CC}	97	A11	133	V _{CC}
26	TEST	62	GND	98	A10	134	GND
27	TCK	63	ID24	99	A9	135	RESET
28	TMS	64	ID25	100	A8	136	TRAP0
29	TDI	65	ID26	101	A7	137	TRAP1
30	TDO	66	ID27	102	A6	138	INTR3
31	TRST	67	ID28	103	A5	139	INTR2
32	ID0	68	ID29	104	A4	140	INTR1
33	ID1	69	ID30	105	A3	141	INTR0
34	ID2	70	ID31	106	A2	142	DI
35	ID3	71	A31	107	GND	143	HIT
36	ID4	72	A30	108	V _{CC}	144	WBC

CERQUAD PIN DESIGNATION

(Sorted by Pin Name)

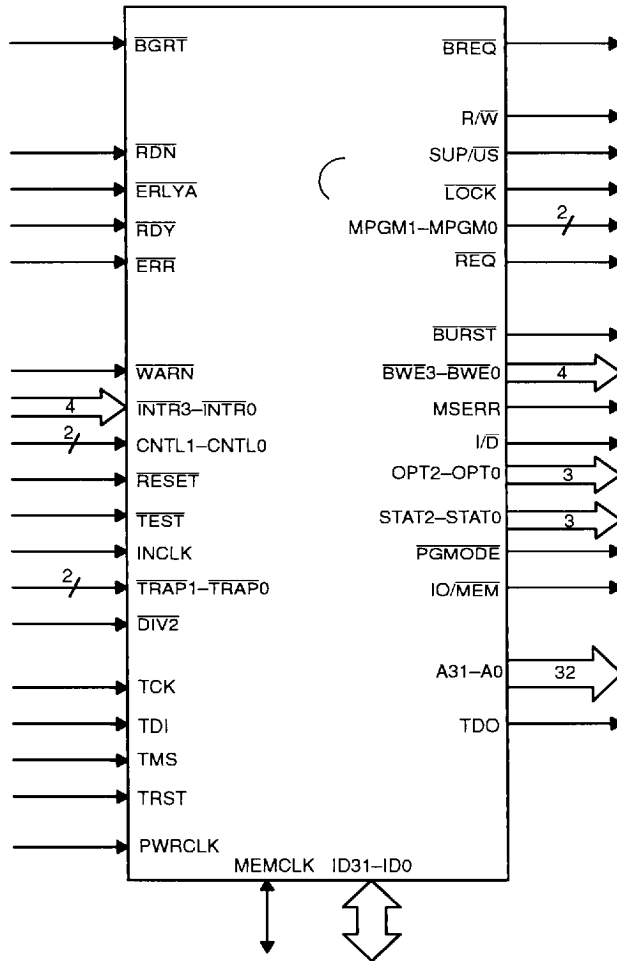
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
110	A0	16	BWE1	45	ID11	125	PWRCLK
109	A1	15	BWE2	46	ID12	113	RDN
106	A2	14	BWE3	47	ID13	114	RDY
105	A3	131	CNTL0	48	ID14	135	RESET
104	A4	132	CNTL1	49	ID15	120	REQ
103	A5	130	DIV2	52	ID16	25	R/W
102	A6	111	ERLYA	53	ID17	6	STAT0
101	A7	112	ERR	54	ID18	5	STAT1
100	A8	2	GND	55	ID19	4	STAT2
99	A9	19	GND	56	ID20	13	SUP/US
98	A10	23	GND	57	ID21	27	TCK
97	A11	38	GND	58	ID22	29	TDI
96	A12	51	GND	59	ID23	30	TDO
95	A13	60	GND	63	ID24	26	TEST
94	A14	62	GND	64	ID25	28	TMS
93	A15	74	GND	65	ID26	136	TRAP0
88	A16	90	GND	66	ID27	137	TRAP1
87	A17	92	GND	67	ID28	31	TRST
86	A18	107	GND	68	ID29	1	Vcc
85	A19	116	GND	69	ID30	18	Vcc
84	A20	122	GND	70	ID31	24	Vcc
83	A21	127	GND	123	INCLK	37	Vcc
82	A22	129	GND	141	INTR0	50	Vcc
81	A23	134	GND	140	INTR1	61	Vcc
80	A24	22	I/O	139	INTR2	73	Vcc
79	A25	32	ID0	138	INTR3	89	Vcc
78	A26	33	ID1	21	IO/MEM	91	Vcc
77	A27	34	ID2	12	LOCK	108	Vcc
76	A28	35	ID3	126	MEMCLK	117	Vcc
75	A29	36	ID4	8	MPGM0	124	Vcc
72	A30	39	ID5	7	MPGM1	128	Vcc
71	A31	40	ID6	3	MSERR	133	Vcc
115	BGR	41	ID7	11	OPT0	20	WARN
121	BREQ	42	ID8	10	OPT1		
119	BURST	43	ID9	9	OPT2		
17	BWE0	44	ID10	118	PGMODE		

Note: The following signals are reserved for future processor implementations:

Pin No.	Pin Name
142	DI
143	HIT
144	WBC

To maintain compatibility with future processor implementations, these pins should be connected to V_{CC} by individual pull-up resistors.

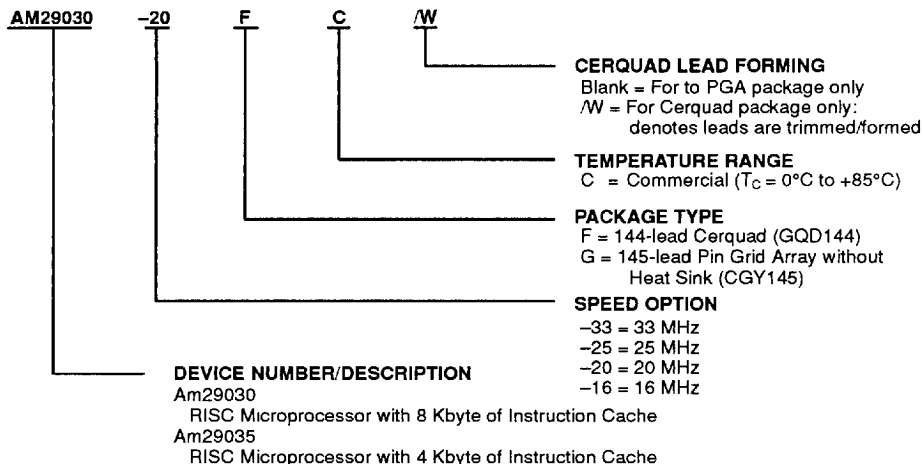
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29030-33 AM29030-25	GC
AM29030-20 AM29035-16	FC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Voltage on any Pin
 with Respect to GND -0.5 to $V_{\text{CC}} + 0.5$ V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Case Temperature (T_c) 0°C to $+85^{\circ}\text{C}$
 Supply Voltage (V_{CC}) $+4.75$ to $+5.25$ V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	$V_{\text{CC}} + 0.5$	V
V_{ILINCLK}	INCLK Input Low Voltage		-0.5	0.8	V
V_{IHINCLK}	INCLK Input High Voltage		2.0	$V_{\text{CC}} + 0.5$	V
V_{ILMEMCLK}	MEMCLK Input Low Voltage		-0.5	0.8	V
V_{IHMCLK}	MEMCLK Input High Voltage		$V_{\text{CC}} - 0.8$	$V_{\text{CC}} + 0.5$	V
V_{OL}	Output Low Voltage for All Outputs except MEMCLK	$I_{\text{OL}} = 3.2$ mA		0.45	V
V_{OH}	Output High Voltage for All Outputs except MEMCLK	$I_{\text{OH}} = -400$ μA	2.4		V
I_{LI}	Input Leakage Current	0.45 V $\leq V_{\text{IN}} \leq V_{\text{CC}} - 0.45$ V		± 10	μA
I_{LO}	Output Leakage Current	0.45 V $\leq V_{\text{OUT}} \leq V_{\text{CC}} - 0.4$ V		± 10	μA
I_{CCOP}	Operating Power Supply Current	$V_{\text{CC}} = 5.25$ V, Outputs Floating; Holding RESET active with externally supplied MEMCLK 16.7 MHz Cerquad 20 MHz Cerquad 25 MHz PGA 33.3 MHz PGA		30 30 28 27	mA/MHz
V_{OLC}	MEMCLK Output Low Voltage	$I_{\text{OLC}} = 20$ mA		0.6	V
V_{OHC}	MEMCLK Output High Voltage	$I_{\text{OHC}} = 20$ mA	$V_{\text{CC}} - 0.6$		V
I_{OSGND}	MEMCLK GND Short Circuit Current	$V_{\text{CC}} = 5.0$ V	100		mA
I_{OSVCC}	MEMCLK V_{CC} Short Circuit Current	$V_{\text{CC}} = 5.0$ V	100		mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
C_{IN}	Input Capacitance	$f_c = 10$ MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			20	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{\text{I/O}}$	I/O Pin Capacitance			20	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (PGA)

No.	Parameter Description	Test Conditions	Preliminary				Unit
			25 MHz		33 MHz		
			Min	Max	Min	Max	
1	INCLK Period (T)		40	100	30	100	ns
2	INCLK High Time		16	84	14.4	85.6	ns
3	INCLK Low Time		16	84	14.4	85.6	ns
4	INCLK Rise Time		0	6	0	6	ns
5	INCLK Fall Time		0	6	0	6	ns
6	MEMCLK Delay From INCLK	Notes 1, 2	0	6	0	6	ns
7	Synchronous Output Valid Delay for signals not broken out below	MEMCLK Output MEMCLK Input	1 2	13 17	1 2	13 17	ns
7a	Synchronous Output Valid Delay for ID31-ID0	MEMCLK Output MEMCLK Input	1 2	13 17	1 2	13 17	ns
7b	Synchronous Output Valid Delay for PGMODE	MEMCLK Output MEMCLK Input	1 2	13 19	1 2	13 19	ns
8	Synchronous Output Invalid Delay for signals not broken out below	MEMCLK Output MEMCLK Input	1 2	13 17	1 2	13 17	ns
8a	Synchronous Output Invalid Delay for ID31-ID0	MEMCLK Output MEMCLK Input	1 2	13 17	1 2	13 17	ns
8b	Synchronous Output Invalid Delay for PGMODE	MEMCLK Output MEMCLK Input	1 2	13 19	1 2	13 19	ns
9	Synchronous Input Setup Time for signals not broken out below (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	17 17 12		17 17 12		ns
9a	Synchronous Input Setup Time for ID31-ID0 (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	9 9 6		9 9 6		ns
9b	Synchronous Input Setup Time for ERR (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	11 11 7		11 11 7		ns
9c	Synchronous Input Setup Time for RDN (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	18 18 12		18 18 12		ns
10	Synchronous Input Hold Time	MEMCLK Output MEMCLK= INCLK	0 2		0 2		ns
11	Setup Time for Synchronous RESET Deassertion			2		2	ns
12	Hold Time for Synchronous RESET Deassertion			5		5	ns
13	WARN Pulse Width		4T		4T		ns
14	Asynchronous Input Pulse Width		T+10		T+10		ns
15	MEMCLK High Time	MEMCLK Period=T MEMCLK Period=2T	16 T-3	84 T+3	14.4 T-3	85.6 T+3	ns
16	MEMCLK Low Time	MEMCLK Period=T MEMCLK Period=2T	16 T-3	84 T+3	14.4 T-3	85.6 T+3	ns
17	MEMCLK Rise Time		0	5	0	5	ns
18	MEMCLK Fall Time		0	5	0	5	ns

Notes:

1. MEMCLK as an input is always CMOS level.
2. MEMCLK can drive an external load of 150 pF.
3. The input setup times with MEMCLK used as an input are improved if MEMCLK and INCLK are tied to the same clock input. This is possible only if the processor and bus operate at the same frequency.
4. Except where noted, measurement conditions are the same as the Am29000 microprocessor.
5. All output valid delays are measured with $V_{OL} = 1.5$ V and $V_{OH} = 1.5$ V.

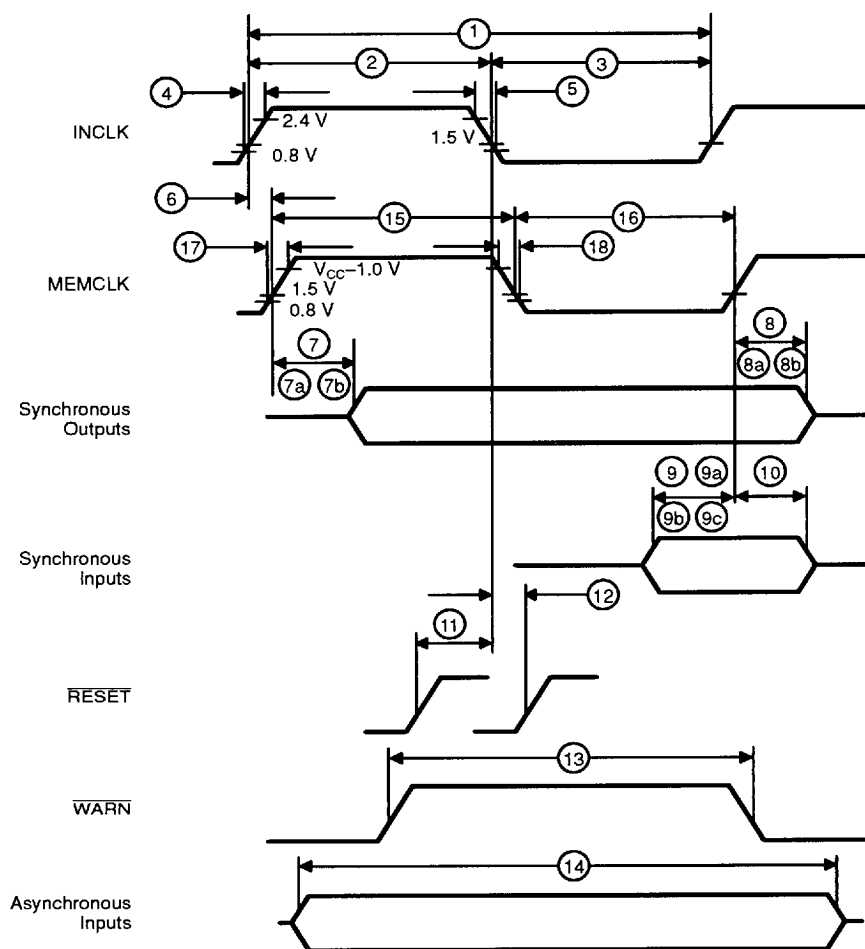
SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cerquad)

No.	Parameter Description	Test Conditions	Preliminary Information				Unit
			16 MHz		20 MHz		
			Min	Max	Min	Max	
1	INCLK Period (T)		60	100	50	100	ns
2	INCLK High Time		24	76	20	80	ns
3	INCLK Low Time		24	76	20	80	ns
4	INCLK Rise Time		0	6	0	6	ns
5	INCLK Fall Time		0	6	0	6	ns
6	MEMCLK Delay From INCLK	Notes 1, 2	0	6	0	6	ns
7	Synchronous Output Valid Delay for signal not broken out below	MEMCLK Output MEMCLK Input	1 2	20 24	1 2	18 22	ns
7a	Synchronous Output Valid Delay for ID31-ID0	MEMCLK Output MEMCLK Input	1 2	22 26	1 2	20 24	ns
7b	Synchronous Output Valid Delay for PGMODE	MEMCLK Output MEMCLK Input	1 2	22 26	1 2	20 24	ns
8	Synchronous Output Invalid Delay for signals not broken out below	MEMCLK Output MEMCLK Input	1 2	20 24	1 2	18 22	ns
8a	Synchronous Output Invalid Delay for ID31-ID0	MEMCLK Output MEMCLK Input	1 2	22 26	1 2	20 24	ns
8b	Synchronous Output Invalid Delay for PGMODE	MEMCLK Output MEMCLK Input	1 2	22 26	1 2	22 26	ns
9	Synchronous Input Setup Time for signals not broken out below (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	21 21 17		19 19 15		ns
9a	Synchronous Input Setup Time for ID31-ID0 (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	17 17 13		15 15 11		ns
9b	Synchronous Input Setup Time for ERR (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	17 17 13		15 15 11		ns
9c	Synchronous Input Setup Time for RDN (Note 3)	MEMCLK Output MEMCLK Input MEMCLK = INCLK	21 21 17		19 19 15		ns
10	Synchronous Input Hold Time	MEMCLK Output MEMCLK Input	2 3		2 3		ns
11	Setup Time for Synchronous RESET Deassertion			4		4	ns
12	Hold Time for Synchronous RESET Deassertion			7		7	ns
13	WARN Pulse Width		4T		4T		ns
14	Asynchronous Input Pulse Width		T+10		T+10		ns
15	MEMCLK High Time	MEMCLK Period=T MEMCLK Period=2T	24 T-3	76 T+3	20 T-3	80 T+3	ns
16	MEMCLK Low Time	MEMCLK Period=T MEMCLK Period=2T	24 T-3	76 T+3	20 T-3	80 T+3	ns
17	MEMCLK Rise Time		0	6	0	6	ns
18	MEMCLK Fall Time		0	6	0	6	ns

Notes:

1. MEMCLK as an input is always CMOS level.
2. MEMCLK can drive an external load of 150 pF.
3. The input setup times with MEMCLK used as an input are improved if MEMCLK and INCLK are tied to the same clock input. This is possible only if the processor and bus operate at the same frequency.
4. Except where noted, measurement conditions are the same as the Am29000 microprocessor.
5. All output valid delays are measured with $V_{OL} = 1.5\text{ V}$ and $V_{OH} = 1.5\text{ V}$.

SWITCHING WAVEFORMS

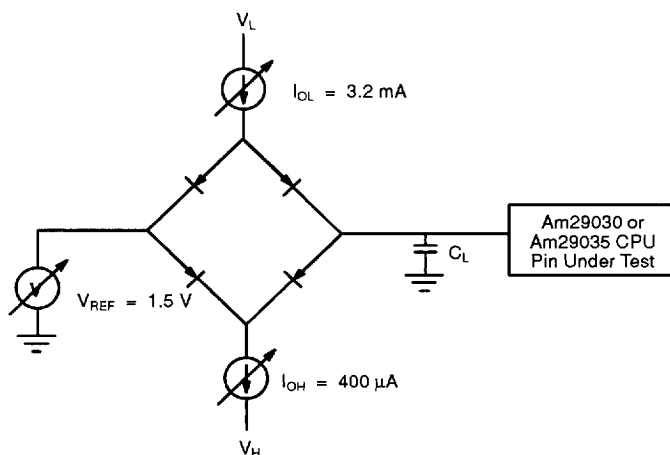


Capacitive Output Delays**For loads greater than 80 pF**

The following table describes the additional output delays for capacitive loads greater than 80 pF. Values in

the Maximum Additional Delay column should be added to the value listed in the Switching Characteristics table. For loads less than or equal to 80 pF, refer to the delays listed in the Switching Characteristics table. This table applies to the PGA package only.

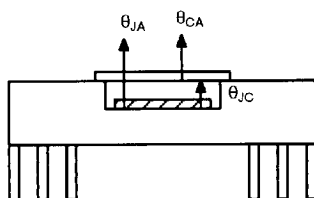
No.	Parameter Description	Preliminary	
		Total External Capacitance (pF)	Maximum Additional Delay (ns)
7	Synchronous MEMCLK Output Valid Delay	100 pF	+1 ns
		150 pF	+2 ns
		200 pF	+4 ns
		250 pF	+6 ns
		300 pF	+8 ns
7a	Synchronous MEMCLK Output Valid Delay for ID31-ID0	100 pF	+1 ns
		150 pF	+6 ns
		200 pF	+10 ns
		250 pF	+15 ns
		300 pF	+19 ns

SWITCHING TEST CIRCUIT

Note: C_L is guaranteed to 80 pF. For capacitive loading greater than 80 pF, refer to the Capacitive Output Delay table.

THERMAL CHARACTERISTICS

Pin-Grid-Array Package



$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Thermal Resistance – °C/Watt

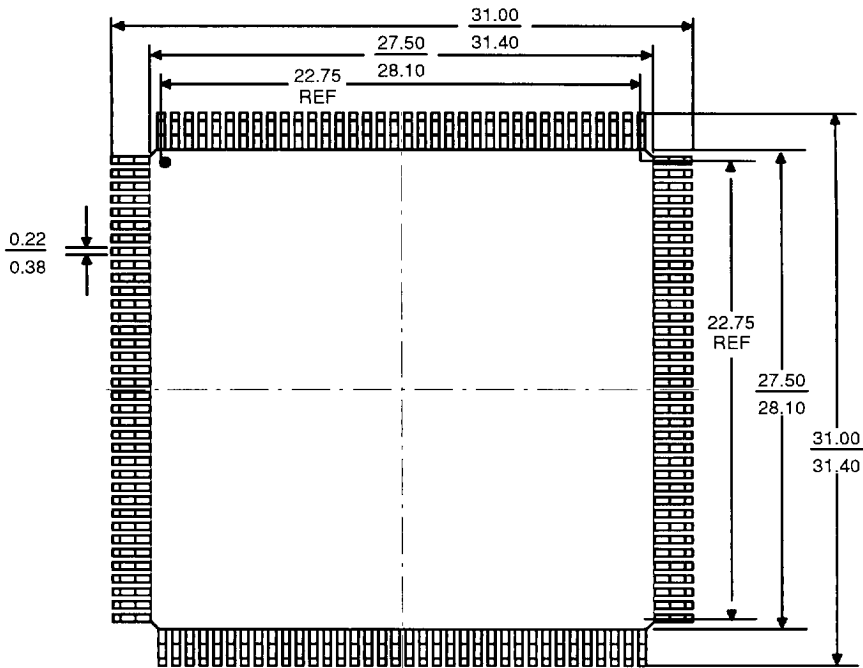
Pin-Grid-Array Package

		Airflow (LFPM)			
		0	150	300	500
θ_{JC}	Junction-to-Case	3	–	–	–
θ_{CA}	Case-to-Ambient	20	18	16	13

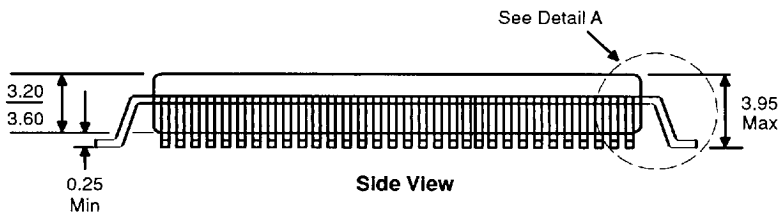
Cerquad Package

		Airflow (LFPM)			
		0	150	300	500
θ_{JC}	Junction-to-Case	7.5	–	–	–
θ_{CA}	Case-to-Ambient	20.8	18.7	16.4	13.3

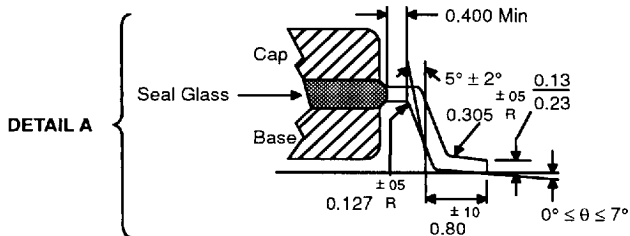
GQD 144 — Cerquad Trimmed and Formed (metric unit)



Top View

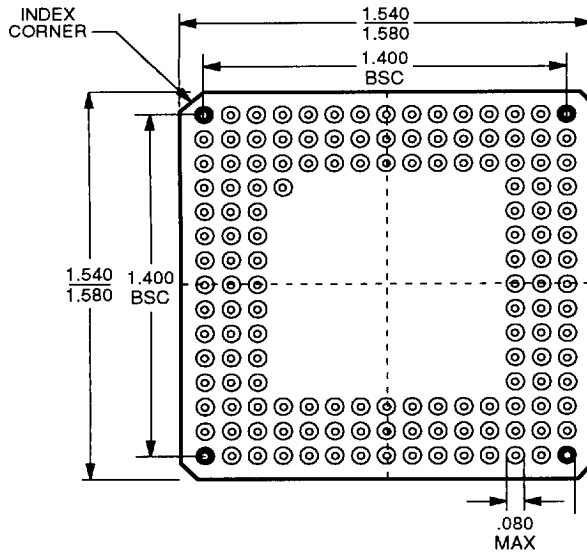


Side View

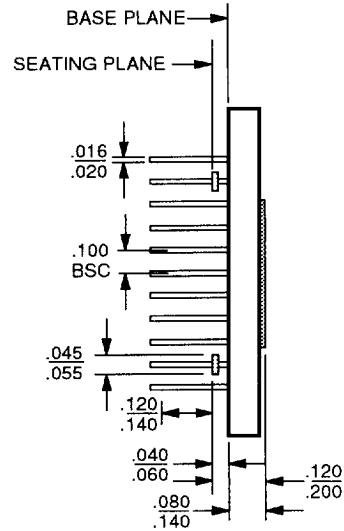


20000A
CK 64
08/03/93 MH

CGY 145 – Pin Grid Array (PGA)



BOTTOM VIEW



SIDE VIEW

17447A
8/02/93
CJ57 ae

Note: Bottom view observed from pin side of package (pins facing viewer).

Trademarks

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