GENERAL DESCRIPTION

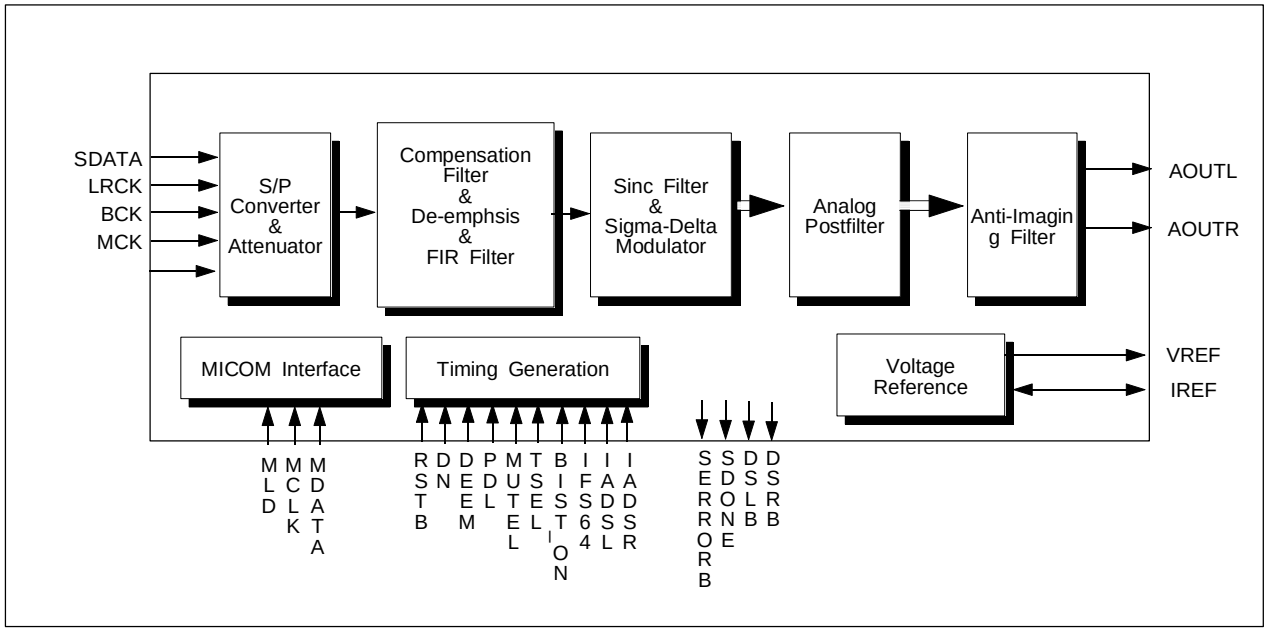
This product is ΣΔ Digital-To-Analog Converter for digital audio System (CDP). The product contains Serial-to-Parallel Converter and Compensation Filter, Digital Volume Attenuator by the MICOM Interface, De-Emphasis Filter, FIR filter, Sinc Filter, digital sigma-delta modulator, analog postfilter, AIF (Anti-Image-Filter). The normal input and output channels provides 95dB SNR (Signal to Noise Ratio) over in band (20kHz).

The product employs 1bit 4th-order sigma-delta architecture with 16bit resolution, over sampling of 64X. And analog postfilter with low clock sensitivity and linear phase, filters the shaping-nosie and outputs analog voltage with high resolution. An on-chip reference voltage is included to allow single supply operations.

FEATURES

- 16bit ΣΔ Digital-To-Analog Converter
- On-Chip Analog Postfilter
- Filtered Line-Level Outputs, Linear Phase Filtering
- On-Chip Voltage Reference
- 95dB SNR
- Sampling Rate 44.1kHz
- Input Rate 1Fs or 2Fs by Normal Mode/ Double Mode Selection
- Zero Input Detection Mute
- On-Chip Compensation Filter
- Input Volume Attenuator by the MICOM Interface
- On-Chip De-Emphasis Filter
- On-Chip 4 times oversampling Digital Filter
- Single 5V Power Supply
- Low Clock Jitter Sensitivity

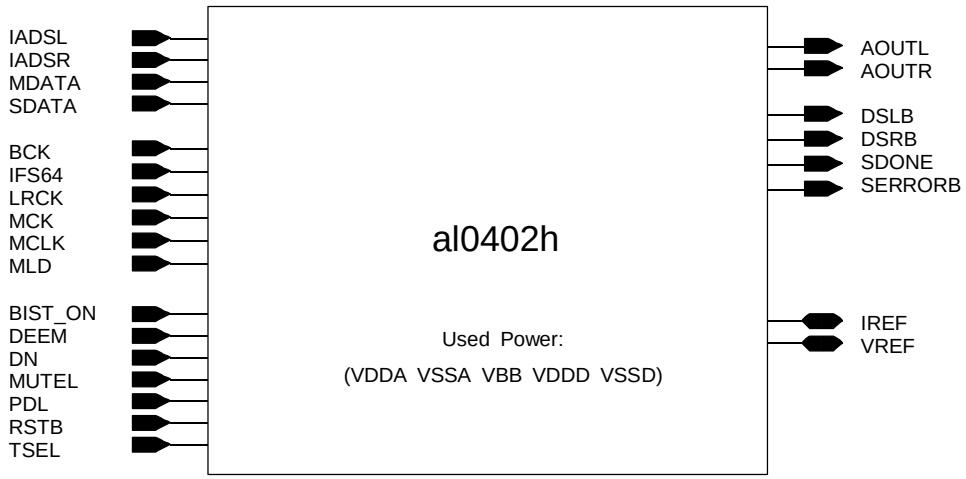
BLOCK DIAGRAM



CORE PIN DESCRIPTION

SYMBOL	I/O TYPE	I/O PAD	DESCRIPTION
IADSL	DI	picc_bb	1bit Input for Analog Postfilter of L-CH (When TSEL=H,used)
IADSR	DI	picc_bb	1bit Input for Analog Postfilter of R-CH (When TSEL=H, used)
MDATA	DI	picc_bb	Micon Interface Command Data Input
SDATA	DI	picc_bb	Serial Digital Input
BCK	DI	picc_bb	Bit Clock Input
IFS64	DI	picc_bb	64X Sampling Clock Input for Analog Postfilter (When TSEL=H, used)
LRCK	DI	picc_bb	Sample Rate Clock Input
MCK	DI	picc_bb	Master Clock Input
MCLK	DI	picc_bb	Micom Interface Clock Input
MLD	DI	picc_bb	Micom Interface Command load Input(When low,load)
BIST_ON	DI	picc_bb	Memory Bist Test Mode. "H" enabled
DEEM	DI	picc_bb	De-Emphasis On/Off. "H" is enabled. "L" is disabled.
DN	DI	picc_bb	Input Rate Select. High is Double(2Fs) Mode, Low is Normal(1Fs) Mode.
MUTEL	DI	picc_bb	Analog Output Mute. "L" enabled
PDL	DI	picc_bb	Power Down. "L" enabled
RSTB	DI	picc_bb	Reset Input. "L" Enabled
TSEL	DI	picc_bb	Test pin for Analog Postfilter Input Selection
AOUTL	AO	poa_bb	Analog Output for L-CH
AOUTR	AO	poa_bb	Analog Output for R-CH
DSLB	DO	pot2_bb	L-CH 1bit Output for Digital sigma-delta Modulator.
DSRB	DO	pot2_bb	R-CH 1bit Output for Digital sigma-delta Modulator.
SDONE	DO	pot2_bb	Test Output pin for embeded memory BIST (BIST_ON="H") or Digital Block test (BIST_ON="L")
SERRORB	DO	pot2_bb	Test Output Pin for Embeded memory BIST (BIST_ON="H") or Digital Block test (BIST_ON="L")
IREF	AB	poa_bb	Test Pin for Analog Supply Current
VREF	AB	poa_bb	Reference Voltage Output for Bypass

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Values	Unit
Supply Voltage	VDDD VDDA	-0.3 TO 7.0	V
Voltage on any Digital Voltage	Vin	VSSD-0.3 to VDDD+0.3	V
Storage Temperature Range	Tstg	-45 to 150	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to Ground unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Charateristics	SYMBOL	MIN	TYP	MAX	UNI
Supply Voltage	VDDD VDDA	4.75	5.0	5.25	V
Operating Temp.	Topr	0	25	70	°C

ELECTRICAL CHARACTERISTICS

(VDD=5V, Temp=25°C, Fs=44.1kHz, Signal Frequency=20~20kHz)

PARAMETER	MIN	TYP	MAX	UNITS
Resolution		16		bits
SNR<1>	90	95		dB
THD<2>	0.007	0.004		%
SND<3>	82	87		dB
Dynamic Range<4>	85	90		dB
Reference Voltage Ouput		2.25		V
Frequency Responce		±0.1	±0.5	dB
Analog Output				
Voltage Range		±1.414		V
Load Impedance	5k			Ω
Digital Filter				
Pass Band Ripple		±0.0072		dB
Stop Band Attenuation		62.7		dB
Pass Band		0.45		Fs
Power Supply				
Analog Current		25		mA
Digital Current		20		mA
Power Dissipation		225		mW
Power Down Current			1	mA

<1> 1kHz 0dB Sinewave Input, EIAJ

<2> 1kHz 0dB Sinewave Input

<3> 1kHz 0dB Sinewave Input, (Not EIAJ)

Measured by Teledyne A585 System (using 30kHz LPF)

<4> 1kHz -60dB Sinewve Input, and then measured data + 60dB

AC TIMING CHARACTERISTICS

(VDDD=5V, VSSD=0V,Temp=25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
MCK Frequency	Fmck	-	16.9344	-	MHz
BCK Frequency (Normal/Doube Mode)	Fbck		1.4112 / 2.8224	-	MHz
MCK Rising and LRCK Edge Dealay	Tmld	0	-	-	ns
MCK Risng and LRCK Edge Setup Time	Tmlst	10	-	-	ns
BCK Rising and LRCK Edge Dealay	Tbld	0	-	-	ns
BCK Risng and LRCK Edge Setup Time	Tblst	10	-	-	ns
SDATA and BCK Rising Setup Time	Tsbst	10	-	-	ns
BCK Ring and SDATA Hold Time	Tbsht	10	-	-	ns

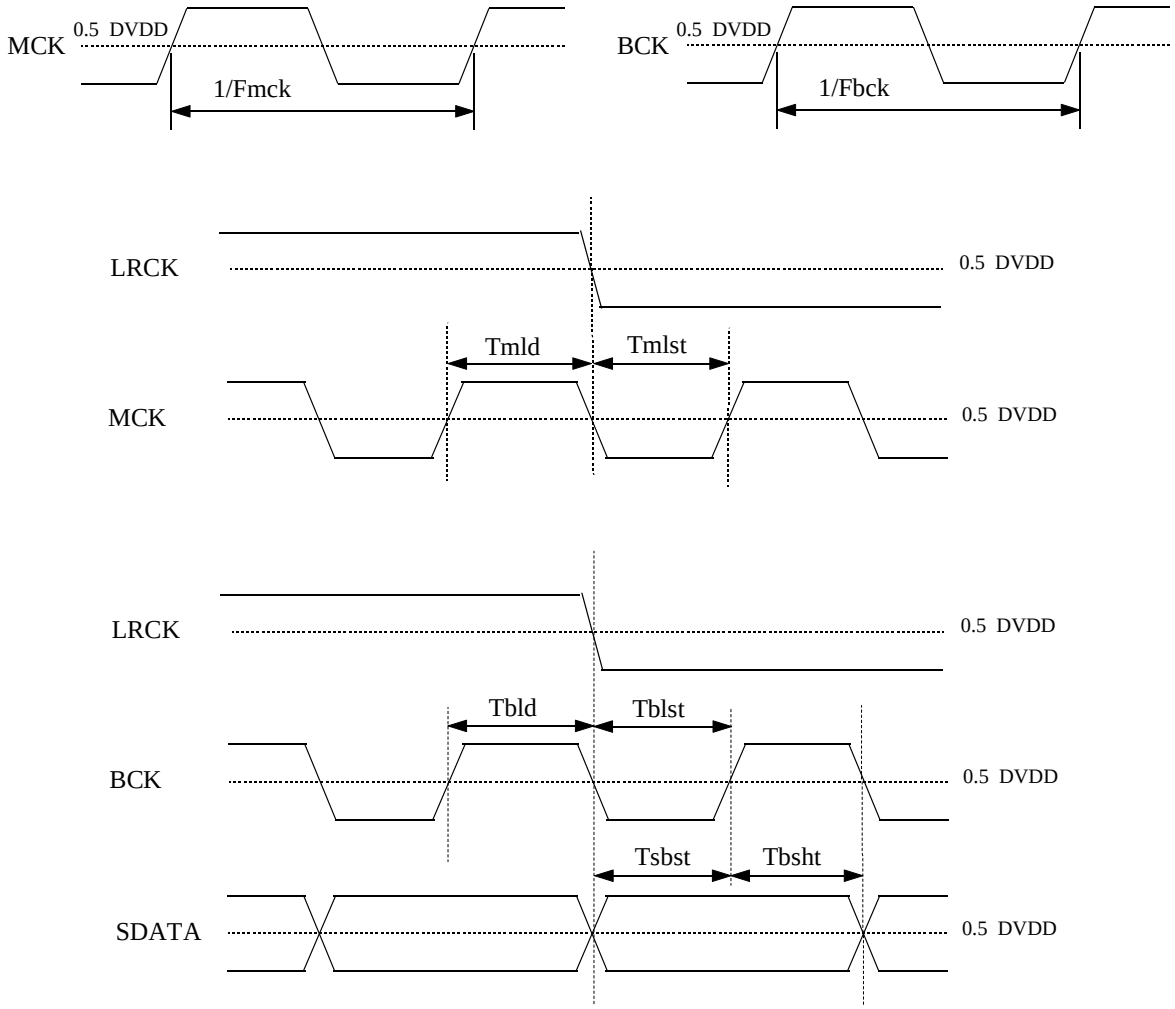


Fig1. Timing Diagram

TIMING DIAGRAM (Fs=44.1KHz)

Clock Input and Serial Input Data Inform

If DN(Double Mode/Normal Mode) pin is Low state, that is Normal Mode. And BCK, LRCK is following,

MCK=384*Fs=16.9344MHz

BCK=32*Fs=1.4112MHz

LRCK=1*Fs=44.1kHz

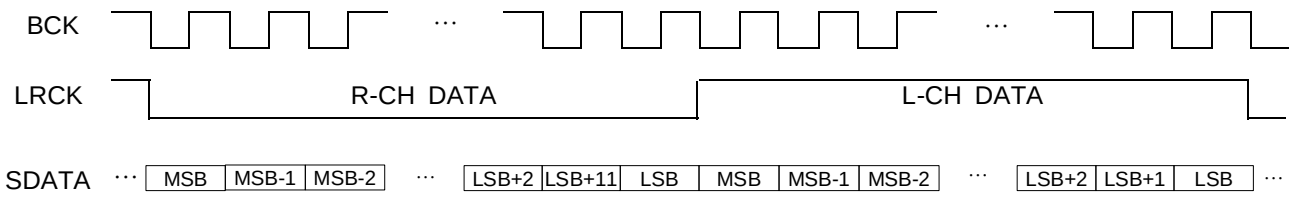
If DN pin is High state, that is Double mode. And BCK, LRCK is following,

MCK=384*Fs=16.9344MHz

BCK=64*Fs=2.8224MHz

LRCK=2*Fs=88.2kHz

SDATA is MSB fisrt at falling edge triggered of BCK



FUNCTIONAL DESCRIPTION

Fig2 is the 1bit 4th-order sigma-delta DAC block daigram. S/P Converter converts serial 16bit input data to parallel 16bit data. Digital input data is attenuated by MICOM interface pin control. Compensation Filter compensates gain droop in Passband by Sinc Filter and Sigma-Dellta Modulator Signal Transfer Function. De-emphasis Block de-emphasizes pre-emphasised input data to emphssize high frequency in audible band. FIR Filter perfroms 4X interpolation. And it outputs 4Fs(DN='Low') rate data or 8Fs(DN='High') rate data by variabled input data rate. It also removes the images of the input signal that are present at multiples of the input sample frequency. And Sinc filter makes the constant 64Fs rate data by 16 times or 8 times upsampling FIR Filter output data according to DN(Double/Normal Mode) Pin Selection. This operation intorduces a sinc function responce on the resulting frequency spectrum, which greatly attenuates the energy of images at the multifules of 4Fs(or 8Fs).

Digital sigma-delta modulator of bit-stream type has the IFL (Inversse-Follower-Leader) topology, and it performs a noise-shaping function. The modulator shapes the quantization noise by suppressing its in-band component and pushes the noise energy of outside the band-of-interest without deteriorating the audio input signal. The 64 times oversampled 1-bit PDM output from the modulator the drives a analog postfilter.

The analog postfilter comprises SC-postfilter, anti-imaging filter. The SC-postfilter removes the quantization noise shaped to out-of-band by digital sigma-delta modulator. This Analog filter has the good clock jitter characteristc and very linear characteristic. And following the CTF (continuous time filter) removes the sampling images and makes the high resolution analog output.

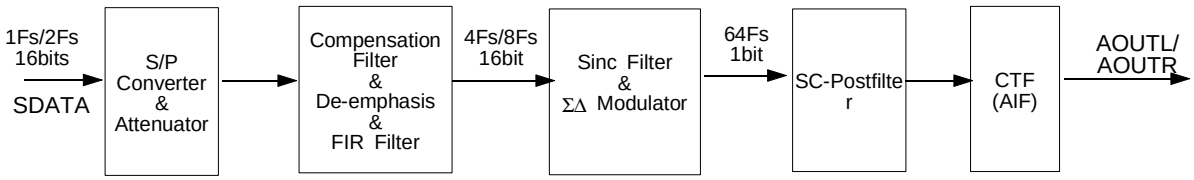


Fig2. 1bit sigma-delta dac block diagram

MICOM Interface

This product can do the function of digital attenuation whenever it receives thd MDATA, MLD, MCLK signals form the MICOM.

Digital Attenuation

When the 14-bit serial data is applied to the MDATA, MCLK, MLD in the form of Fig3, according to the data digital attenuation is accomplished. The lower eight LSBs should be 5D(LSB First Format-Hex) and according to the upper 6 bits(LSB First Format-Bin) the attenuation level can be adjusted. (see Table1)

When RSTB is low state the latch circuitry for setting the attenuation level becomes reset and the attenuation level is 0dB. At this instance, because the digital filter circuit gets to stop operation the act of attenuation is impossible. In addition, whenever MDATA is not carried, MCLK must be 'HIGH' state. In case of no attenuation fuction needed, MDATA should be 'L', MCLK and MLD should be 'H.

CORE EVALUATION GUIDE

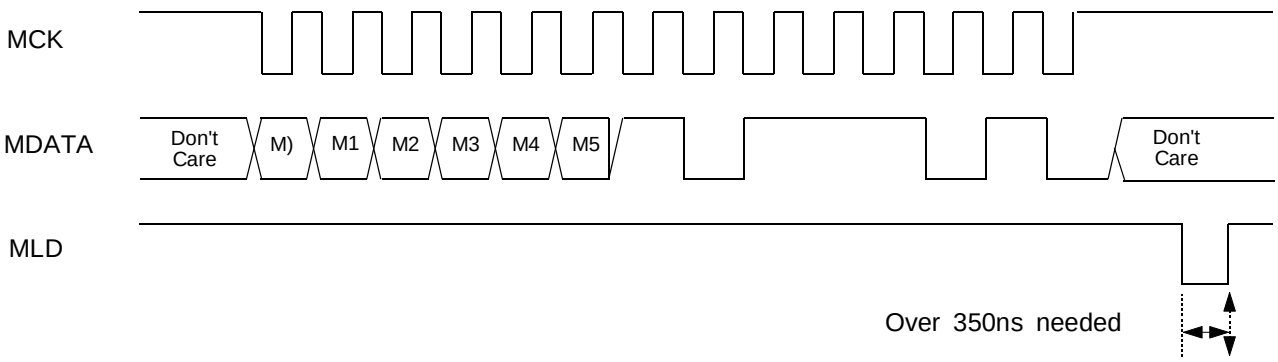
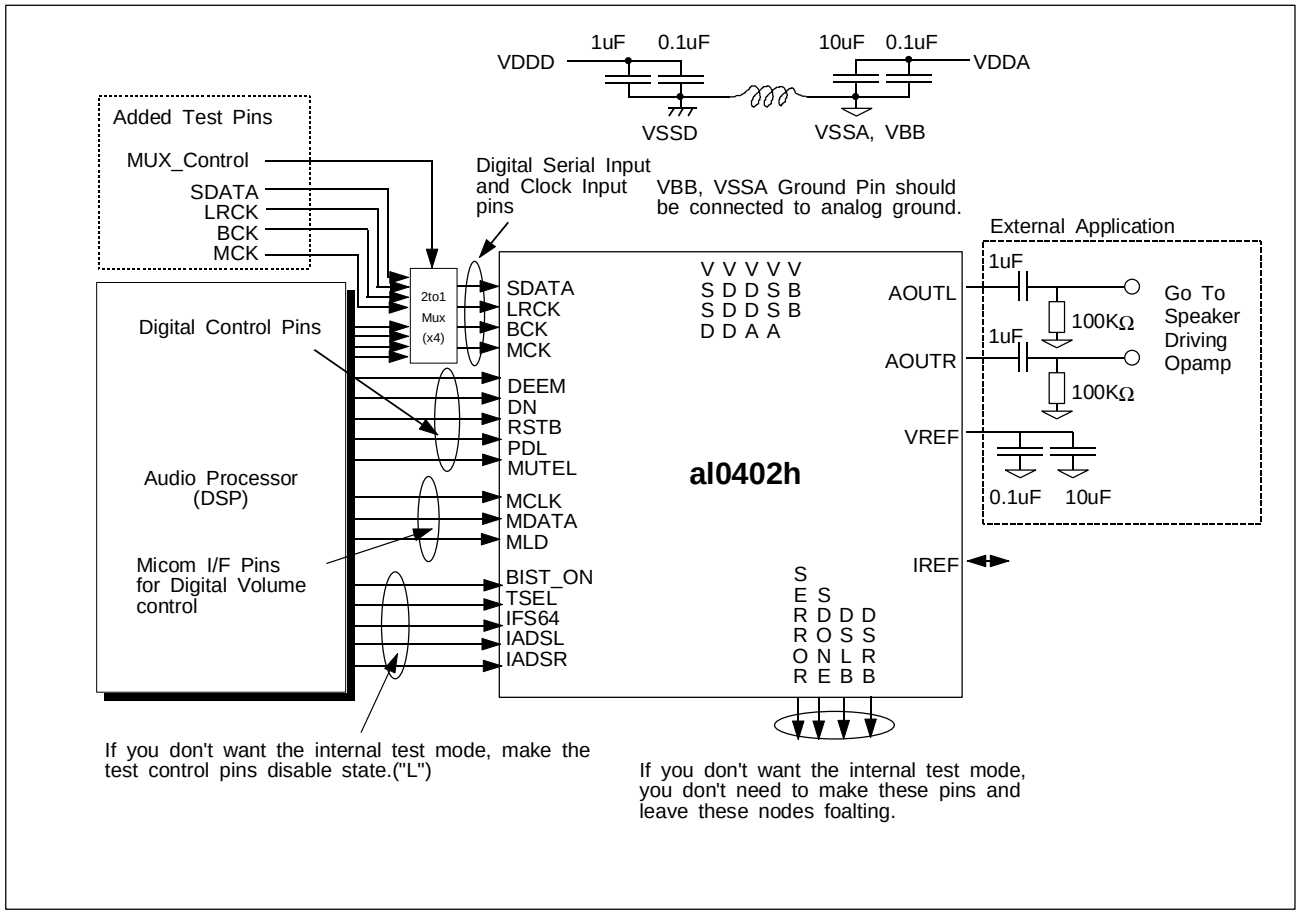


Fig3. MICOM Interface Timing Chart

MDATA									Attenuation Level (dB)	MDATA									Attenuation Level (dB)
MSB								LSB		MSB								LSB	
		M5	M4	M3	M2	M1	M0					M5	M4	M3	M2	M1	M0		
5	D	0	0	0	0	0	0		0	5	D	1	0	0	0	0	0		-6.30
5	D	0	0	0	0	0	1		-0.28	5	D	1	0	0	0	0	1		-6.58
5	D	0	0	0	0	1	0		-0.42	5	D	1	0	0	0	1	0		-6.88
5	D	0	0	0	0	1	1		-0.56	5	D	1	0	0	0	1	1		-7.18
5	D	0	0	0	1	0	0		-0.71	5	D	1	0	0	1	0	0		-7.50
5	D	0	0	0	1	0	1		-0.86	5	D	1	0	0	1	0	1		-7.82
5	D	0	0	0	1	1	0		-1.01	5	D	1	0	0	1	1	0		-8.16
5	D	0	0	0	1	1	1		-1.16	5	D	1	0	0	1	1	1		-8.52
5	D	0	0	1	0	0	0		-1.32	5	D	1	0	1	0	0	0		-8.89
5	D	0	0	1	0	0	1		-1.48	5	D	1	0	1	0	0	1		-9.28
5	D	0	0	1	0	1	0		-1.64	5	D	1	0	1	0	1	0		-9.68
5	D	0	0	1	0	1	1		-1.80	5	D	1	0	1	0	1	1		-10.10
5	D	0	0	1	1	0	0		-1.97	5	D	1	0	1	1	0	0		-10.55
5	D	0	0	1	1	0	1		-2.14	5	D	1	0	1	1	0	1		-11.02
5	D	0	0	1	1	1	0		-2.32	5	D	1	0	1	1	1	0		-11.51
5	D	0	0	1	1	1	1		-2.50	5	D	1	0	1	1	1	1		-12.04
5	D	0	1	0	0	0	0		-2.68	5	D	1	1	0	0	0	0		-12.60
5	D	0	1	0	0	0	1		-2.87	5	D	1	1	0	0	0	1		-13.20
5	D	0	1	0	0	1	0		-3.06	5	D	1	1	0	0	1	0		-13.84
5	D	0	1	0	0	1	1		-3.25	5	D	1	1	0	0	1	1		-14.54
5	D	0	1	0	1	0	0		-3.45	5	D	1	1	0	1	0	0		-15.30
5	D	0	1	0	1	0	1		-3.66	5	D	1	1	0	1	0	1		-16.12
5	D	0	1	0	1	1	0		-3.87	5	D	1	1	0	1	1	0		-17.04
5	D	0	1	0	1	1	1		-4.08	5	D	1	1	0	1	1	1		-18.06
5	D	0	1	1	0	0	0		-4.30	5	D	1	1	1	0	0	0		-19.22
5	D	0	1	1	0	0	1		-4.53	5	D	1	1	1	0	0	1		-20.56
5	D	0	1	1	0	1	0		-4.76	5	D	1	1	1	0	1	0		-22.14
5	D	0	1	1	0	1	1		-5.00	5	D	1	1	1	0	1	1		-24.08
5	D	0	1	1	1	0	0		-5.24	5	D	1	1	1	1	0	0		-26.58
5	D	0	1	1	1	0	1		-5.49	5	D	1	1	1	1	0	1		-30.10
5	D	0	1	1	1	1	0		-5.75	5	D	1	1	1	1	1	0		-36.12
5	D	0	1	1	1	1	1		-6.02	5	D	1	1	1	1	1	1		-∞

Table1. Digital Attenuation Level



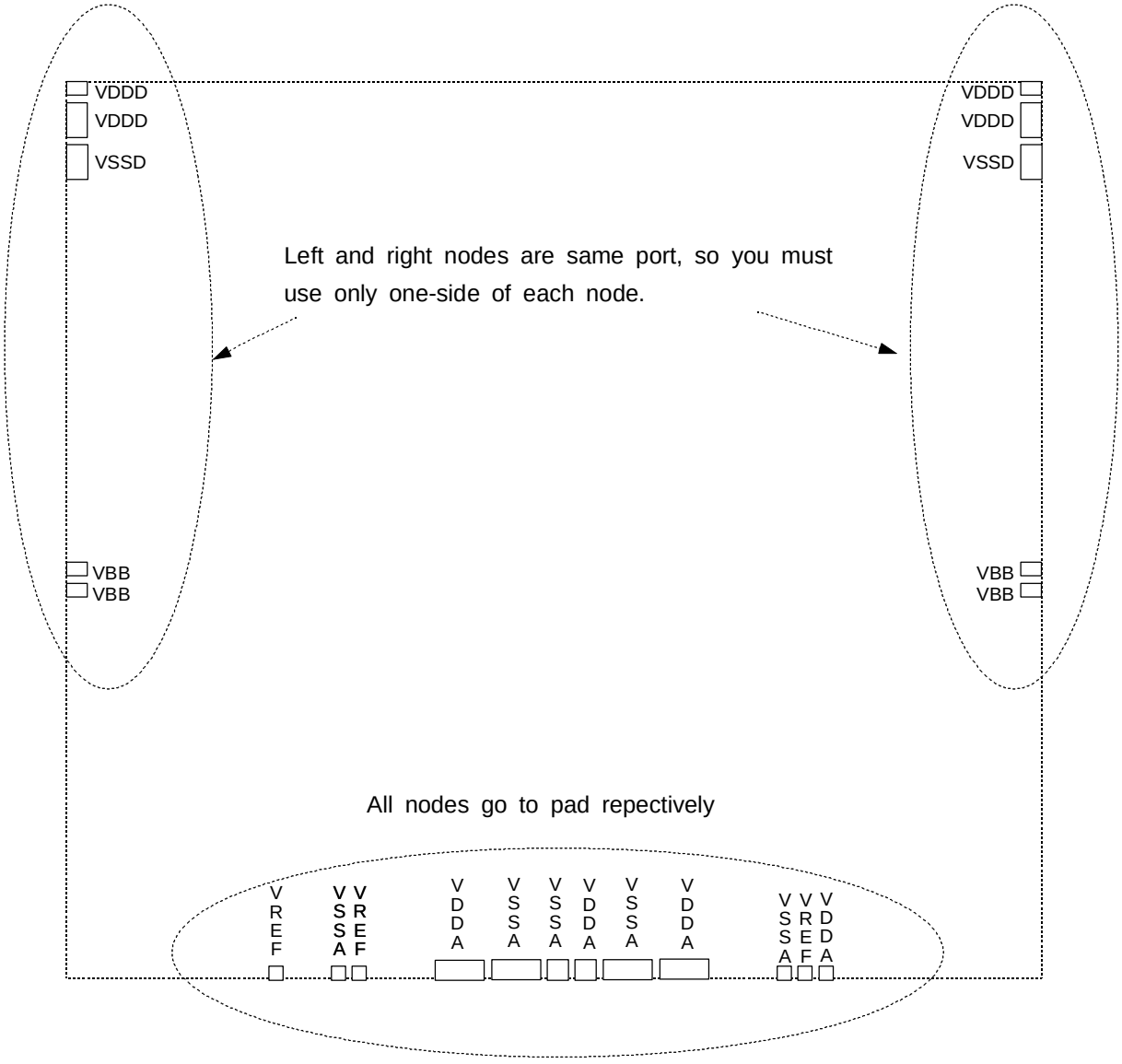
- If you will test only analog core(al0402h), just add the 4 pins to supply digital inputs(LRCK, BCK, SDATA, MUX_control)
- Digital serial input and clock input pins refer to timming diagram.
- Digital Control Pins inform refer to PIN Description.
- Analog powers(VDDA,VSSA,VBB) and digital powers(VDDD,VSSD) should be seperated.
- VBB pin should be connected to analog ground.
- For Internal block test pins, if you don't need this mode, you make these pins to disable state('L') and output pins floating.
- This analog Core modeling (by Verilog) is provided.

APPLICATION GUIDE

- Locate bypass capacitors(0.1uF, 1uF, 10uF in pins VDDA, VDDD, Vref) as close as to Analog Core
- Vref line make short and thick
- Analog and digital ground plane must be seperlated, and just connected by ferrite bead in one path.

CORE LAYOUT GUIDE

- VDDA, VSSA is the analog power of this core, and recomand that you should make pad for only this power.
- VBB(Bulk Bias) should be connected to VSSA pad (not internal VSSA line), or you should make pad for VBB and exteranlly connect to VSSA in board.
- VREF is analog reference pin, all VREF pin should be respectively connected to PAD for VREF (do not internally merge and then go to pad for VREF)
- VSSA is analog ground pin, all VSSA pins should be respectively connected to PAD for VSSA.
- VDDA is analog supply pin, all VDDA pins should be respectively connected to PAD for VDDA.
- AOUTL, AOUTR is analog output pins, should be connected to pad by way of thick and short.



FEEDBACK REQUEST

Sigma-Delta DAC Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
supply voltage				V	
Max master clock frequency				Hz	
Operating temperature				°C	
Sampling Frequency				Hz	
Dynamic range				dB	
Total harmonic distortion				dB	
Signal-to-noise ratio				dB	
Input format resolution (Serial/Parallel interface)				Bit	
Channel		Mono		Stereo	
Power dissipation				mW	
Full scale output voltage range				Vpp	
group delay				sec	
Phase linearity deviation for passband region				- (Deg)	
Peak-to-peak frequency response ripple for passband region				dB	

- Could you explain external/internal pin configurations as required?

Specially requested function list :