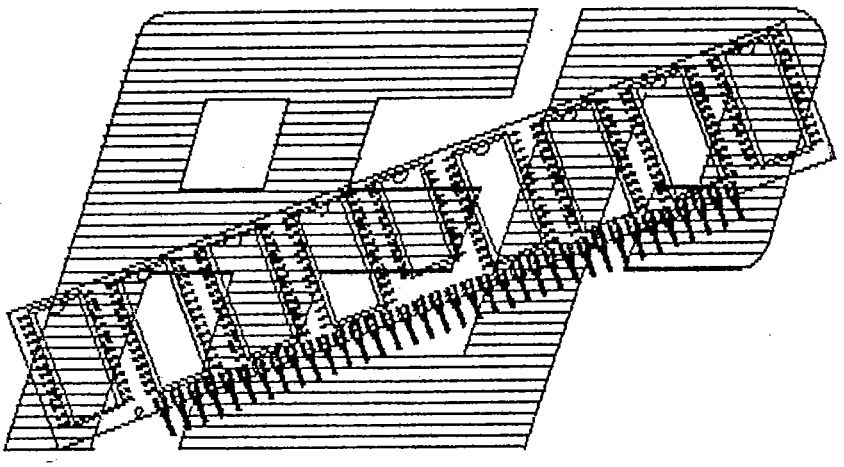
T-46-23-14

- >> 131,072 x 8 Organization
- >> Access speeds as fast as 40ns in High Speed version
- >> Double sided to maximize bit density
- >> On board 1-of-16 Decoder
- >> Completely Static operation
- >> TTL compatible
- >> Low power, battery back-up operation capability
- >> Uses single +5V power supply



128 KILOBYTE STATIC RAM MODULE

DESCRIPTION:

The AEPSx128K8 is a high density 128 Kilo-word by 8 bit static random access memory module in a 36 pin single-inline-package format. Physically it consists of an FR4 PC material substrate mounted with sixteen 8K x 8 SOP (small outline package) ICs, the 1-of-16 decoder, four 0.1 microfarad decoupling capacitors, and 36 edge-clip I/O pins.

The module can use any of the 8K x 8 SRAMs made by any of a large number of manufacturers in both Mix-MOS and CMOS technologies. A wide range of access speeds are available. The decoder normally used on standard speed modules is the 74HCT154 with the fully CMOS version 74HC154 also available for low power applications. High speed modules get the 74F154.

Performance specifications and electrical characteristics are determined by the IC devices used. These items vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors data sheets which are included here or from data books.

Mechanical dimensions are 0.88 in. high by 4.79 in. long by 0.28 in. wide. The module is available with either vertical or 90 degree (horizontal) lead pins. The latter allows the module to be mounted on its side which gives a low 0.315 stand-off height.

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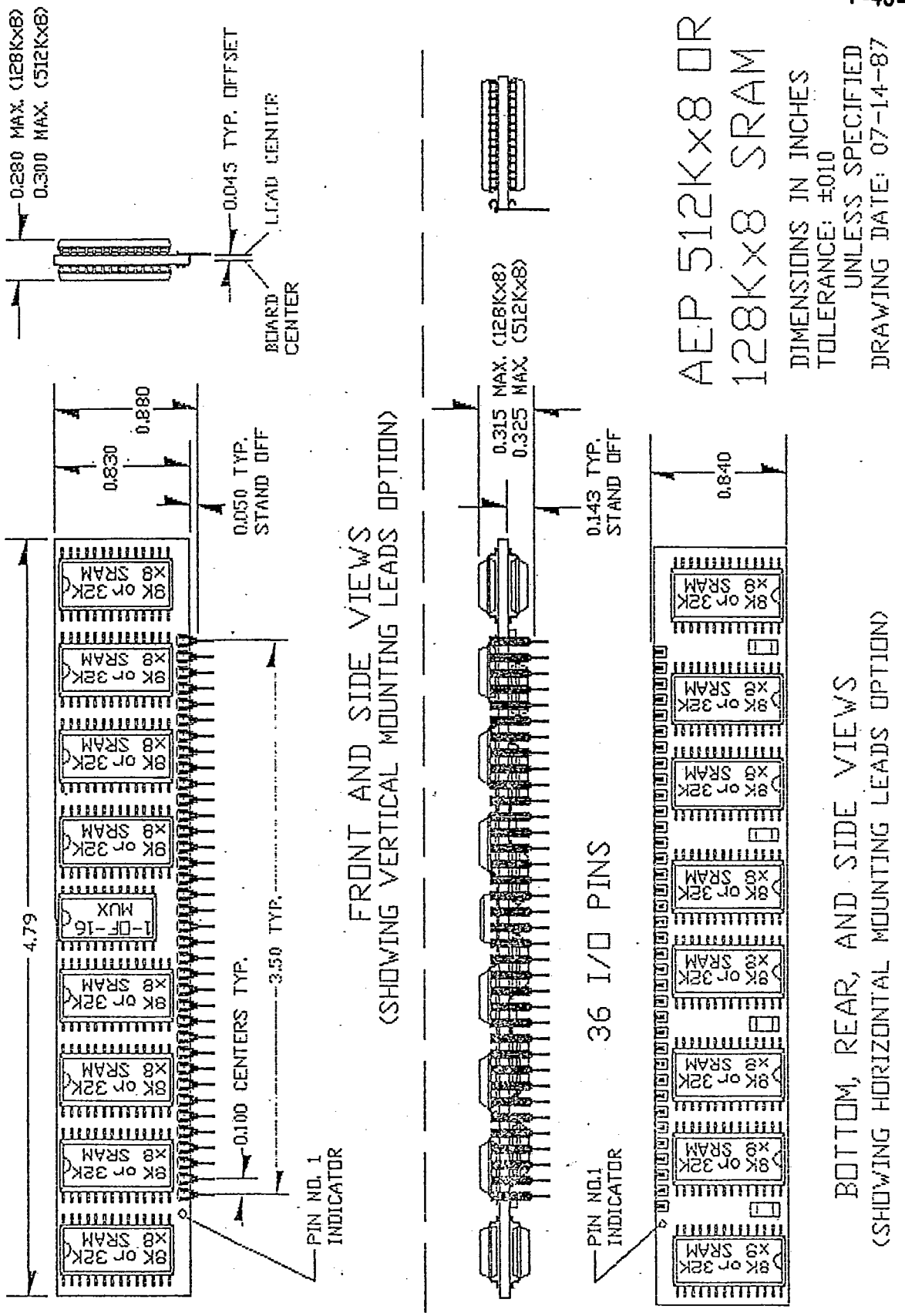

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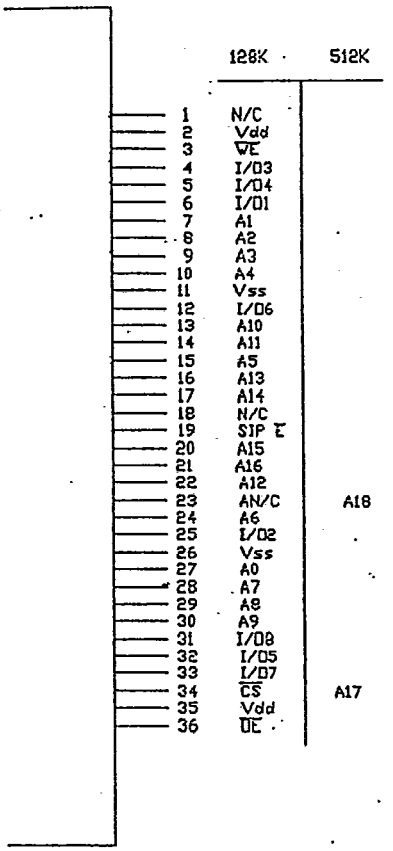
PIN CONFIGURATION
128/512K x 8 SRAM WITH DECODER

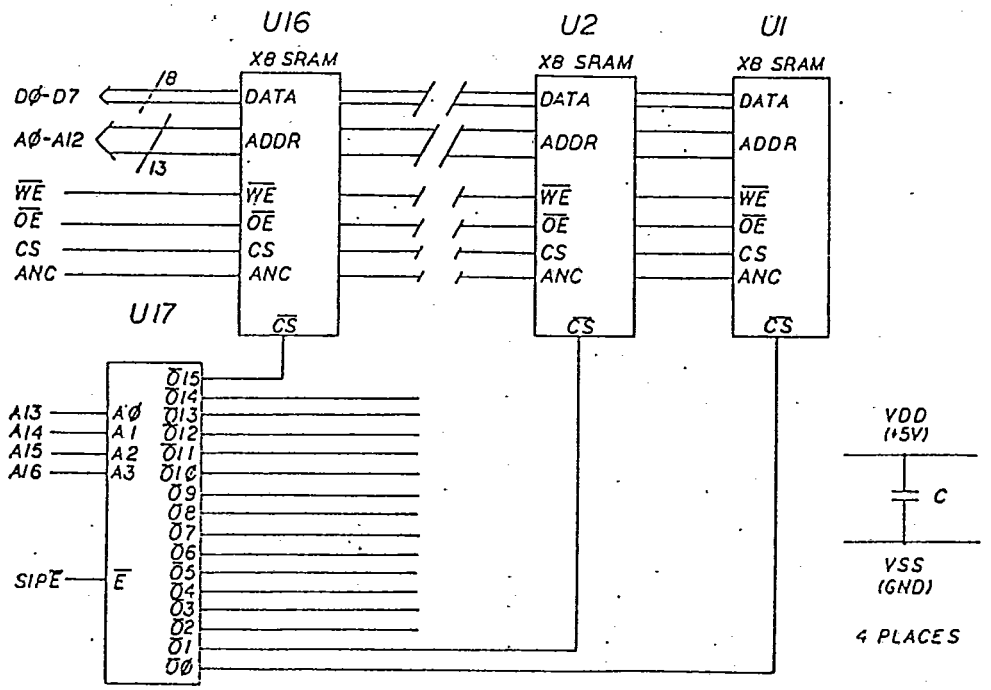


A0 - A16	ADDRESS INPUTS (128K)
A0 - A18	ADDRESS INPUTS (512K)
CS	CHIP SELECT
I/O1 - I/O8	DATA LINES
WE	WRITE ENABLE
SIP E	SIP ENABLE (active LOW)
OE	OUTPUT ENABLE
Vdd	POWER +5V
Vss	GROUND
N/C	NO CONNECT
AN/C	NO CONNECT (reserved for next generation address lines)

NOTE:

ADDRESS INPUTS A13 TO A16 ARE CONNECTED TO THE DECODER ON BOTH THE 128K AND 512K MODULES. IF COMPATIBILITY BETWEEN THE TWO VERSIONS IS NOT A CONCERN, WE RECOMMEND MAKING THESE THE HIGHEST ORDER ADDRESS LINES WHEN USING ONLY 512K MODULES.

FUNCTIONAL DIAGRAM OF THE 128K X 8 SRAM



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PART NUMBERING CHART

	Vertical lead pins	Horizontal lead pins
Standard 128K x 8		
100ns SRAM ICs	AEPSS128K8-10	AEPSH128K8-10
120ns SRAM ICs	AEPSS128K8-12	AEPSH128K8-12
High Speed		
30ns SRAM ICs	AEPSS128K8-30	AEPSH128K8-30
35ns SRAM ICs	AEPSS128K8-35	AEPSH128K8-35
45ns SRAM ICs	AEPSS128K8-45	AEPSH128K8-45
55ns SRAM ICs	AEPSS128K8-55	AEPSH128K8-55
70ns SRAM ICs	AEPSS128K8-70	AEPSH128K8-70

Decoder notes:
The standard decoder is the HCT154 (which can add 35ns to the access speed in worst case). AEP may substitute the F154 or the LS154 if these are more readily available. Specific decoders may be ordered by adding -HCT or -F or -LS to the end of the part number. Add -HC to order the low power CMOS compatible HC154 decoder. The F154 (which can add 10ns in worst case to the access time) is standard with the high speed versions. This device does draw slightly more power than the HCT type -- see Signetics data sheet.

Memory notes:
Memory access speeds specified in the part numbers are maximums. AEP reserves the right to use faster rated devices unless requested not to. As an example, 100ns parts may be substituted for 120ns parts depending on stocks on hand.

Vendor notes:
The IC device specification information included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this may affect module price.

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