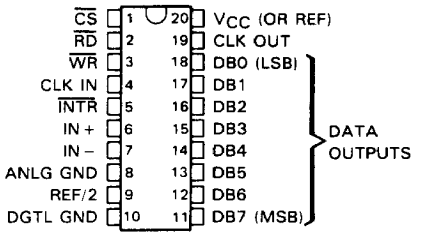
TYPES ADC0801, ADC0802, ADC0803, ADC0805 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH DIFFERENTIAL INPUTS

D2754, NOVEMBER 1983

- 8-Bit Resolution
- Ratiometric Conversion
- 100 μs Conversion Time
- 135 ns Access Time
- Guaranteed Monotonicity
- High Reference Ladder Impedance 8 kΩ Typical
- No Zero Adjust Requirement
- On-Chip Clock Generator
- Single 5-Volt Power Supply
- Operates With Microprocessor or as Stand-Alone
- Designed to be Interchangeable with National Semiconductor ADC0801, ADC0802, ADC0803, ADC0805

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The ADC0801, ADC0802, ADC0803, and ADC0805 are CMOS 8-bit successive-approximation analog-to-digital converters that use a modified potentiometric (256R) ladder. These devices are designed to operate from common microprocessor control buses, with the three-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The devices can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0801I, ADC0802I, ADC0803I, and ADC0805I will be characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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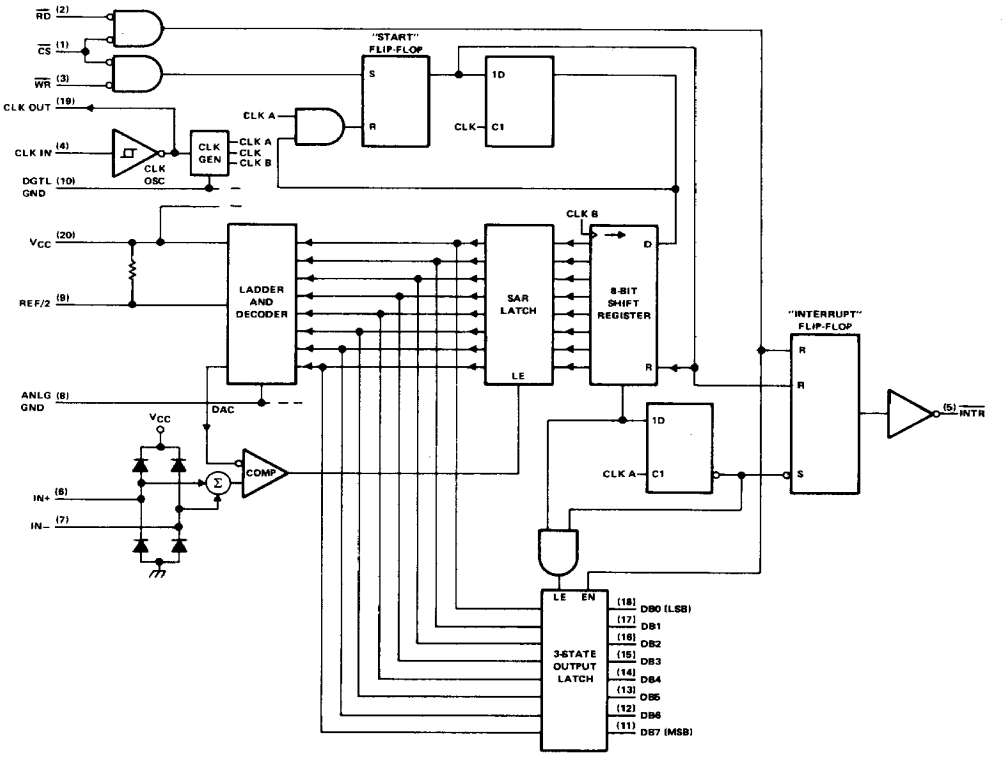
functional block diagram (positive logic)



Data Acquisition

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
Other inputs . . . . . −0.3 V to V_{CC} +0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} +0.3 V
Continuous total power dissipation at 25°C free-air temperature (see Note 2) . . . . . 875 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together (unless otherwise noted).
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, section 2.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	6.3	V
$V_{REF/2}$	Voltage at REF/2 (see Note 3)	0.25	2.5		V
V_{IH}	High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$	2		15	V
V_{IL}	Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$			0.8	V
	Analog ground voltage (see Note 4)	−0.05	0	1	V
	Analog input voltage (see Note 5)	GND−0.05		V_{CC}+0.05	V
f_{clock}	Clock input frequency (see Note 6)	100	640	1460	kHz
	Duty cycle above 640 kHz (see Note 6)	40		60	%
$t_{w(CLK)}$	Pulse duration clock input (high or low)	275	781		ns
$t_{w(WR)}$	Pulse duration, $\overline{WR}$ input low	100			ns
T_A	Operating free-air temperature	−40		85	°C

NOTES: 3. Proper operation is achieved over a differential input range of 0 V to V_{CC} when the REF/2 input is open.
4. These values are with respect to digital ground (pin 10).
5. When the positive analog input with respect to the negative analog input ($V_{in+} - V_{in-}$) is zero or negative, the output code is 0000 0000.
6. Total unadjusted error is guaranteed only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, f_{clock} = 640 kHz, $V_{REF/2}$ = 2 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V,	I_{OH} = −360 μA	2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V,	I_{OH} = −10 μA	4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA			0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V,	I_{OL} = 1 mA			0.4	
		CLK OUT	V_{CC} = 4.75 V,	I_{OL} = 360 μA			0.4	
V_{T+}	Clock positive-going threshold voltage				2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage				1.5	1.8	2.1	V
$V_{T+} - V_{T-}$	Clock input hysteresis				0.6	1.3	2	V
I_{IH}	High-level input current					0.005	1	μA
I_{IL}	Low-level input current					−0.005	−1	μA
I_{OZ}	Off-state output current		V_O = 0				−3	μA
			V_O = 5 V				3	
I_{OHS}	Short-current output current	Output high	V_O = 0,	T_A = 25°C	−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V,	T_A = 25°C	9	16		mA
I_{CC}	Supply current plus reference current		$V_{REF/2}$ = open, $\overline{CS}$ at 5 V	T_A = 25°C,		1.1	1.8	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 7		2.5	8		kΩ
C_i	Input capacitance (control)					5	7.5	pF
C_o	Output capacitance (DB)					5	7.5	pF

NOTE 7: Resistance is calculated from the current drawn from a 5-volt supply applied to pins 8 and 9.

operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error		V_{CC} = 4.5 V to 5.5 V,	See Note 8		±1/16	±1/8	LSB
	Total adjusted error	ADC0801	With full-scale adjust,	See Notes 8 and 9			±1/4	LSB
		ADC0803					±1/2	
	Total unadjusted error	ADC0802	$V_{REF/2}$ = 2.5 V,	See Notes 8 and 9			±1/2	LSB
		ADC0805	$V_{REF/2}$ open,	See Notes 8 and 9			±1	
	DC common-mode error		See Note 8 and 9			±1/16	±1/8	LSB
t_{en}	Output enable time		C_L = 100 pF			135	200	ns
t_{dis}	Output disable time		C_L = 10 pF,	R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$					300	450	ns
t_{conv}	Conversion cycle time		f_{clock} = 100 kHz to 1.46 MHz, See Note 10		66		73	clock cycles
CR	Free-running conversion rate		$\overline{INTR}$ connected to $\overline{WR}$, $\overline{CS}$ at 0 V				8770	conv/s

†All typical values are at T_A = 25°C.

NOTES: 8. These parameters are guaranteed over the recommended analog input voltage range.
9. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristic.
10. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

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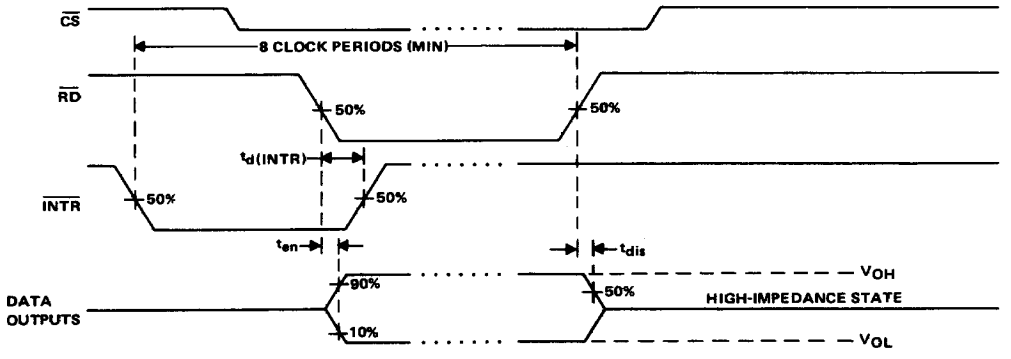
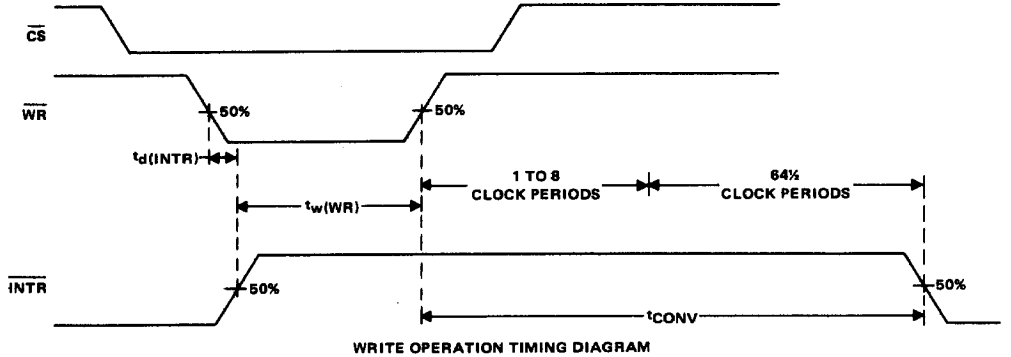
PARAMETER MEASUREMENT INFORMATION



READ OPERATION TIMING DIAGRAM



WRITE OPERATION TIMING DIAGRAM

PRINCIPLES OF OPERATION

The ADC0801, ADC0802, ADC0803, and ADC0805 each contain a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive approximation logic to match an analog differential input voltage ($V_{in+} - V_{in-}$) to a corresponding tap on the 256R network. The most-significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low anytime after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the internal successive approximation register (SAR) and eight-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter will remain in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and eight-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the eight-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the eight-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the three-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

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