ADC-856
Monolithic 10-Bit Tracking A/D Converter

FEATURES

- **Continuous tracking operation**
- **10^6 conversions/second**
- **10-Bit resolution**
- **Monotonic over temperature**
- **Controllable outputs**
- **TTL/CMOS compatible**

GENERAL DESCRIPTION

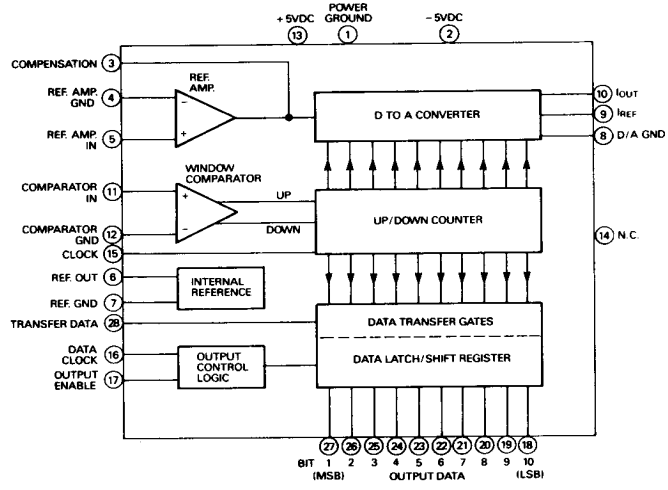
The ADC-856 is a 10-bit tracking A/D converter, capable of supplying continuously updated conversion data on full-scale sinusoidal signals up to 300 Hz without the need for a sample and hold. This converter is linear to ±½ LSB minimum and is monotonic over its operating temperature range. A number of innovative features give this device the flexibility for a wide range of applications.

The circuit is implemented in bipolar, monolithic form. The chip contains a fast window comparator, tracking logic, an up/down counter, a D/A converter, a precision voltage reference with amplifier, data transfer gates, and a data latch/shift register. The external parts required for operation have been held to a few passive components, and allow external programming of the analog input voltage range. Gain temperature coefficient of the circuit is ± 10 ppm/°C, exclusive of reference.

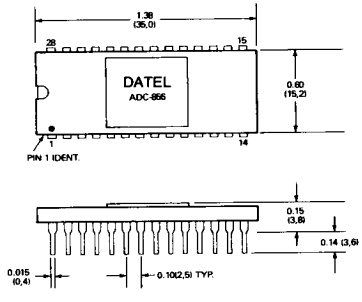
The ADC-856 is optimized for operation in a continuous tracking mode. In this conversion technique each conversion of an analog signal is based on the last converted value of that signal. For signals that do not vary faster than the converter can track, or 1 LSB/microsecond, continuous tracking will provide a valid, updated conversion result every microsecond.

Logic control inputs contribute to this device's usefulness in many different applications. The data transfer gates allow selection of the rate at which the output latch/shift register is updated. The rate may vary from once every microsecond to updating only upon receipt of a command from an external controller. External control also allows selection of output data form, which may be parallel or serial (by supplying an optional clock input). The outputs may be disabled completely in either mode by holding the output enable input low.

The ADC-856 operates on ± 5V dc power at 50 mA with a power supply rejection of 0.1%/V. The device is packaged in a 28 ceramic DIP and is available in two operating temperature ranges: 0°C to +70°C and −55°C to +125°C.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	15	CLOCK
2	-5VDC	16	DATA CLOCK
3	COMPENSATION	17	OUTPUT ENABLE
4	REF. AMP. GND	18	BIT 10 OUT (LSB)
5	REF. AMP. IN	19	BIT 9 OUT
6	REF. OUT	20	BIT 8 OUT
7	REF. GND	21	BIT 7 OUT
8	D/A GND	22	BIT 6 OUT
9	I_{REF}	23	BIT 5 OUT
10	I_{OUT}	24	BIT 4 OUT
11	COMPARATOR IN	25	BIT 3 OUT
12	COMPARATOR GND	26	BIT 2 OUT
13	+5VDC	27	BIT 1 OUT* (MSB)
14	N.C.	28	TRANSFER DATA

*Serial data output when in serial data mode

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage	±7 Volts
Logic Input Voltage	0V to $+V_{CC}$

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supply and Internal Reference, unless otherwise noted.

PERFORMANCE	
Resolution	10 Bits
Linearity Error	±½ LSB maximum
Differential Linearity Error	±½ LSB
No Missing Codes	Over Oper. Temp. Range
Conversion Time, 1 LSB change	1 μsec.
Conversion Time, Full Scale Change	1.024 msec.[1]
Tracking Speed	1 LSB/μsec. maximum
Tracking Bandwidth, Full Scale	300 Hz[2]
Gain Tempco	10 ppm/°C[4]
Zero Tempco	7 ppm/°C of FSR[6]
Power Supply Rejection	0.1%/V

INPUTS	
Analog Input Range[7], Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Reference Current	1 mA ±0.2 mA
Input Logic Level, high ("1")	+2.0V minimum at 50 μA[3]
Input Logic Level, low ("0")	+0.8V maximum at 1 μA[3]
Clock Pulse Width	100 nsec. minimum
Clock Rate	1 MHz maximum
Data Transfer Input	Hold high for 50 nsec. minimum to load output latches
Output Enable Input	When low, disables data clock and turns outputs off (high)
Data Clock Input	When driven by clock at ≤1 MHz with minimum pulse width of 100 nsec., provides serial data output at Pin 27.

OUTPUTS	
Reference Voltage	2.48V ±1.5%
Reference Tempco	40 ppm/°C
Reference Load Current, maximum	4 mA
D/A Output Current, Full Scale	4 mA[5]
Data Output	Parallel or Serial
Output Logic Level, high ("1")	+2.4V minimum at −40 μA
Output Logic Level, low ("0")	+0.4V maximum at 1.6 mA
Coding, Unipolar	Straight Binary
Coding, Bipolar	Offset Binary

POWER REQUIREMENTS	
Supply Voltage Range	±4.5V to ±5.5V
Supply Current	50 mA
Power Consumption	500 mW
Operating Temperature Range	
ADC-856C	0°C to +70°C
ADC-856M	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Package	28 Pin Ceramic DIP

FOOTNOTES:

1. Conversion time is directly dependent on the magnitude of input signal change.
2. Tracking bandwidth is inversely proportional to input signal amplitude, e.g. bandwidth is 600 Hz at half scale.
3. V_S = ±5.5V
4. Exclusive of Reference.
5. The full scale D/A output current is 4 times I_{REF}.
6. FSR is the Full Scale Range, the difference between maximum and minimum inputs.
7. Analog input range is programmed by an external resistor.

TECHNICAL NOTES

1. The transfer of conversion data to the outputs is controlled by the transfer gates. When TRANSFER DATA is held high the outputs update with each conversion. To update the outputs upon command. TRANSFER DATA is taken high for a minimum of 50 nanoseconds, no sooner than 150 nanoseconds after the active (negative going) edge of the main clock. TRANSFER DATA must go low before the next main clock edge. When TRANSFER DATA is low, the data is held in the output register.
2. Conversion data appears at the outputs in parallel form. Data may be obtained in serial form by clocking DATA CLOCK at up to 1 MHz, with a minimum pulse width of 100 nanoseconds and TRANSFER DATA low. Serial output data (MSB first) is then available at pin 27.
3. When OUTPUT ENABLE is taken low DATA CLOCK is disabled and all output transistors are turned off (all bit outputs go high).
4. The converter tracks the input signal level at a speed of 1 LSB/microsecond; thus the conversion time for any input signal change is given by

$$\frac{\Delta V_{IN}}{1\ LSB} = \text{conversion time in microseconds.}$$

5. Full Scale D/A output current is four times the reference current; for optimum performance the reference current should be 1 mA. An external reference can be used which can range from 0.8 mA to 1.2 mA.
6. The tracking bandwidth is inversely proportional to the amplitude of the input signal, e.g., at half scale the bandwidth is 600 Hz.
7. The window comparator and tracking logic determine whether the up/down counter will count up/count down or retain the same value on the negative going edge of the clock pulse.
8. Since the gain tempco of the converter is typically 10 ppm/°C, it is recommended that 10 ppm/°C metal film resistors be used for R_3, R_4 and R_5 for best performance over temperature. The internal reference will typically add 40 ppm/°C to the gain tempco. For improved performance a high quality external reference should be used.
9. R_1 and R_2 compensate for the input bias currents of the reference amplifier and comparator whose inputs are at virtual ground. Thus $R_1 = R_3$ and R_2 = the parallel combination of R_4, R_5 and R_6. The parallel combination of R_4, R_5 and R_6 should be as close to 625Ω as possible as this determines the D/A setting time and therefore the conversion time. Refer to the resistor tables for a list of typical values for these resistors.

THEORY OF OPERATION

The ADC-856 converters employ a tracking conversion technique. Tracking converters are most effectively used in single-channel operations on a continuous signal. In this technique each conversion is based on the previous conversion value. A fast window comparator determines whether an up/down counter increments by 1 LSB, decrements by 1 LSB or remains at its last value. The digital word in the counter controls a D/A converter with a precision reference; the analog output goes to the comparator and is compared with the analog input signal.

For signals with a rate of change less than the converter's maximum rate of change (tracking speed), each comparison represents a valid conversion and the converter is therefore tracking the signal. Tracking is not possible when the input signal varies at a rate greater than the converter's maximum or is discontinuous, as in multiplexed applications. In these cases the converter will change at its maximum rate (1 LSB/microsecond) until it attains the new signal level. While this acquisition is in progress, each converter step is available to the output as data, even though it does not yet represent the input signal level. The time required to acquire a new signal level is directly proportional to its difference from the previous level; for a full scale change this period is over 1 microsecond. Allowance should be made for the acquisition time when a rapid signal change is introduced.

UNIPOLAR OPERATION

Zero and Gain Adjustments

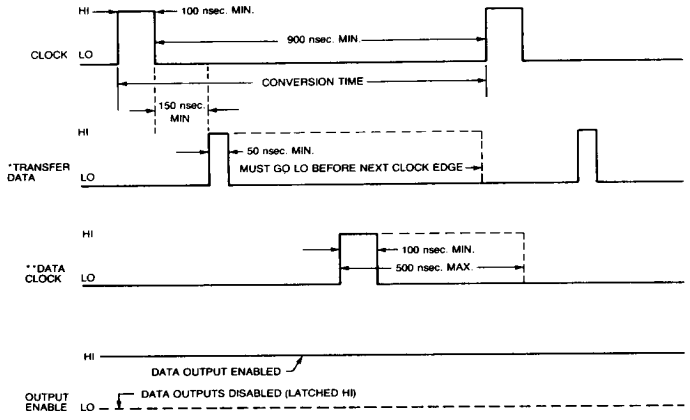
1. Apply an analog input voltage of zero + ½ LSB.
2. Adjust the zero adjustment so that the ouput code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of + F.S. – 1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

BIPOLAR OPERATION

Offset and Gain Adjustments

1. Apply an analog input voltage of – full-scale + ½ LSB.
2. Adjust the offset adjustment (R_4) so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of + full-scale – 1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

TIMING DIAGRAM



*IF TRANSFER DATA IS HELD HI, THEN THE COUNTER OUTPUTS APPEAR DIRECTLY AT THE BIT OUTPUTS.
**DRIVEN FOR SERIAL DATA OUTPUT ONLY.

CODING TABLES

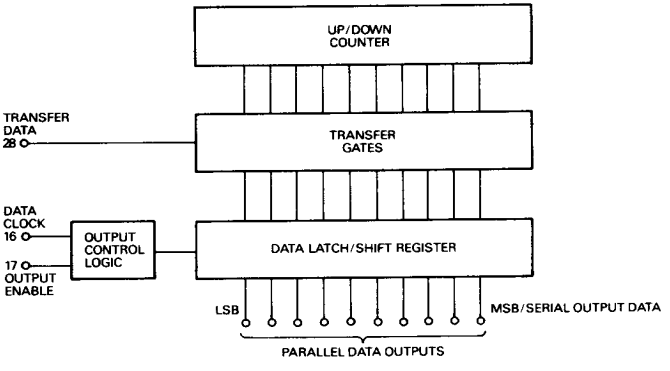
UNIPOLAR OPERATION STRAIGHT BINARY

SCALE	CODE
+ FS – 1 LSB	1111111111
+ ¾ FS	1100000000
+ ½ FS	1000000000
+ ¼ FS	0100000000
+ 1 LSB	0000000001
0	0000000000

BIPOLAR OPERATION OFFSET BINARY

SCALE	CODE
+ FS – 1 LSB	1111111111
+ ½ FS	1100000000
+ 1 LSB	1000000001
0	1000000000
– 1 LSB	0111111111
– ½ FS	0100000000
– FS + 1 LSB	0000000001
– FS	0000000000

OUTPUT LOGIC CONTROL



TRANSFER DATA (PIN 28)

HI: Min. 50 nsec pulse transfers parallel data from the up/down counter to the data latch/shift register. May be held high for continuous data transfer

LO: Data in latches held, new data from counter not transferred to data latches

DATA CLOCK (PIN 16)

HI: Clocked at up to 1 MHz for serial data output at Pin 27, MSB first

LO: Output data in parallel format at pins 18-27

OUTPUT ENABLE (PIN 17)

HI: Data available at outputs (parallel or serial)

LO: Output transistors turned OFF, all data outputs latched HI

CONNECTION AND CALIBRATION

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram. Note that Pin 6 is connected to R_3 and R_4 only when the internal reference is used (dotted line on diagram).
2. Select R_1 through R_6 from values given in the resistor table or calculate from the equations that accompany it.
3. Drive the MAIN CLOCK input (Pin 15) with a compatible clock signal at up to 1 MHz and apply a logic high to TRANSFER DATA (Pin 28).

CALIBRATION RESISTOR VALUES

R_4 adjusts the offset for bipolar operations; in unipolar operations R_4 is replaced with a zero adjustment circuit shown in applications. In either mode R_3 adjusts the gain. If the predicted values of these resistors do not supply the transition points expected, their values should be recalculated. Each may be trimmed with a 100 ppm/°C trimming pot used in series with the resistor. The trim pots should be constrained to approximately 1% of the nominal value calculated.

The values of R_1 through R_6 are calculated from the following:

*R_1 = R_3 *R_2 = the parallel combination of R_4, R_5 and R_6.

$$R_3 = \frac{V_{REF}}{1.0\ mA} \qquad R_4 = \frac{-V_{REF}R_5}{V_{IN}min}$$

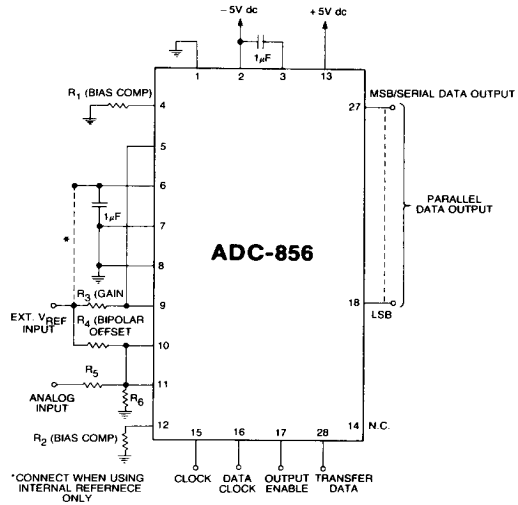
$$R_5 = \frac{FSR^{**}}{I_{OUT}(max)}$$

*R_6 is chosen so that the parallel combination of R_4, R_5 and R_6 is approximately 625Ω. This determines the D/A time constant and conversion time.

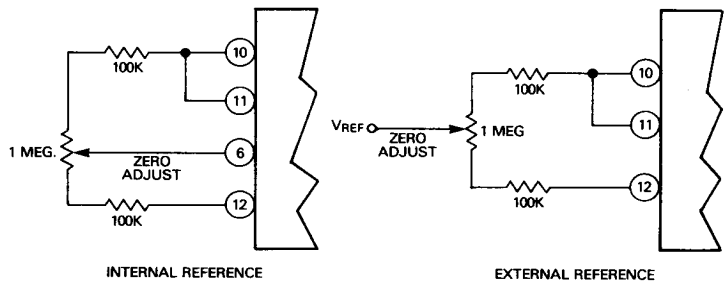
*The nearest preferred value may be used for these resistors.

**F.S.R. is the Full Scale Range, the difference between maximum input voltage and minimum input voltage.

CONNECTION AND CALIBRATION DIAGRAM



UNIPOLAR ZERO



FOR UNIPOLAR OPERATION WHERE R_4 APPROACHES ∞ AND A ZERO ADJUSTMENT IS REQUIRED, THIS CIRCUIT MAY BE USED TO REPLACE R_4.

RESISTOR TABLES

ANALOG INPUT RANGE	V_{REF}[2]	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
0 to +2.5V	2.5V	2.5K	625Ω	2.5K	∞	625Ω	∞
0 to +5.0V	2.5V	2.5K	625Ω	2.5K	∞	1.25K	1.25K
±2.5V	2.5V	2.5K	625Ω	2.5K	1.25K	1.25K	∞
0 to +10V	2.5V	2.5K	625Ω	2.5K	∞	2.5K	835Ω
±5V	2.5V	2.5K	625Ω	2.5K	1.25K	2.5K	2.5K
±10V	2.5V	2.5K	625Ω	2.5K	1.25K	5K	1.67K

NOTES: 1. The nearest preferred value may be used for R_1, R_2 and R_6.
2. For external reference set R_1 = V_{REF} (Kohms)

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE
ADC-856C	0°C to +70°C
ADC-856M	-55°C to +125°C

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356