



### 3 V Self Recovering Watchdog

#### Features

- Watchdog fully operational from 2.7 to 5.25 V
- Regulated DC voltage monitor, internal voltage reference
- Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100 ms), externally programmable from 3 ms to 3 mins if required
- Works down to 1.6 V supply voltage
- Low voltage alarm prior to reset on power-down
- Reset outputs of both polarities
- Open drain outputs
- Small footprint SO8 and DIP8 packages

#### Description

The H6061 is a combined initialiser, watchdog and voltage monitor. The circuit is a low voltage low power monolithic CMOS device combining a series of voltage comparators and a programmable timer on the same chip. The device is specially suited to telecommunications applications where 3 V working is expected, for functions such as supply voltage and microprocessor monitoring. The reset outputs are self recovering after a watchdog timeout, enabling the circuit to work with standalone systems without any external push-switch or control signal to restart after a watchdog timeout. The circuit provides a reset signal of both polarities. The state of the outputs is defined down to 1.6 V. An internal debouncer ensures power-up performance for fast-rise supply lines.

#### Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems
- Microcontroller 68HC05 applications

#### Typical Operating Configuration

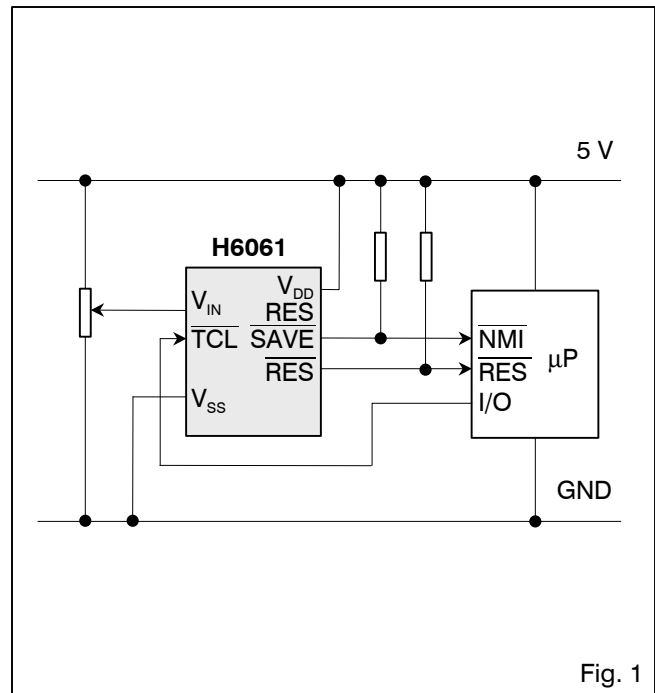


Fig. 1

#### Pin Assignment

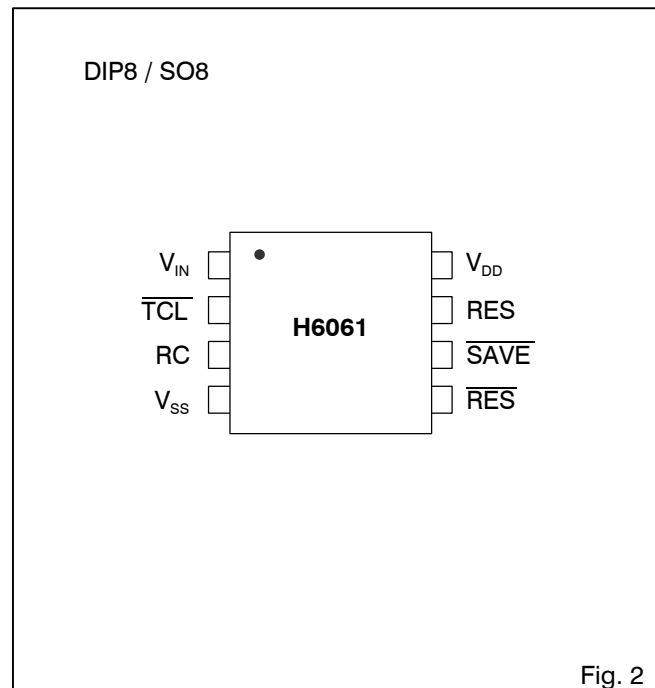
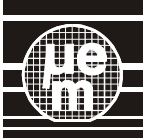


Fig. 2



## Absolute Maximum Ratings

| Parameter  | Symbol      | Conditions       |
|--|-------------|------------------|
| Voltage $V_{DD}$ to $V_{SS}$                             | $V_{DD}$    | - 0.3 to + 5.6 V |
| Voltage at any pin to $V_{SS}$                           | $V_{MIN}$   | - 0.3            |
| Voltage at any pin to $V_{DD}$                           | $V_{MAX}$   | + 0.3            |
| Voltage at $V_{IN}$ to $V_{SS}$                          | $V_{INMAX}$ | + 12 V           |
| Current at any output                                    | $I_{MAX}$   | ± 10 mA          |
| Storage temperature                                      | $T_{STO}$   | -65 to +150 °C   |
| Electrostatic discharge max. to MIL-STD-883C method 3015 | $V_{Smax}$  | 1000 V           |

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

## Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, it is advised that normal precautions be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

## Operating Conditions

| Parameter                               | Symbol   | Min. | Typ. | Max. | Units |
|---|----------|------|------|------|-------|
| Operating temperature Industrial        | $T_A$    | -40  |      | +85  | °C    |
| Supply voltage                          | $V_{DD}$ | 2.7  |      | 5.25 | V     |
| Monitored input voltage                 | $V_{IN}$ | 0    |      | 12   | V     |
| RC-oscillator programming (see Fig. 15) |          |      |      |      |       |
| External capacitance*                   | C1       |      |      | 1    | μF    |
| External resistance                     | R1       | 10   |      |      | kΩ    |

\* Leakage < 1 μA

Table 2

## Electrical Characteristics

$V_{DD} = 5.0$  V,  $T_A = -40$  to +85 °C, unless otherwise specified

| Parameter                                    | Symbol    | Test Conditions                             | Min. | Typ.           | Max. | Units |
|--|-----------|---|------|----------------|------|-------|
| $V_{DD}$ activation threshold                | $V_{ON}$  | $T_A = 25$ °C                               | 2.3  |                | 2.7  | V     |
| $V_{DD}$ deactivation threshold              | $V_{OFF}$ | $T_A = 25$ °C                               |      | $V_{ON} - 0.3$ |      | V     |
| Supply current                               | $I_{DD}$  | RC open, TCL at $V_{DD}$ or $V_{SS}$        |      | 80             | 140  | μA    |
| <b>Input <math>V_{IN}</math>, TCL</b>        |           |   |      |                |      |       |
| Leakage current                              | $I_P$     | $V_{SS} < V_{IP} < V_{DD}$<br>$T_A = 80$ °C |      | 0.005          | 1    | μA    |
| TCL input low level                          | $V_{IL}$  |   |      |                | 0.8  | V     |
| TCL input high level                         | $V_{IH}$  |   | 2.4  |                |      | V     |
| Leakage on pins $\overline{SAVE}$ , RES, RES | $I_{OLK}$ | $V_{OUT} = V_{DD}$                          |      | 0.050          | 1    | μA    |
| O/P drive logic low                          | $I_{OL}$  | $V_{OL} = 0.4$ V                            | 4    | 8              |      | mA    |
|  | $I_{OL}$  | $V_{DD} = 3.5$ V; $V_{OL} = 0.4$ V          | 2    |                |      | mA    |
|  | $I_{OL}$  | $V_{DD} = 1.6$ V; $V_{OL} = 0.4$ V          | 80   |                |      | μA    |

Table 3

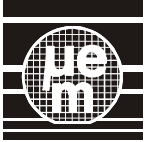
## $V_{IN}$ Surveillance

Voltage thresholds at  $T_A = 25$  °C

| Version No. | Thresholds |          |          | at $V_{DD}$ | Threshold Voltage Tolerance | Threshold Ratio* | Pin $V_{IN}$ Input |
|-------------|------------|----------|----------|-------------|-----------------------------|------------------|--------------------|
|             | $V_{SH}$   | $V_{SL}$ | $V_{RL}$ |             |                             |                  |                    |
| 25          | 1.54       | 1.50     | 1.46     | 2.7 – 5.0 V | ±10%                        | ±2%              | ~100 MΩ            |

\* Threshold ratio defined as  $V_{SH} / V_{SL}$  or  $V_{SL} / V_{RL}$ .

Table 4



## Timing Characteristics

$V_{DD} = 5.0\text{ V}$ ,  $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$  ( $-40\text{ to }+125\text{ }^\circ\text{C}$  for extended temperature range version), unless otherwise specified

| Parameter                                    | Symbol     | Test Conditions                                       | Min. | Typ.        | Max. | Units         |
|--|------------|---|------|-------------|------|---------------|
| Propagation delays<br>TCL to output pins     | $T_{DIDO}$ | Excluding debounce time $T_{DB}$                      |      | 250         | 500  | ns            |
| $V_{IN}$ to output pins                      | $T_{AIDO}$ |   |      | 4           | 10   | $\mu\text{s}$ |
| Logic transition times on<br>all output pins | $T_{TR}$   | Load 10 k $\Omega$ , 100 pF                           |      | 30          | 100  | ns            |
| Timeout period                               | $T_{TO}$   | RC open, unshielded, $T_A = 25\text{ }^\circ\text{C}$ | 60   | 100         | 160  | ms            |
| $T_{TCL}$ input pulse width                  | $T_{TCL}$  |   | 150  |             |      | ns            |
| Power-on reset debounce                      | $T_{DB}$   |   |      | $T_{TO}/64$ |      | ms            |
| Fastest pulse $V_{IN}$<br>with debounce      | $T_{VINL}$ | $-40\text{ to }+85\text{ }^\circ\text{C}$             | 10   |             |      | $\mu\text{s}$ |

Table 5

## Timing Waveforms

### Voltage Reaction: $V_{DD}$ Monitoring

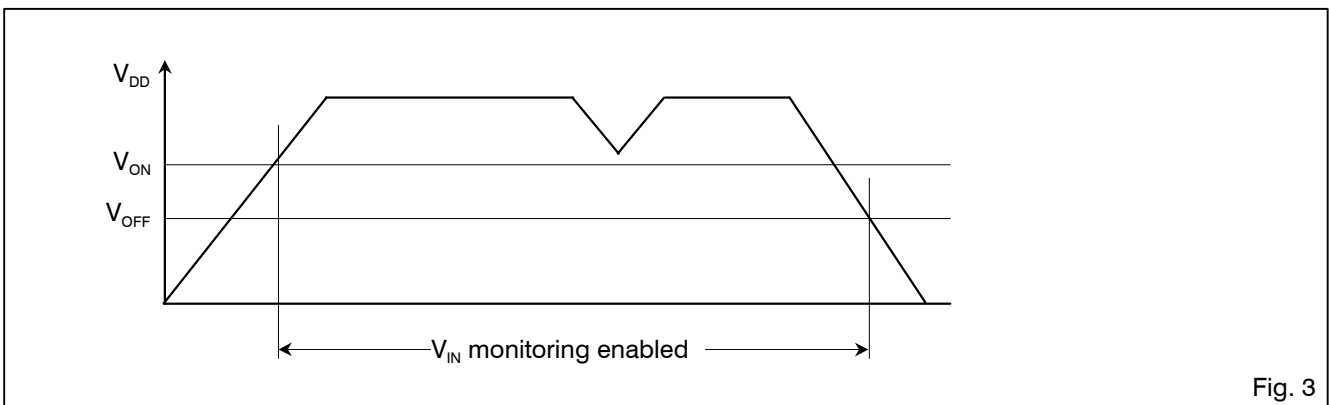


Fig. 3

### Voltage Reaction: $V_{IN}$ Monitoring

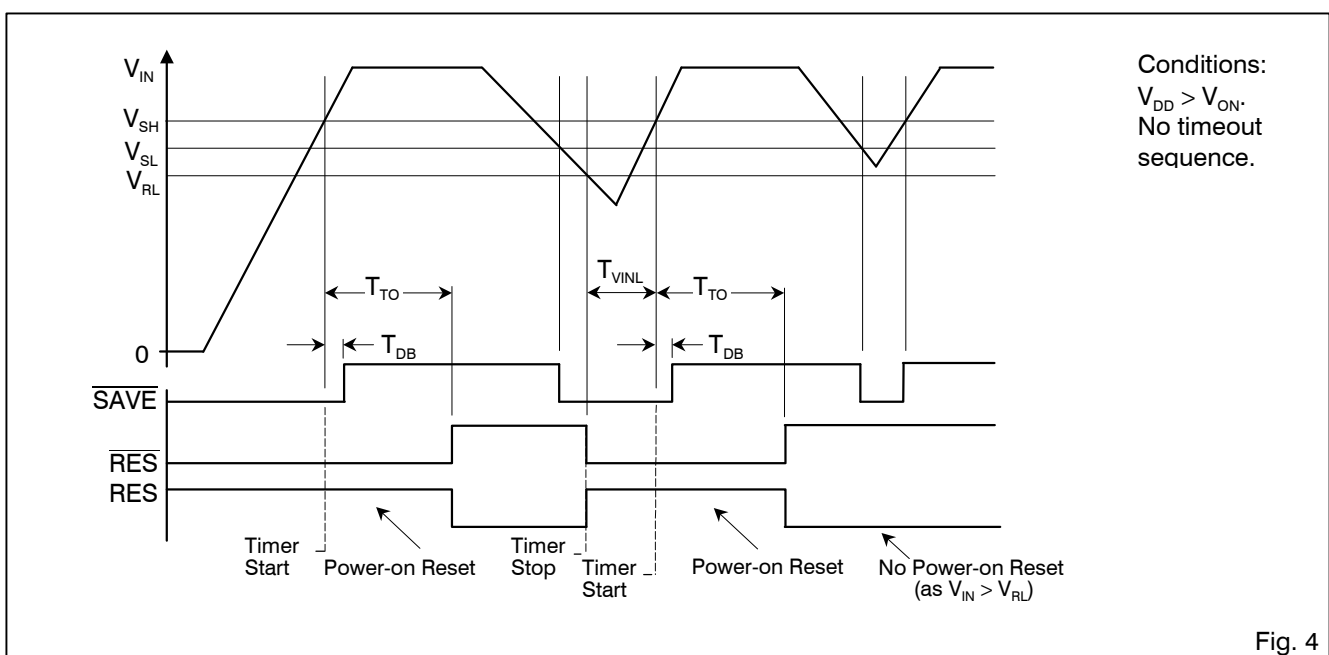
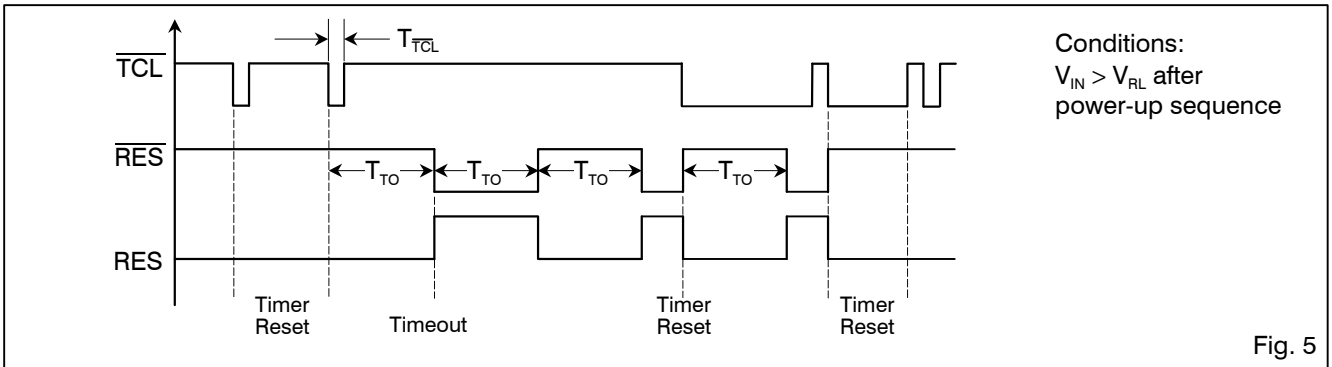


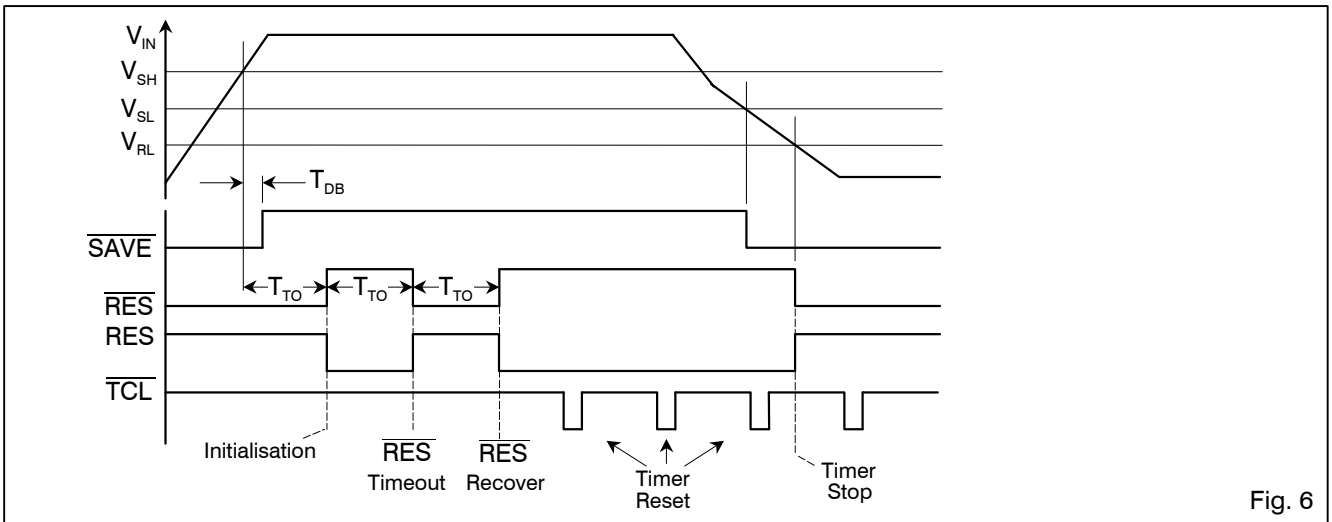
Fig. 4



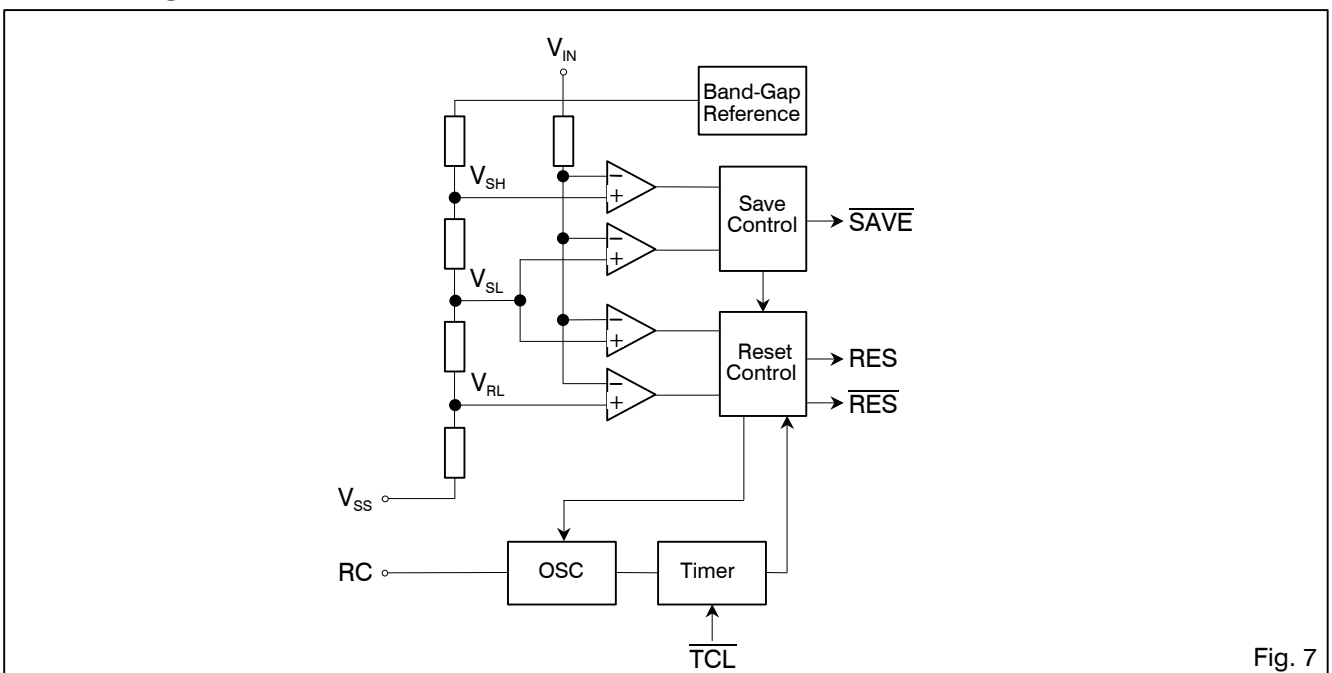
## Timer Reaction

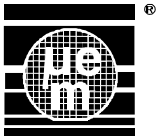


## Combined Voltage and Timer Reaction



## Block Diagram





## Pin Description

| Pin | Name            | Function                          |
|-----|-----------------|-----------------------------------|
| 1   | V <sub>IN</sub> | Voltage monitoring input          |
| 2   | TCL             | Timer clear input signal          |
| 3   | RC              | RC oscillator tuning input        |
| 4   | V <sub>SS</sub> | GND terminal                      |
| 5   | RES             | Reset output, open drain          |
| 6   | SAVE            | Save output, open drain           |
| 7   | RES             | Positive reset output, open drain |
| 8   | V <sub>DD</sub> | Positive supply voltage           |

Table 6

## Functional Description

### Thresholds and Outputs

The H6061 has open-drain outputs and voltage thresholds on pin V<sub>IN</sub> of typically 1.5 V.

### Internal Voltage Comparators

The voltage comparators detect the voltage applied to pin V<sub>IN</sub> and compare it with thresholds V<sub>SH</sub>, V<sub>SL</sub> and V<sub>RL</sub>. The H6061 is designed for monitoring regulated DC voltages and has bandgap thresholds independent of V<sub>DD</sub>. The reaction of the H6061 to voltage changes on pin V<sub>IN</sub> is given in Fig. 4. During powering-up, the outputs are active. After V<sub>IN</sub> reaches the V<sub>SH</sub> level, pin  $\overline{\text{SAVE}}$  deactivates after a short debounce time T<sub>DB</sub> to allow for fast ramp-ups. The initialization time T<sub>TO</sub> then passes before the two reset outputs go inactive. Thereafter, when the voltage on pin V<sub>IN</sub> falls below the V<sub>SL</sub> level, pin  $\overline{\text{SAVE}}$  goes active low as a first warning. If V<sub>IN</sub> then drops below the V<sub>RL</sub> level, the reset signals go active and are guaranteed down to 1.6 V. The reset outputs react also to timeouts (see "Timer clearing"). Note that when the supply voltage V<sub>DD</sub> is below the level V<sub>OFF</sub> (about 2.2 V), all outputs are in the active state for any allowed voltage of V<sub>IN</sub>.

### Voltage Programming

The H6061 was designed to give the best compromise in normal usage (see Table 3). Its voltage threshold can be programmed by an external resistor divider or a potentiometer to react at proportionally higher voltage levels (see Fig. 8 below).

### Voltage Programming

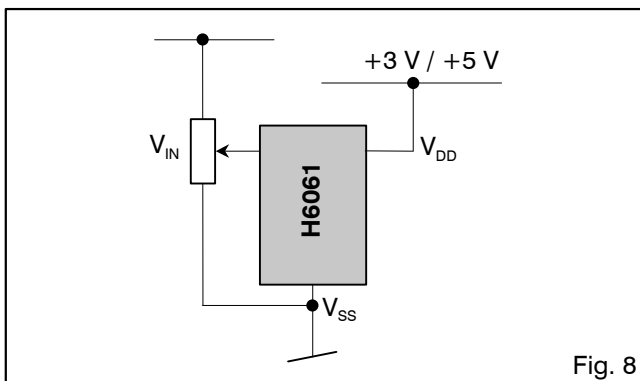


Fig. 8

### Timer Programming

A single timeout period T<sub>TO</sub> is used for the initialization reset duration and the watchdog timeout. With pin RC unconnected, the on-chip RC oscillator and divider chain give a timeout period T<sub>TO</sub> of typically 100 ms. A resistor to V<sub>DD</sub> will shorten this time, and a capacitor to V<sub>SS</sub> will lengthen it (see Fig. 11). An approximation for calculating trial values given in milliseconds by the formula:

$$T_{TO} = \left[ 0.75 + \frac{(32 + C_1) \cdot 1.6}{4.8 + \frac{V_{DD} - 0.8}{R_1}} \right] \cdot 8.192$$

$$R_{1 \min.} = 10 \text{ k}\Omega, C_{1 \max.} = 1 \mu\text{F}$$

If R<sub>1</sub> is in MΩ and C<sub>1</sub> in pF, T<sub>TO</sub> will be in ms.

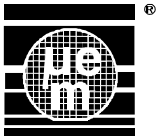
Choice of component values must be determined in practice. To have a square wave of period 2T<sub>TO</sub>, simply connect pin  $\overline{\text{TCL}}$  to V<sub>DD</sub> or V<sub>SS</sub> and take the signal output from a reset pin.

### Timer Clearing

A negative edge or pulse at the  $\overline{\text{TCL}}$  input longer than 150 ns will clear the timer and deactivate the reset outputs under normal running conditions (see Fig. 3).  $\overline{\text{TCL}}$  will however have no effect either when V<sub>DD</sub> < V<sub>OFF</sub> or during the initialization period before the deactivation of the reset pins.

### Combined Voltage and Timer Action

In Fig. 6 is a typical sequence of power-up, watchdog run, and power-down. During initialization the  $\overline{\text{SAVE}}$  pin deactivates one debounce delay time T<sub>DB</sub> after V<sub>IN</sub> rises above V<sub>SH</sub>, or when the power line V<sub>DD</sub> rises above V<sub>ON</sub>, whichever happens last. The reset pins only deactivate one timeout period T<sub>TO</sub> afterwards to free the watchdog timer and end the initialization. Note that either V<sub>IN</sub> falling below V<sub>RL</sub> threshold or V<sub>DD</sub> below V<sub>ON</sub> will cause an initialization upon recovery. Following initialization, the watchdog timer will time out after time T<sub>TO</sub> unless at least one  $\overline{\text{TCL}}$  pulse clears it. On timeout the reset pins reactivate for a further T<sub>TO</sub> period before deactivating again for another try. A  $\overline{\text{TCL}}$  pulse will deactivate any timeout reset, and another  $\overline{\text{TCL}}$  pulse must follow within a time T<sub>TO</sub> to keep reset inactive. If no  $\overline{\text{TCL}}$  pulses come at all, the reset pins go square-wave. Power-down overrides all this however. A falling voltage on V<sub>IN</sub> gives a warning  $\overline{\text{SAVE}} = 0$  signal at V<sub>IN</sub> = V<sub>SL</sub> before activating the reset pins as soon as V<sub>IN</sub> drops below V<sub>RL</sub>. The H6061 has fixed thresholds and low hysteresis for monitoring regulated DC lines. Additional protection is provided in case V<sub>DD</sub> supply falls over about 10% below V<sub>ON</sub> which thereupon activates all outputs at once.



## Typical Applications

### Microprocessor Watchdog with Voltage Monitor

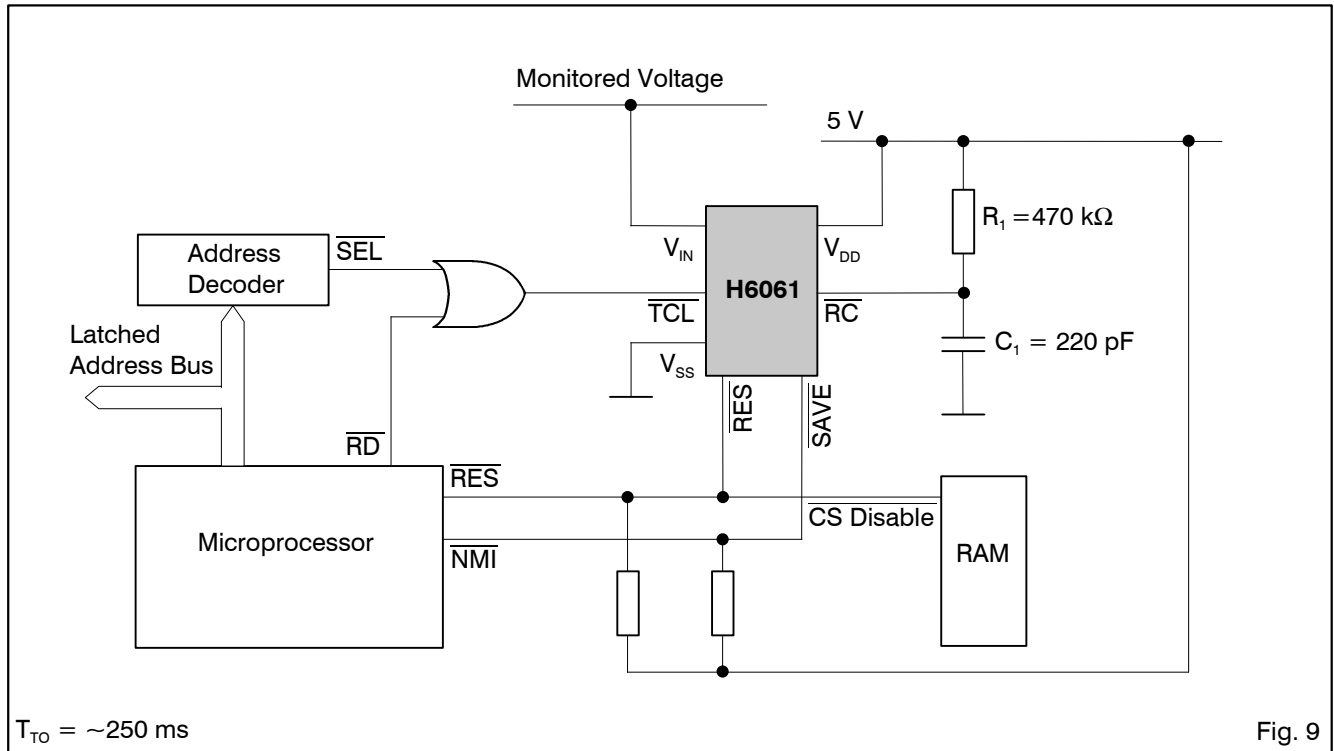


Fig. 9

### Selection of Watchdogs for Each Application

The H6061 is designed for monitoring regulated DC voltages anywhere between 2.7 and 5.25 V. Typically, it is used to monitor  $V_{DD}$  with pin  $V_{IN}$  tied to the midpoint of a voltage divider (see Fig. 8). This arrangement has the advantage of being able to trigger at selectable voltage limits, i. e. it can be used where the regulated voltage is below 5 VDC.

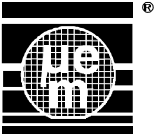
### Industrial Heavy-Duty Utilisation

The H6061 debounce protects against reactions due to fast-rise power lines, but absolute maximum ratings must be respected. With its flexibility of voltage programming and supply voltage the H6061 can allow for voltage drops along supply lines, so it can be placed remotely, like on plug-in boards (see Fig. 9). The H6061 is suitable for supply voltages down to 2.7 VDC. As the H6061 is designed to be sensitive to voltage changes, fast switching lines, like address/data bus lines should not be run between the  $V_{DD}$  and  $V_{SS}$  supply lines near the H6061 without ground-plane shielding. Tracks from components to pin RC must be kept very short. Pin RC if left free should be shielded with a ground ring in noisy environments.

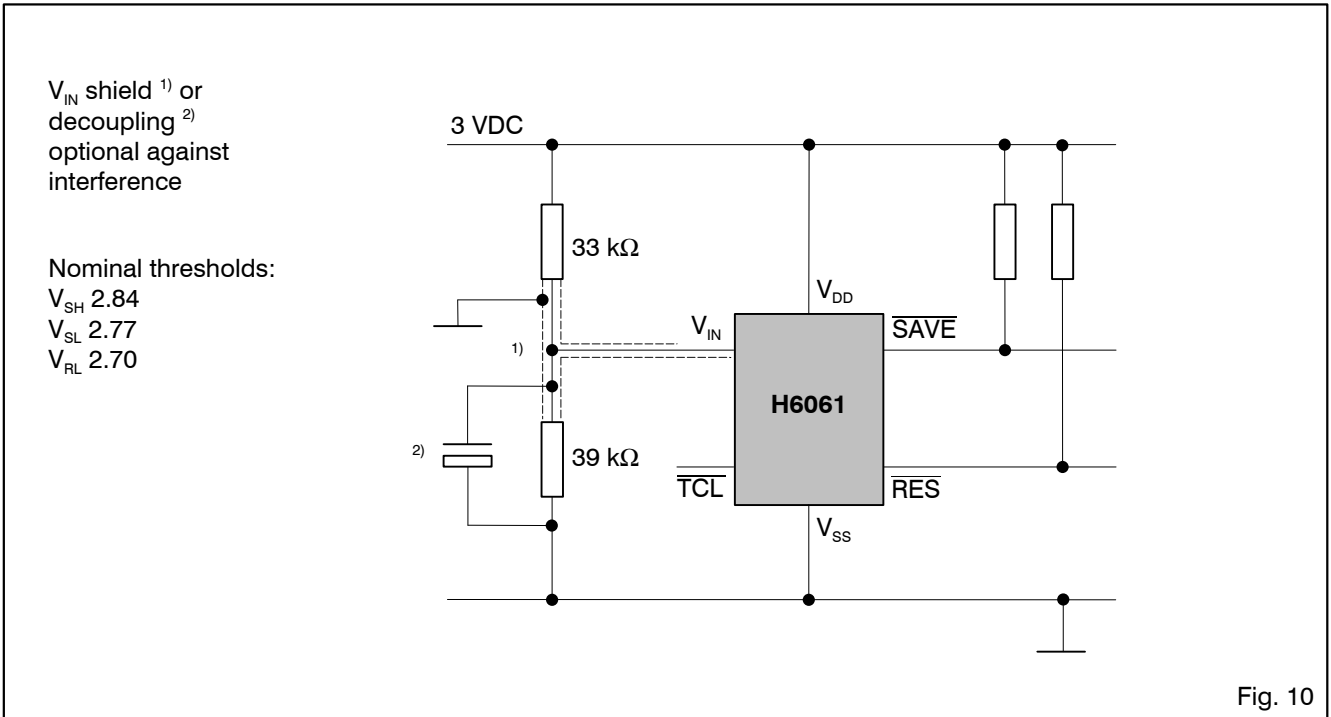
The H6061 has only 40 mV hysteresis specially for monitoring regulated DC. Pin  $V_{IN}$  must be protected from any significant mains ripple or RFI (see Fig. 10). It should be placed as near as possible to the point where voltage is to be monitored. Pin  $V_{IN}$  is protected by an

internal resistor (nominal 15 k $\Omega$ ) against voltages in excess of  $V_{DD}$ . In some environments this may however pick up enough mains ripple or RFI to distort the voltage detection thresholds or even cause unwanted sporadic resets in the absence of adequate shielding or filtering on  $V_{IN}$ .

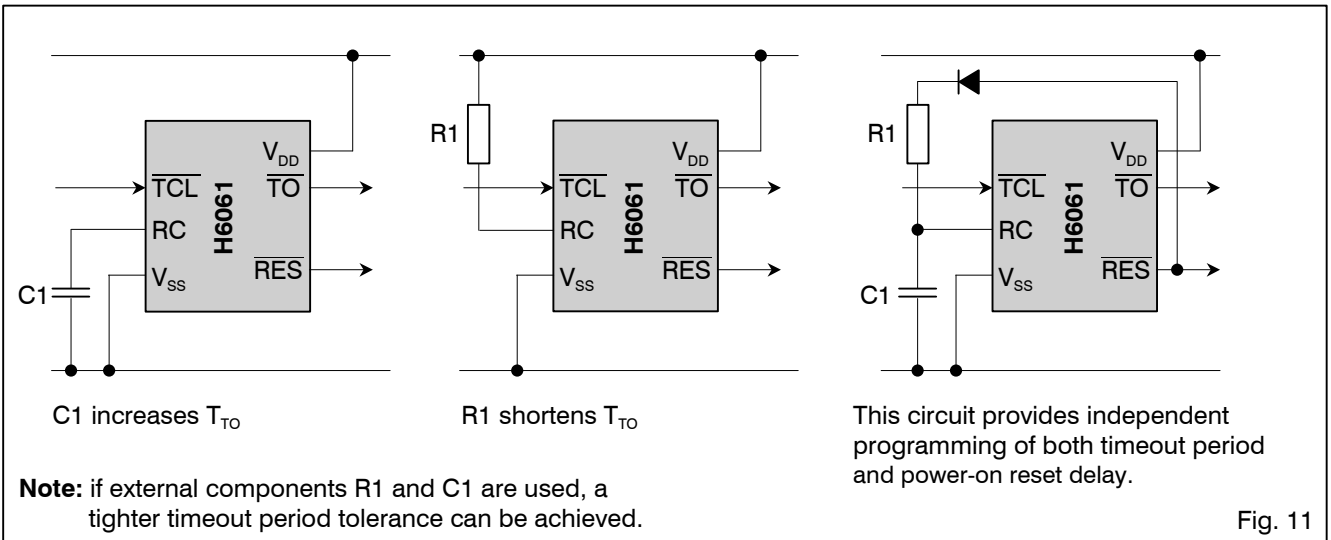
The H6061 has sufficient immunity to ripple and interference on the  $V_{DD}$  supply line, but if it is important that a system meet severe criteria for injected spikes and RFI, then care must be taken also decouple  $V_{DD}$  from these influences, as system protection must continue even under these conditions. With normal series voltage regulators, the regulated 5 VDC output voltage follows the DC rough voltage within 1.5 V on powering up. If the application has pin  $V_{IN}$  monitoring the DC rough, the internal inputs to the on-chip comparators will not rise above  $V_{DD}$  if the H6061 is correctly programmed. With switched-mode power supplies however, the DC-rough voltage on power-up rises almost to its working level before the 5 VDC line starts to ramp up. The H6061 has been specially designed to work under these extreme conditions but care must be taken not to exceed absolute maximum ratings. In addition to the voltage monitoring on pin  $V_{IN}$ , a final protection is given by the H6061 monitoring its own  $V_{DD}$  supply. If a system malfunction causes  $V_{DD}$  to fall below  $V_{OFF}$  even though pin  $V_{IN}$  stays high, then all outputs go active at once.

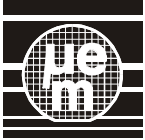


## Combined Supply Monitor, Initializer and Watchdog



## External Programming of RC Oscillator





# H6061

## Ordering Information

Industrial temperature range (-40 to +85 °C)

| Type <sup>1)</sup> | Package |
|--------------------|---------|
| H6061 25 8P        | DIP8    |
| H6061 25 8S        | SO8     |

Extended temperature range (-40 to +125 °C)

| Type         | Package |
|--------------|---------|
| H6061 25X 8P | DIP8*   |
| H6061 25X 8S | SO8*    |

\* Non-stock items  
Chip form on request

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