3-W Stereo Audio Power Amplifier with Advanced DC Volume Control

DESCRIPTOIN

The EUA6011A is a stereo audio power amplifier that drives 3 W/channel of continuous RMS power into a 3-Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

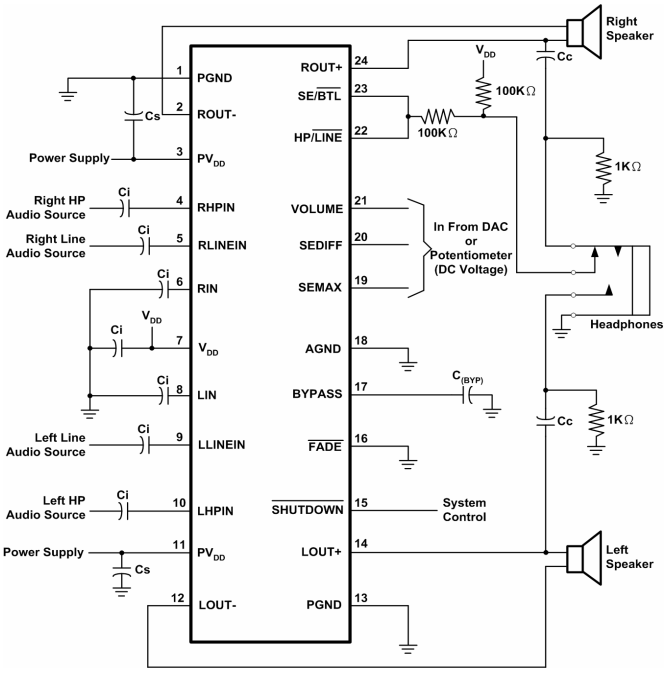
To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

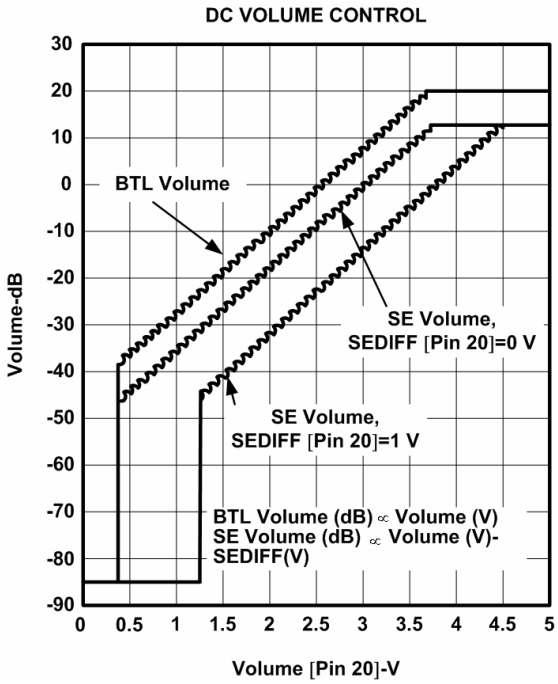
FEATURES

- Advanced DC Volume Control With 2-dB Steps From -40 dB to 20 dB
  - -Fade Mode
  - -Maximum Volume Setting for SE Mode
  - -Adjustable SE Volume Control Referenced to BTL Volume control
- 3 W into 3-Ω Speakers
- Stereo Input MUX
- Differential Inputs
- RoHS Compliant and 100% Lead (Pb)-Free

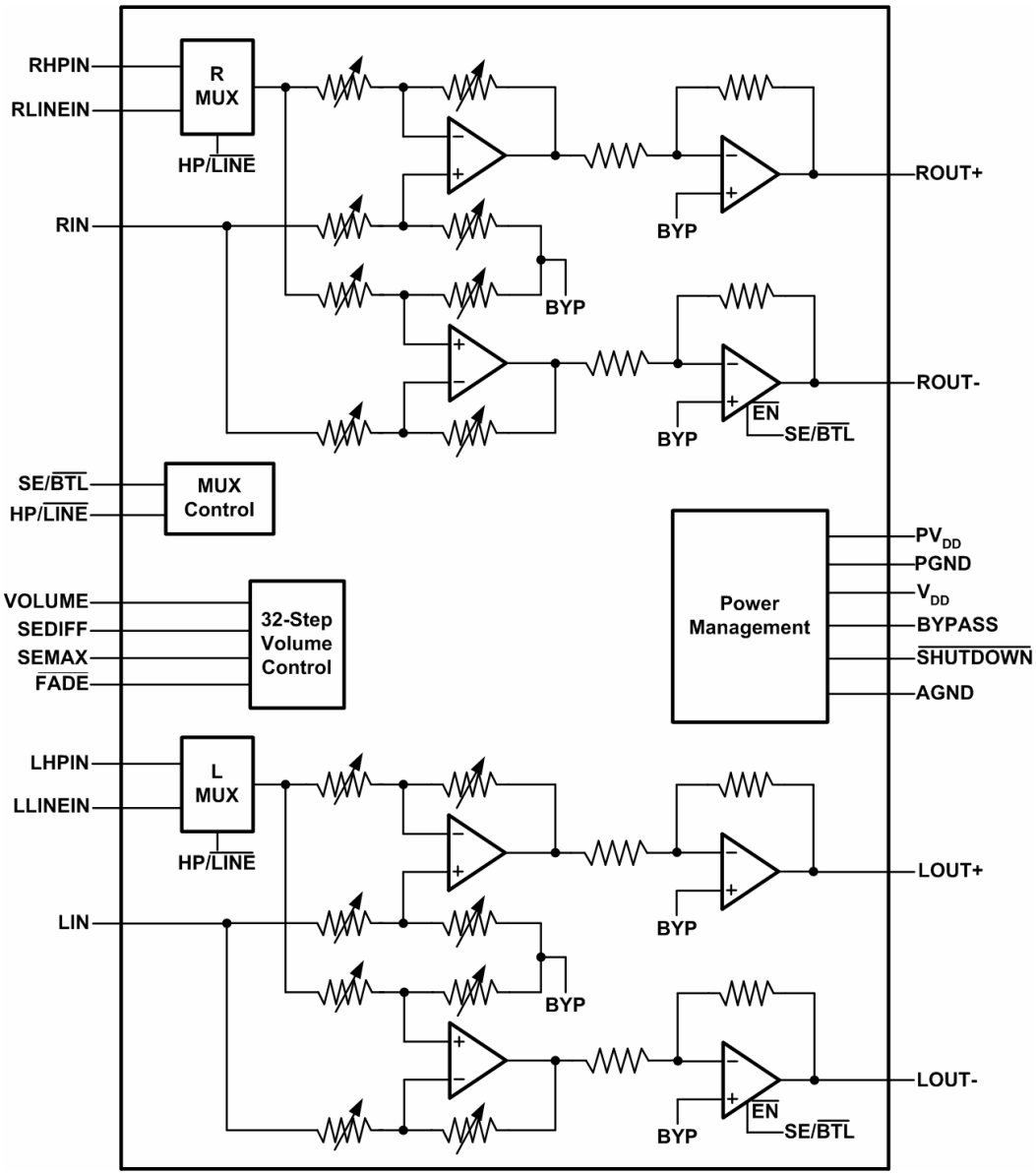
APPLICATIONS

- Notebook PC
- LCD Monitors
- Pocket PC





Block Diagram



Typical Application Circuit

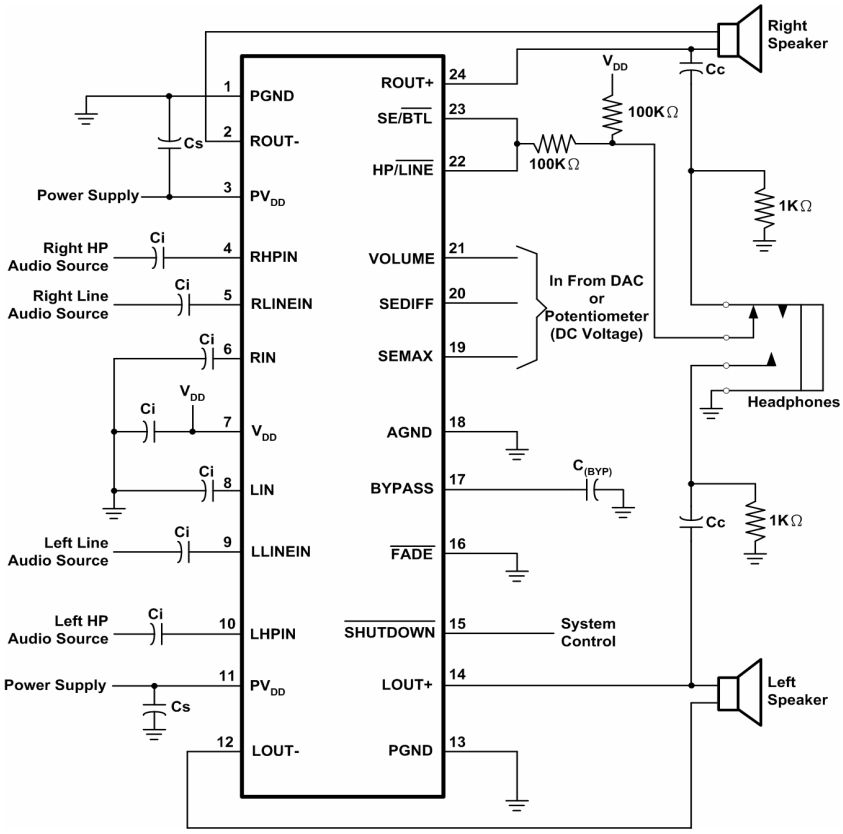


Figure 1. Application circuit using single-ended inputs and input MUX

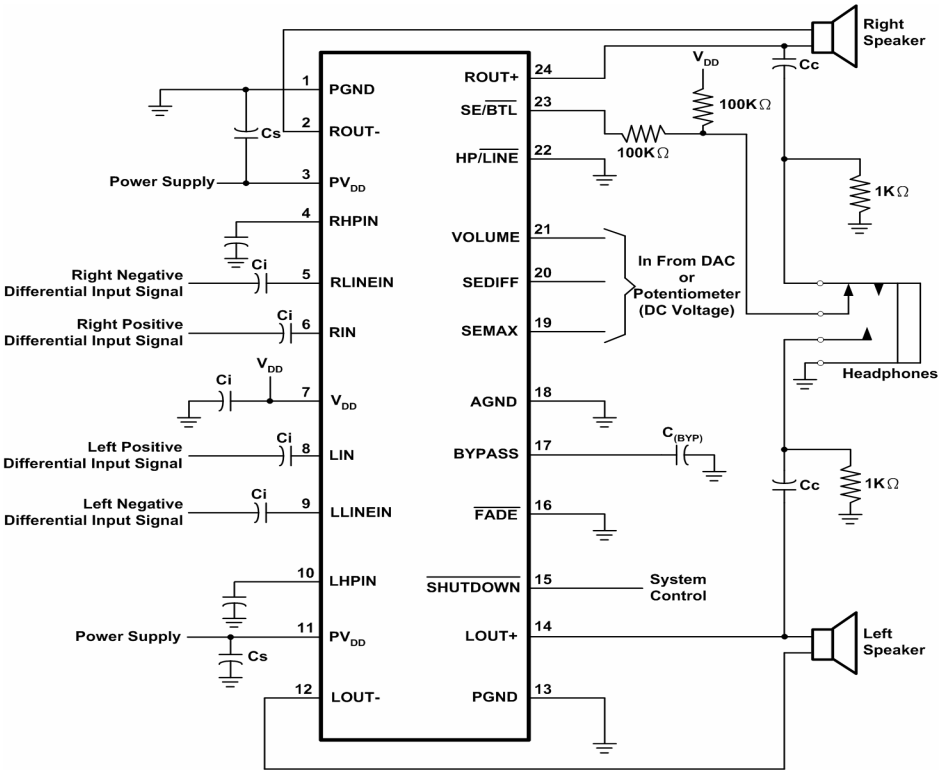
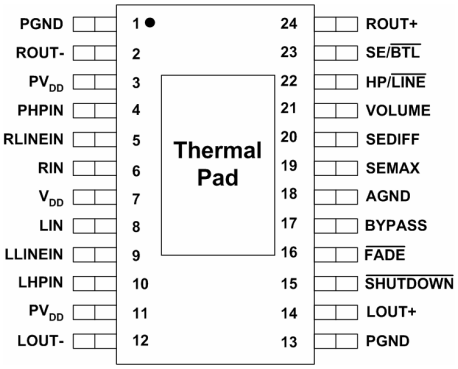


Figure 2. Application circuit using differential inputs

Pin Configurations

Package	Pin Configurations(Top View)
TSSOP-24 with a Thermal Pad exposure on the bottom of the package	

Pin Description

PIN	PIN	I/O	DESCRIPTION
PGND	1,13	-	Power ground
LOUT-	12	O	Left channel negative audio output
PV_{DD}	3,11	-	Supply voltage terminal for power stage
LHPIN	10	I	Left channel headphone input, selected when HP/$\overline{LINE}$ is held high
LLINEIN	9	I	Left channel line input, selected when HP/$\overline{LINE}$ is held low
LIN	8	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
V_{DD}	7	-	Supply voltage terminal
RIN	6	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
RLINEIN	5	I	Right channel line input, selected when HP/$\overline{LINE}$ is held low
RHPIN	4	I	Right channel headphone input, selected when HP/$\overline{LINE}$ is held high
ROUT-	2	O	Right channel negative audio output
ROUT+	24	O	Right channel positive audio output
$\overline{SHUTDOWN}$	15	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
$\overline{FADE}$	16	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal
BYPASS	17	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
AGND	18	-	Analog power supply ground
SEMAX	19	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to $V_{DD.}$
SEDIFF	20	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to $V_{DD.}$
VOLUME	21	I	Terminal for dc volume control. DC voltage range is 0 to $V_{DD.}$
HP/$\overline{LINE}$	22	I	Input MUX control. When logic high, RHPIN and LHPIN inputs are selected .When logic low, RLINEIN and LLINEIN inputs are selected.
SE/$\overline{BTL}$	23	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.
LOUT+	14	O	Left channel positive audio output.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA6011AQIR1	TSSOP 24	xxxx EUA6011A	-40 °C to 85°C
EUA6011AQIT1	TSSOP 24	xxxx EUA6011A	-40 °C to 85°C

EUA6011A □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape& Reel
T: Tube

Operating temperature range
I: Industry Standard

Package Type
Q: TSSOP

Absolute Maximum Ratings

- Supply voltage, V_{DD} ---------- 6V
- Input voltage, V_I ---------- –0.3 V to V_{DD} +0.3 V
- Continuous total power dissipation ---------- internally limited (see Dissipation Rating Table)
- Operating free-air temperature range, T_A ---------- –40°C to 85° C
- Operating junction temperature range, T_J ---------- –40°C to 150°C
- Storage temperature range, T_{stg} ---------- –65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance

  θ_{JA} (TSSOP) ---------- 87.9°C/W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		4	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$	$V_{DD}\times 0.8$		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{FADE}$		$V_{DD}\times 0.6$	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics at Specified Free-air Temperature, VDD = PVDD=5.5V, T_A = 25°C

Symbol	Parameter	Conditions	EUA6011A			Unit
			Min.	Typ.	Max.	
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	$V_{DD=}$ 5.5V,Gain=0 dB, SE/$\overline{BTL}$=0V			30	mV
		$V_{DD=}$ 5.5V,Gain=20 dB, SE/$\overline{BTL}$=0V			50	mV
PSRR	Power supply rejection ratio	V_{DD}= $PV_{DD=}$ 4 V to 5.5 V	-42	-70		dB
$\lvert I_{IH}\rvert$	High-level input current (SE/$\overline{BTL}$, $\overline{SHUTDOWN}$, $\overline{FADE}$, HP/$\overline{LINE}$,SEMAX, VOLUME,SEDIFF)	V_{DD}= $PV_{DD=}$5.5V, V_I= V_{DD} =PV_{DD}			1	µA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD}= $PV_{DD=}$5.5V, V_I= 0V			1	µA
I_{DD}	Supply current, no load	V_{DD}= $PV_{DD=}$5.5V, , SE/$\overline{BTL}$=0V, $\overline{SHUTDOWN}$ =2V	6	7.5	9	mA
		V_{DD}= $PV_{DD=}$5.5V, , SE/$\overline{BTL}$=5.5V $\overline{SHUTDOWN}$ =2V	3	5	6	
I_{DD}	Supply current, max power into a 3-Ω load	V_{DD}= $PV_{DD=}$5.5V, , SE/$\overline{BTL}$=0V, $\overline{SHUTDOWN}$ =2V,R_L=3Ω, Po=2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ =0V		1	20	µA

Operating Characteristics, VDD =PVDD= 5V, T_A = 25°C, R_L = 3Ω, Gain =6 dB

Symbol	Parameter	Conditions		EUA6011A			Unit
				Min.	Typ.	Max.	
P_O	Output power	THD=1%, f=1kHz			2		W
		THD=10%, f=1kHz,V_{DD}=5.5V			3		
THD+N	Total harmonic distortion plus noise	P_O=1W, R_L=8Ω,f=1 kHz			<0.4%		
V_{OH}	High-level output voltage	R_L=8Ω,Measured between output and V_{DD}				700	mV
V_{OL}	Low-level output voltage	R_L=8Ω,Measured between output and GND				400	mV
$V_{(Bypass)}$	Bypass voltage (Nominally V_{DD}/2)	Measured at pin 17,No load, V_{DD}=5.5V		2.65	2.75	2.85	V
B_{OM}	Maximum output power bandwidth	THD=5%			＞20		kHz
	Supply ripple rejection ratio	f =1kHz,Gain=0 dB $C_{(BYP)}$=0.47μF	BTL mode		-63		dB
			SE mode		-57		dB
	Noise output voltage	f=20 Hz to 20 kHz, Gain=0 dB, $C_{(BYP)}$=0.47μF,	BTL mode		36		μV_{RMS}
Z_I	Input impedance (see Figure 25)	VOLUME=5 V			14		kΩ

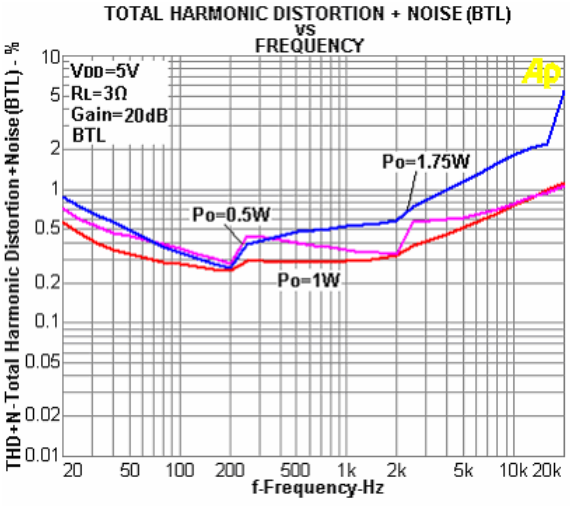
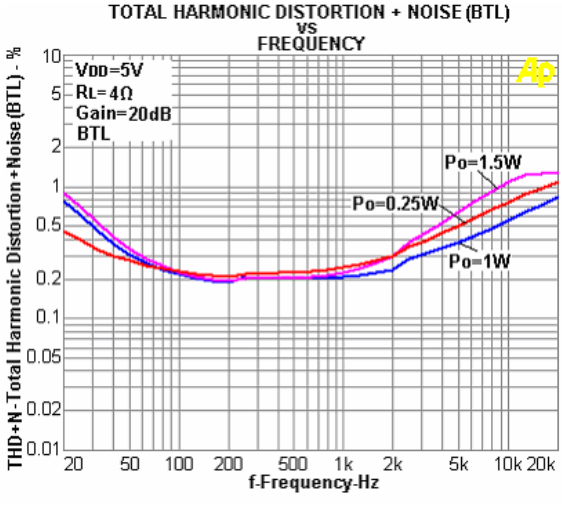


Figure 3



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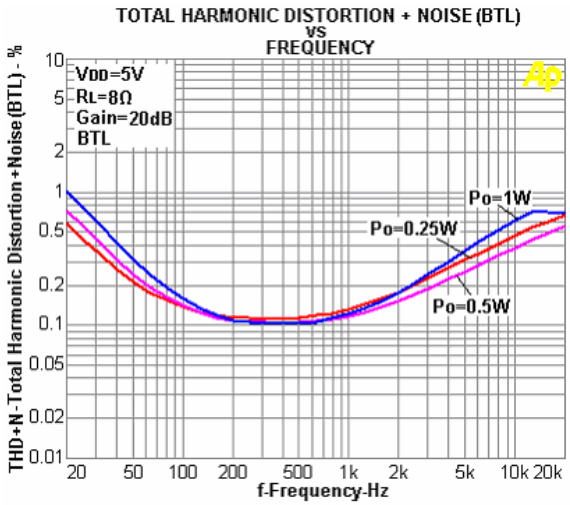

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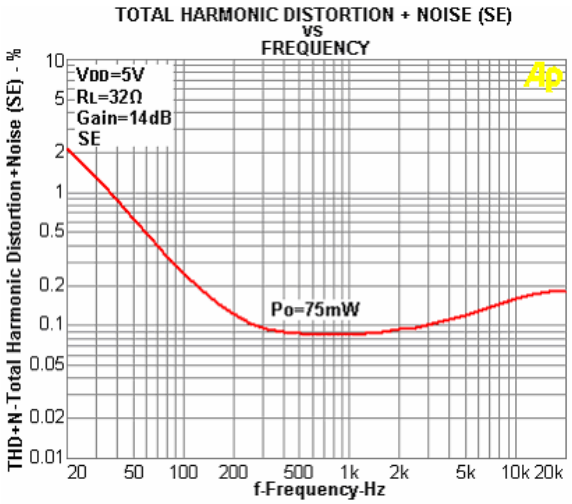

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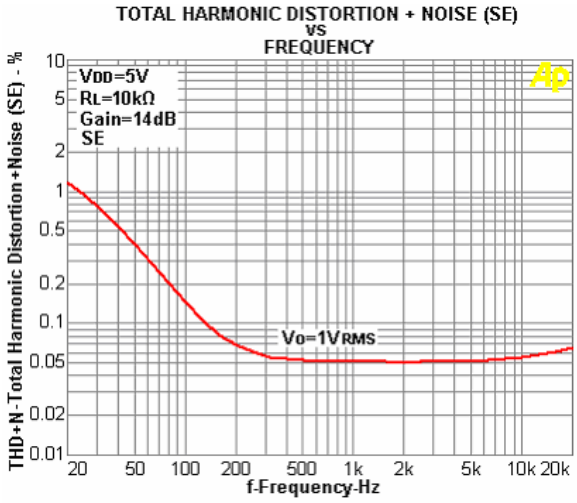

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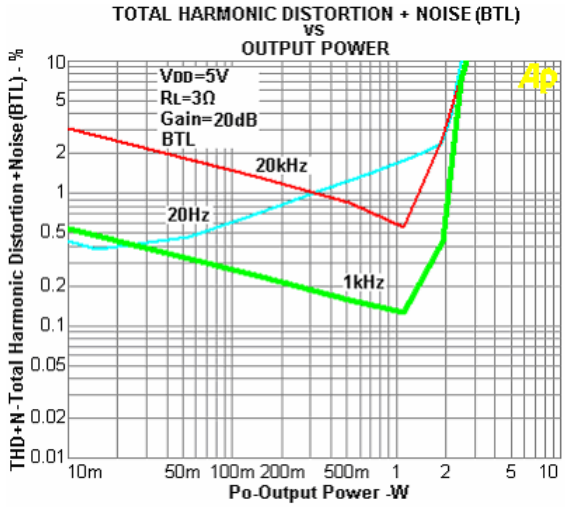

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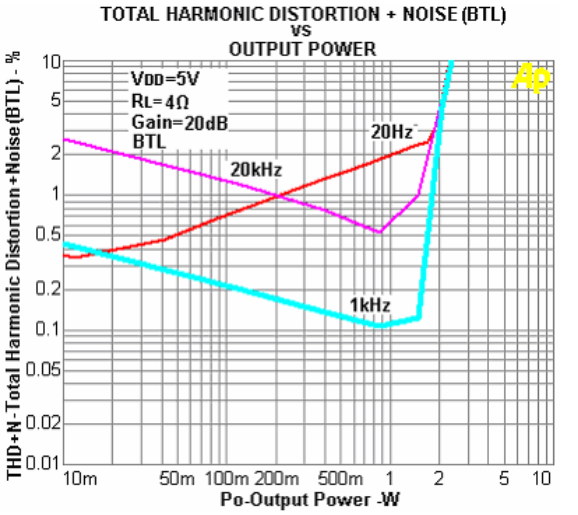

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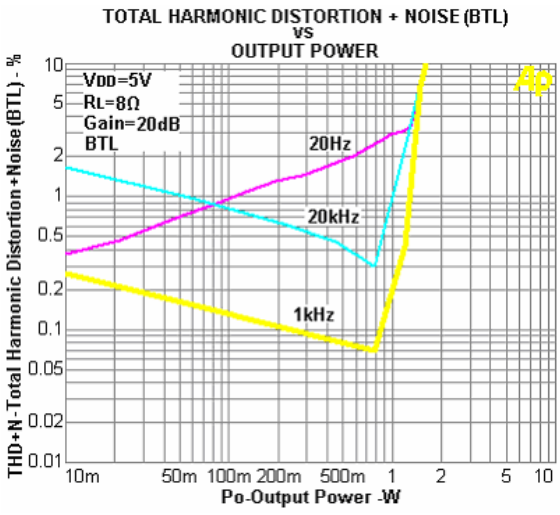

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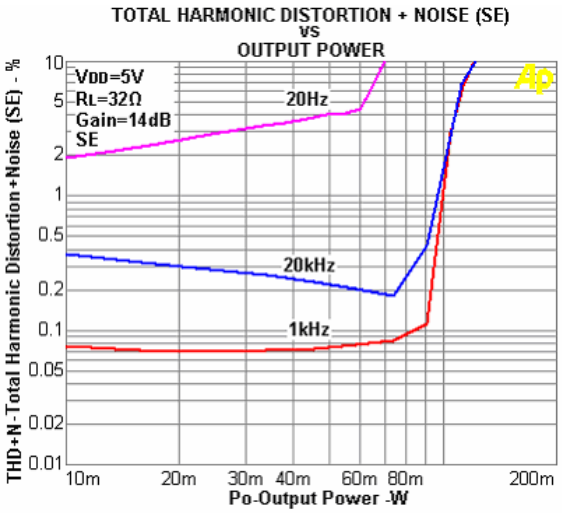

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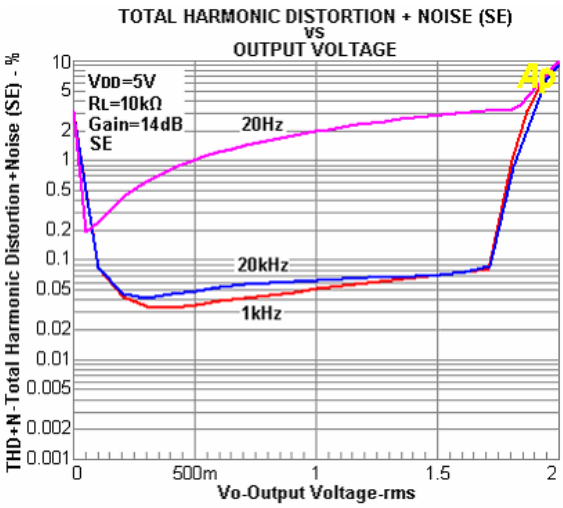

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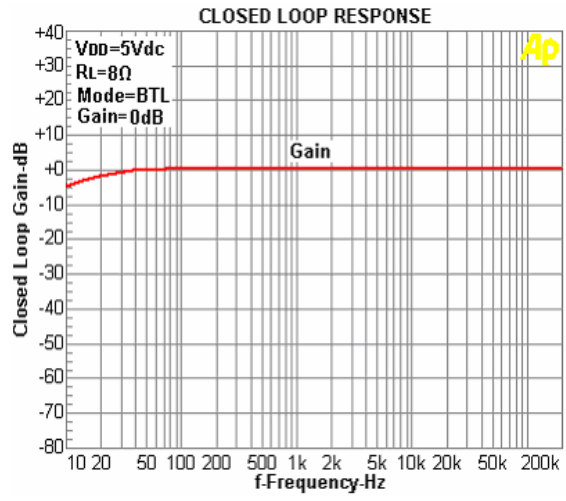

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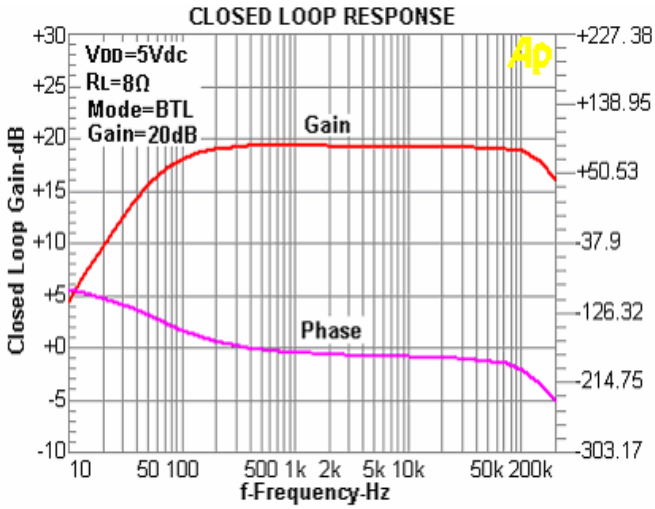
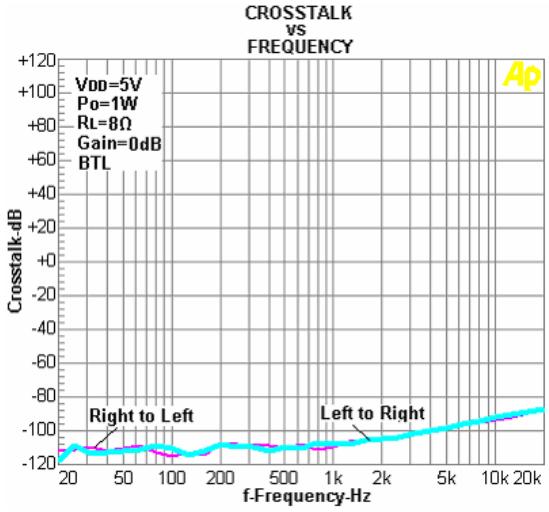


Figure 14



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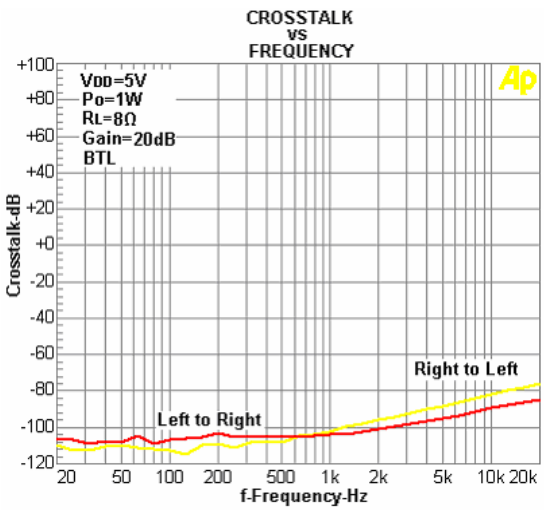

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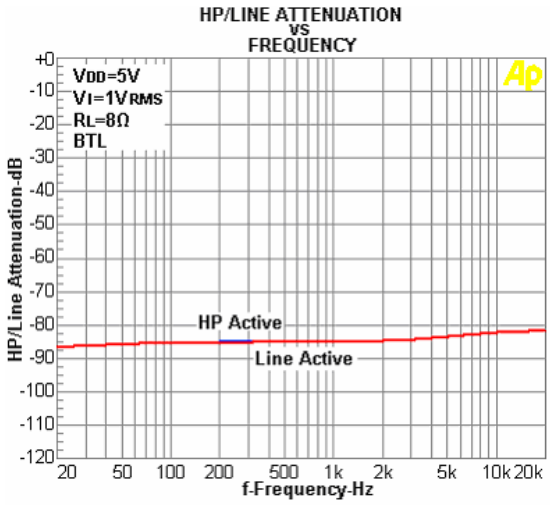

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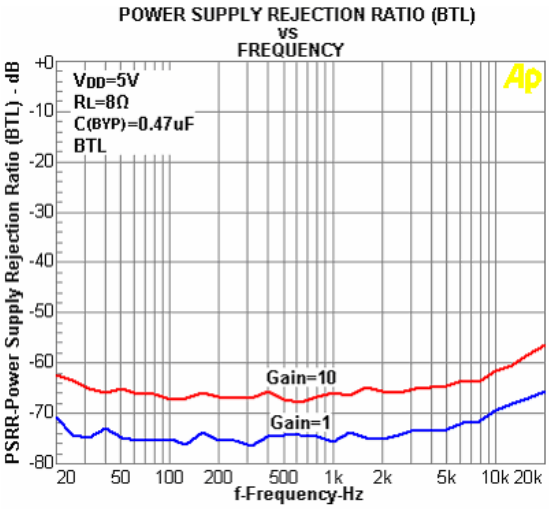

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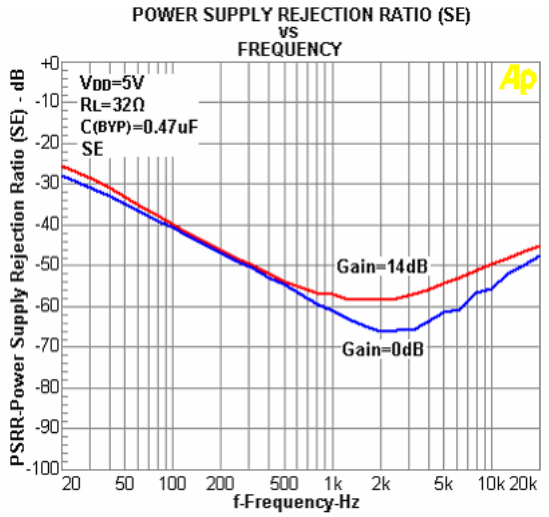

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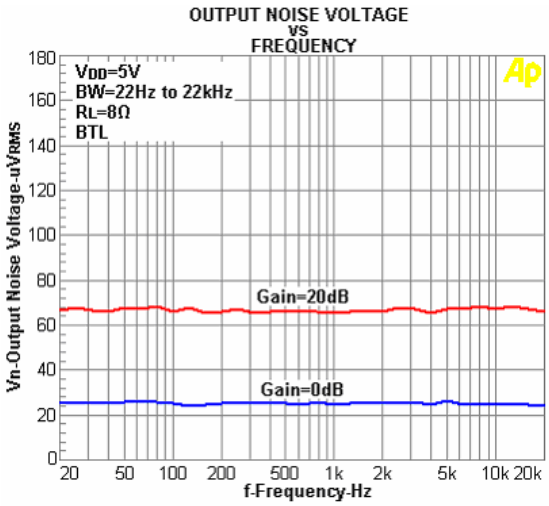

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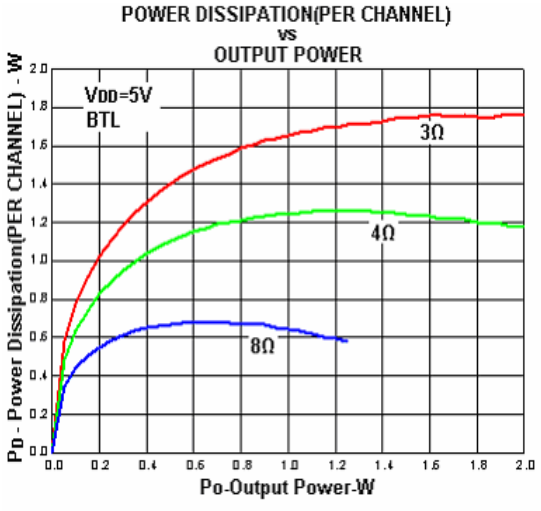

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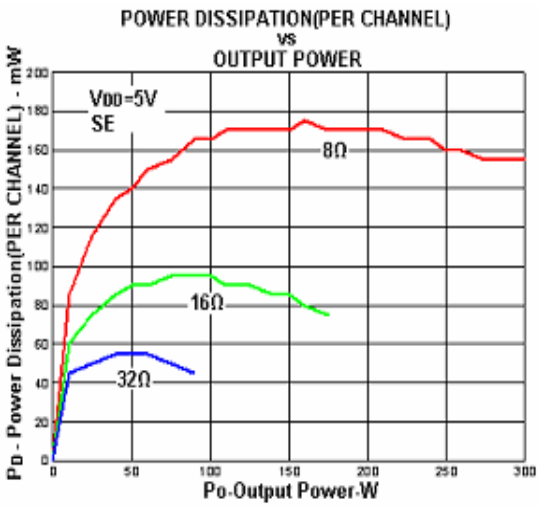

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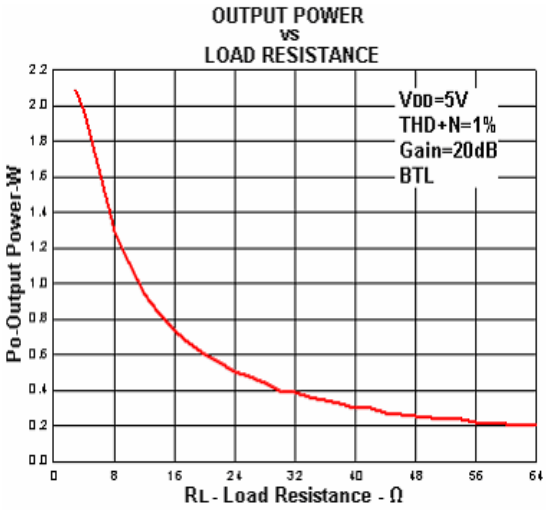

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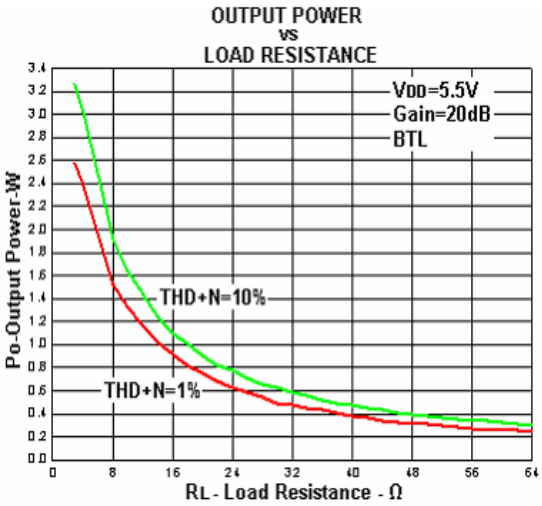


Figure 24

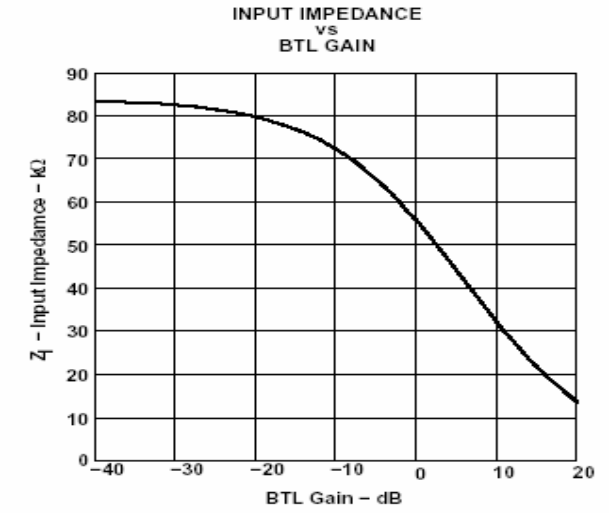


Figure 25

Application Information

Table 1. DC Volume Control (BTL Mode, V_{DD}=5V)(1)

VOLUME(PIN21)		
From(V)	To(V)	Gain of amplifier (dB)
0.00	0.26	-85(2)
0.33	0.37	-40
0.44	0.48	-38
0.56	0.59	36
0.67	0.70	-34
0.78	0.82	-32
0.89	0.93	-30
1.01	1.04	-28
1.12	1.16	-26
1.23	1.27	-24
1.35	1.38	-22
1.46	1.49	-20
1.57	1.60	-18
1.68	1.72	-16
1.79	1.83	-14
1.91	1.94	-12
2.02	2.06	-10
2.13	2.17	-8
2.25	2.28	-6(2)
2.36	2.39	-4
2.47	2.50	-2
2.58	2.61	0
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20(2)

(1)For other values of V_{DD} ,scale the voltage values in the table by a factor of V_{DD}/5.
(2)Tested in production. Remaining gain steps are specified by design.

Table 2. DC Volume Control (SE Mode, V_{DD}=5V) (1)

VOLUME=VOLUME-SEDIFF or SEMAX		
From(V)	**To(V)**	**Gain of amplifier (dB)**
0.00	0.26	-85(2)
0.33	0.37	-46
0.44	0.48	-44
0.56	0.59	-42
0.67	0.70	-40
0.78	0.82	-38
0.89	0.93	-36
1.01	1.04	-34
1.12	1.16	-32
1.23	1.27	-30
1.35	1.38	-28
1.46	1.49	-26
1.57	1.60	-24
1.68	1.72	-22
1.79	1.83	-20
1.91	1.94	-18
2.02	2.06	-16
2.13	2.17	-14
2.25	2.28	-12
2.36	2.39	-10
2.47	2.50	-8
2.58	2.61	-6(2)
2.70	2.73	-4
2.81	2.83	-2
2.92	2.95	0(2)
3.04	3.06	2
3.15	3.17	4
3.26	3.29	6(2)
3.38	3.40	8
3.49	3.51	10
3.60	3.63	12
3.71	5.00	14

(1)For other values of V_{DD} ,scale the voltage values in the table by a factor of V_{DD}/5.
(2)Tested in production. Remaining gain steps are specified by design.

VOLUME,SEDIFF, and SEMAX Operation

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD} =5V. For a different $V_{DD,}$ the values in the table scale linearly. If $V_{DD=}$4V , multiply all the voltages in the table by 4 V/5V, or 0.8.

The EUA6011A allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin,. When SEDIFF =0V, the difference between the BTL gain and the SE gain is 6dB. Refer to the section labeled bridged-tied load versus single-ended load for an explanation on why the gain in BTL mode is 2x that of single-ended mode, or 6DB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20dB , the gain in the headphone channel is fixed at 14dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode. The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 26. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD} =5V**.** The values must be scaled for other values of $V_{DD.}$

Table 1 and Table 2 show a range of voltages for each gain step . There is a gap in the voltage between each gain step . This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate form one gain step to another . If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain actually changes , is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be through of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing .If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 27.The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

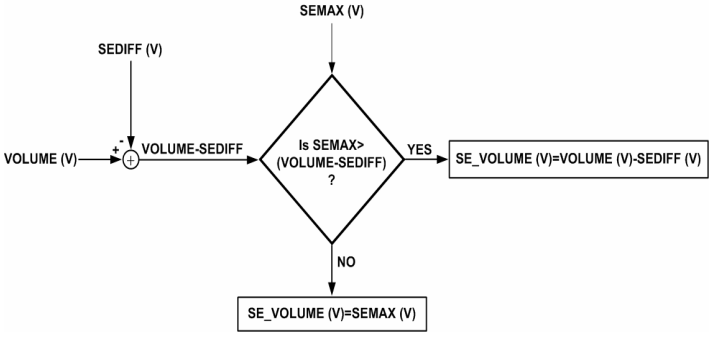


Figure 26. Block diagram of SE Volume Control

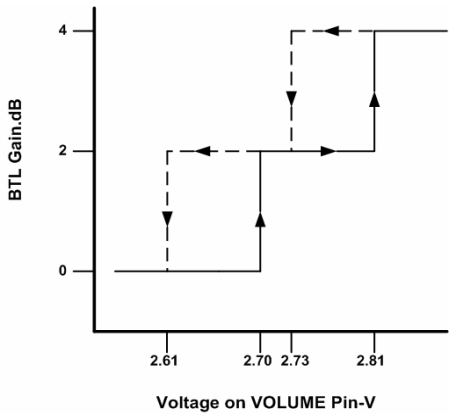


Figure 27. DC Volume Control Operation

HP/$\overline{\text{LINE}}$ Operation

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX).Refer to the block diagram in Figure 30.This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/$\overline{\text{BTL}}$ pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.

When this input is logic high, the RHPIN and LHPIN inputs are selected .when this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 4 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the recommended operation conditions table.

Shutdown Modes

The EUA6011A employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD}<1μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 3 . HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Function

Inputs			Amplifier State	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

X= Do not care

$\overline{\text{FADE}}$ Operation

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (VIL) or logic high (VIH) can be found in the recommended operating conditions table.

When a logic low is applied to the $\overline{\text{FADE}}$ pin and a logic low is then applied on the $\overline{\text{SHUTDOWN}}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58HZ,this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached .The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps , and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of VDD/2 to ground.

This time is dependent on the value of the bypass capacitor. For a 0.47-μF capacitor that is used in the application diagram in Figure 1, the time is approximately 500ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-μF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-μF capacitor, or 1 second. Figure 30 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at VDD when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process, the bypass capacitor will begin charging. Once the bypass voltage reaches the final value of VDD/2 ,the gain increases in2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior the staring the shutdown sequence. The output of the amplifier immediately drops to VDD/2 and the bypass capacitor begins a smooth discharge to ground When shutdown is released, the bypass capacitor charges up to VDD/2 and the channel gain returns immediately to the value stored in memory. Figure 31 below is a waveform captured at the output during the shutdown sequence when

the part is in the fade-off mode. The gain is set to the highest level, and the output is at VDD when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the pin does not change the power-up sequence. Upon a power-up condition, the EUA6011A begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF , and SEMAX pins.

Bridged-Tied Load Versus Single-Ended Mode

Figure 28 show a Class-AB audio power amplifier (APA) in a BTL configuration. The EUA6011A BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2\times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance(see equation 1)

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad \text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad \text{------(1)}$$

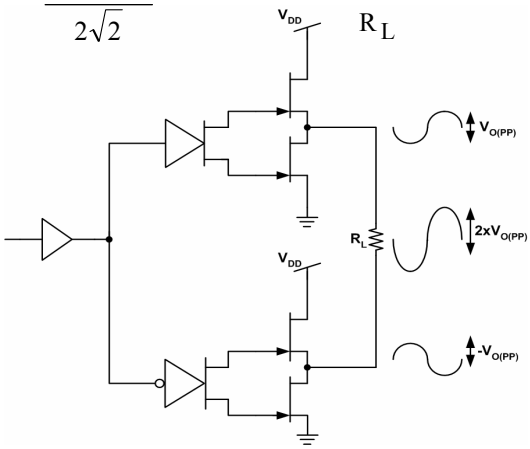


Figure 28.Bridge-Tied Load configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 29.

A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_C = \frac{1}{2\pi R_L C_C} \text{----------(2)}$$

For example, a 68µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

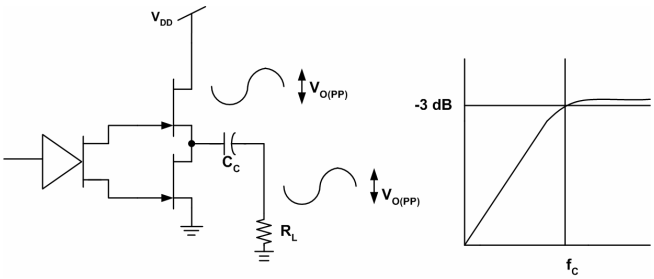


Figure 29. Single-Ended configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 X the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section**.**

Single-Ended Operation

In SE mode the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4). The amplifier switches single-ended operation when the SE/$\overline{BTL}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1V/V.

Input MUX Operation

The input MUX allows two separate inputs to be applied to the amplifier. This allow the designer to choose which input is active independent of the state of the SE/$\overline{BTL}$ terminal. When the HP/$\overline{LINE}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{LINE}$ terminal is held low, the line BTL inputs are active.

SE/$\overline{BTL}$ Operation

The ability of the EUA6011A to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the EUA6011A , two separate amplifiers drive OUT+ and OUT- .The SE/$\overline{BTL}$ input (terminal 15) control the operation of the follower amplifier that drives LOUT- and ROUT- (terminals 9 and 16).When SE/$\overline{BTL}$ is held low, the amplifier is on and the EUA6011A is in the BTL mode. When SE/$\overline{BTL}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the EUA6011A as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{BTL}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 30.

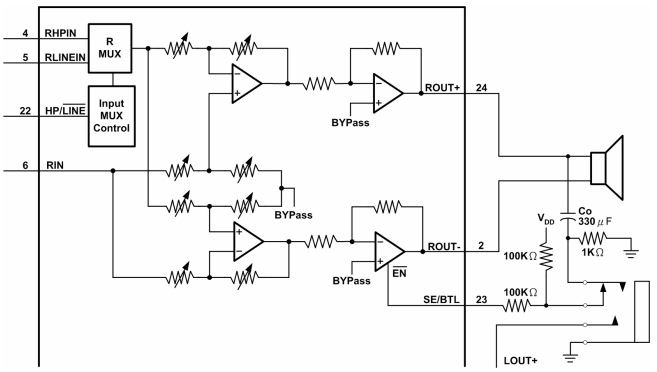


Figure 30. Resistor divider Network circuit 2

Using a readily available 1/8-in. (3.5mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ /1-kΩ divider pulls the SE/$\overline{BTL}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute(virtually open-circuits the speaker).The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

Input Resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a results, if a single capacitor is used in the input high-pass filter, the –3 dB or cut-off frequency will also change by over 6 times.

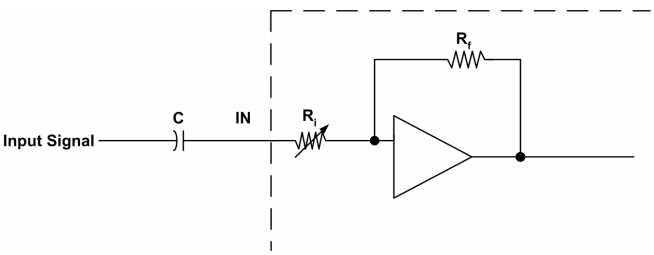


Figure 31. Input Resistor

The-3dB frequency can be calculated using equation 3:

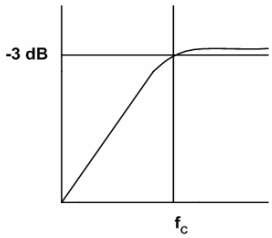
$$f_{-3dB} = \frac{1}{2\pi C (R \parallel R_i)} \quad \text{---------- (3)}$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier, Z_i, from a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi Z_i C_i} \text{----------(4)}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 70kΩ and the specification calls for a flat bass response down to 40Hz. Equation 2 is reconfigured as equation 5.

$$C_i = \frac{1}{2\pi Z_i f_C} \text{----------(5)}$$

In this example, C_i is 56nF so one would likely choose a value in the range of 56nF to 1µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low- leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor, (C_S)

The EUA6011A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between
the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

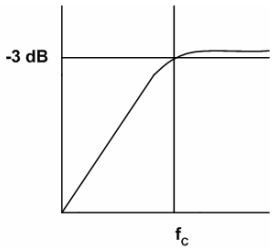
Bypass Capacitor, (C_B)

The bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. Bypass capacitor, C_B, values of 0.47µF to 1µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Output Coupling Capacitor, (C_C)

For general signal-supply SE configuration, the output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 6.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \text{ ----------(6)}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a
C_C of 330µF is chosen and loads vary from 3Ω, 4Ω, 8Ω, 32Ω, 10kΩ, to 47kΩ. Table 3 summarizes the frequency response characteristics of each configuration.

Table4. Common Load Impedances vs Low Frequency Output characteristics in SE Mode

R_L	C_C	Lowest Frequency
3Ω	330µF	161Hz
4Ω	330µF	120Hz
8Ω	330µF	60Hz
32Ω	330µF	15Hz
10000Ω	330µF	0.05Hz
47000Ω	330µF	0.01Hz

As Table 4 indicates, most of the bass response is attenuated into a 4-Ω load and 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Using Low- ESR Capacitors

Low- ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

Thermal Pad Considerations

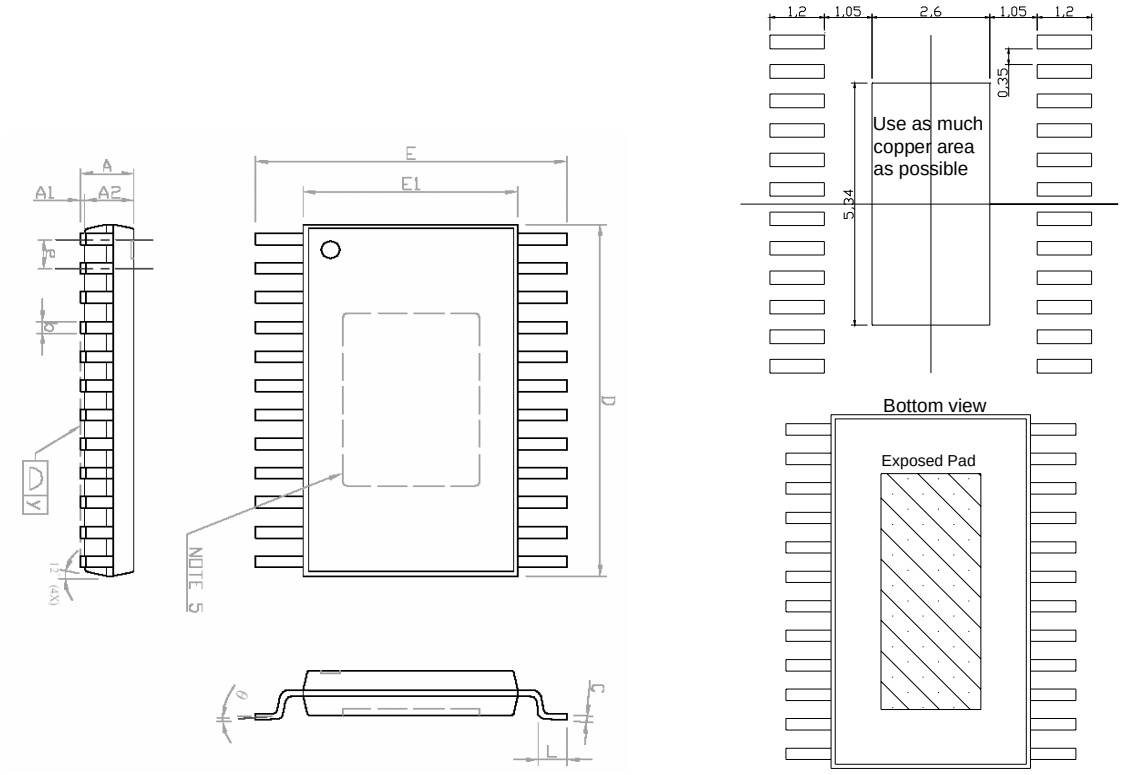
The thermal pad must be connected to ground. The package with thermal pad of the EUA6011A requires special attention on thermal design. If the thermal design issues are not properly addressed, the EUA6011A will go into thermal shutdown when driving a heavy load.

The thermal pad on the bottom of the EUA6011A should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25℃,a larger copper plane or forced-air cooling will be required to keep the EUA6011A junction temperature below the thermal shutdown temperature (150℃). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Package Information



NOTE

1. Package body sizes exclude mold flash protrusion or gate burrs
2. Tolerance ± 0.1mm unless otherwise specified
3. Coplanarity :0.1mm
4. Controlling dimension is millimeter.
5. Die pad exposure size is according to lead frame design.
6. Standard Solder Map dimension is millimeter.
7. Followed from JEDEC MO-15

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	------	------	1.15	------	------	0.045
A1	0.00	------	0.10	0.000	------	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	------	0.30	0.007	------	0.012
C	0.09	------	0.20	0.004	------	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	------	6.40	-----	------	0.252	------
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	------	0.65	-----	------	0.026	------
L	0.45	0.60	0.75	0.018	0.024	0.030
y	------	------	0.10	------	------	0.004
θ	0	------	8	0	------	8