Features

- 8Meg x 8 Organization
- CAS-before-RAS Refresh Capability
- RAS-only and Hidden Refresh Capability
- LVTTL (3.3V) Compatible Inputs and Outputs
- Early Write or Output Enable Controlled Write
- JEDEC Standard pinout
- 32 pin TSOP Type II package
- +3.3Volt ±0.3V Power Supply
- Industrial and Military Temperature Range

8Megx8 DRAM
Ruggedized Plastic

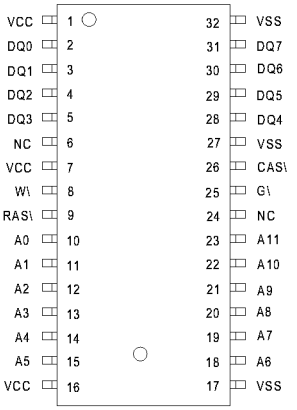
The EDI488MEV-RP is organized as an 8Megx8 bit Extended Data Out (EDO) Mode CMOS DRAM. The EDO mode offers high speed random access of memory cells within the same row.

The EDI488MEV-RP has CAS-before-RAS refresh and RAS-only refresh and Hidden refresh capabilities.

Pin Names

A0-A11	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
VCC	3.3V ±10%
VSS	Ground
NC	No Connection

Pinout



*FRAMM™ Technology produced under license from Dynamem, Inc.
Patent No. 5,224,023

Absolute Maximum Ratings*

Parameter	Rating
Voltage on any pin relative to VSS	-0.5 to +4.6V
Voltage on VCC supply relative to VSS	-0.5 to +4.6V
Industrial Temperature	-40 ℃ to +85 ℃
Military Temperature	-55 ℃ to +125 ℃
Storage Temperature	-40 ℃ to +125 ℃
Power Dissipation	1 Watt
Short Circuit Output Current	50mA

*Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(Voltages referenced to VSS, TA = 0 to 70 ℃)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Ground	VSS	0	0	0	V
Input High Voltage	VIH	2.4	-		V
Input Low Voltage	VIL	-0.3[2]	-	0.8	V

Notes: 1. 6.5V at pulse width ≤15ns which is measured at VCC.
2. -1.3V at pulse width ≤15ns which is measured at VSS.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Address)	CA	5	pF
Input Capacitance	CI	7	pF
Output Capacitance (DQ0)	CDQ	7	pF

DC and Operating Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Sym	Conditions	60ns		70ns		Units
			Min	Max	Min	Max	
Operating Current	ICC1*	RAS+CAS cycling @ tRC=min		140		120	mA
Standby Current	ICC2	RAS=CAS=W=VIH		2		2	mA
RAS-Only Refresh Current	ICC3*	CAS=VIH, RAS cycling @ TRC=min		140		120	mA
Hyper Page Mode Current	ICC4*	RAS=VIL,CAS, Address cycling @ TPC=min		130		110	mA
Standby Current	ICC5	RAS=CAS=W=VCC-0.2V		1		1	mA
CAS-Before-RAS Refresh Current	ICC6*	RAS and CAS cycling @ TRC=min		140		120	mA
Input Leakage Current	IIL	Any input 0<VIN<VCC+0.3V all other pins not under test = 0 Volts	-5	+5	-5	+5	µA
Output Leakage Current	IOL	Data out is disabled, 0V<VOUT<VCC	-5	+5	-5	+5	µA
Output High Voltage Level	VOH	IOH=-2mA	2.4		2.4		V
Output Low Voltage Level	VOL	IOL = 2mA		0.4		0.4	V

* Note: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3, and ICC6, address can be changed maximum once while RAS=VIL. In ICC4, address can be changed maximum once within one fast page mode cycle time, TPC.

AC Characteristics

(0 ℃-TA-70 ℃, See note 1,2)
(Test condition: VCC=3.3V±10%, VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V)

	Symbol	60ns		70ns			
Parameter		**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Random read or write cycle time	TRC	104		124		ns	
Read-modify-write cycle time	TRWC	138		165		ns	
Access time from $\overline{RAS}$	TRAC		60		70	ns	3,4,9
Access time from $\overline{CAS}$	TCAC		15		20	ns	3,4,10
Access time from column address	TAA		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	TCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	TCEZ	3	13	3	15	ns	5
$\overline{OE}$ to output in Low-Z	TOLZ	3		3		ns	3
Transition time (rise and fall)	TT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	TRP	40		50		ns	
$\overline{RAS}$ pulse width	TRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	TRSH	15		20		ns	
$\overline{CAS}$ hold time	TCSH	45		50		ns	
$\overline{CAS}$ pulse width	TCAS	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	TRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	TRAD	15	30	15	35	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	TCRP	5		5		ns	
Row address set-up time	TASR	5		5		ns	
Row address hold time	TRAH	10		10		ns	
Column address set-up time	TASC	5		5		ns	
Column address hold time	TCAH	10		15		ns	
Column address to $\overline{RAS}$ lead time	TRAL	35		40		ns	
Read command set-up time	TRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	TRCH	0		0		ns	7
Read command hold time referenced to$\overline{RAS}$	TRRH	0		0		ns	7
Write command hold time	TWCH	10		15		ns	
Write command pulse width	TWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	TRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	TCWL	15		20		ns	

See Notes on Page 4.

AC Characteristics

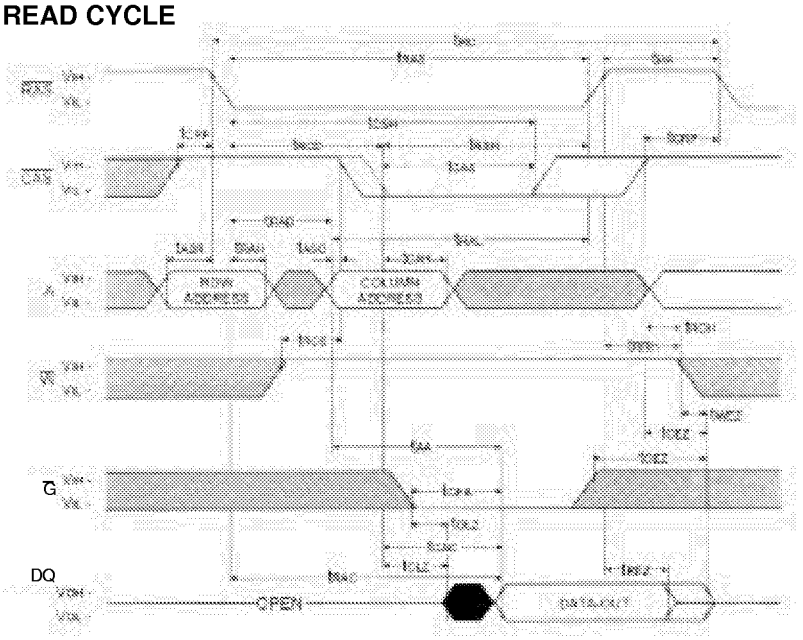
(0 ℃-TA-70 ℃, See note 1)
(Test condition (3V device): VCC=3.0V±10%, VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V)

	Symbol	60ns		70ns			
Parameter		**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Data set-up time	TDS	0		0		ns	8
Data hold time	TDH	10		15		ns	8
Refresh period (4K, 8K Normal)	TREF		64		64	ms	
Write Command set-up time	TWCS	0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	TCWD	32		39		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	TRWD	77		89		ns	6
Column address to $\overline{W}$ delay time	TAWD	47		54		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	TCPWD	54		64		ns	
$\overline{CAS}$ set-up time $\overline{CAS}$-before-$\overline{RAS}$ refresh	TCSR	10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	TCHR	10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	TRPC	5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}\overline{B}\overline{R}$ counter test cycle)	TCPT	20		30		ns	
Access time from $\overline{CAS}$ precharge	TCPA		35		40	ns	3
Hyper page cycle time	THPC	25		30		ns	
Hyper page read-modify-write cycle time	THPRWC	56		71		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	TCP	10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	TRASP	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	TRHCP	35		40		ns	
$\overline{OE}$ access time	TOEA		15		20	ns	
$\overline{OE}$ to data delay	TOED	13		15		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	TCPWD	54		64		ns	
Output buffer turn off delay from $\overline{OE}$	TOEZ	0	13	0	15	ns	
$\overline{OE}$ command hold time	TOEH	15		20		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	TWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	TWRH	10		10		ns	
Output data hold time	TDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	TREZ	3	15	3	20	ns	
Output buffer turn off delay from $\overline{W}$	TWEZ	3	15	3	20	ns	
$\overline{W}$ to data delay	TWED	15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	TOCH	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	TCHO	5		5		ns	
$\overline{OE}$ precharge time	TOEP	5		5		ns	
$\overline{W}$ pulse width (Hyper Page Mode)	TWPE	5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	TRASS	100		100		ns	
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh	TRPS	110		110		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	TCHS	-50		-50		ns	

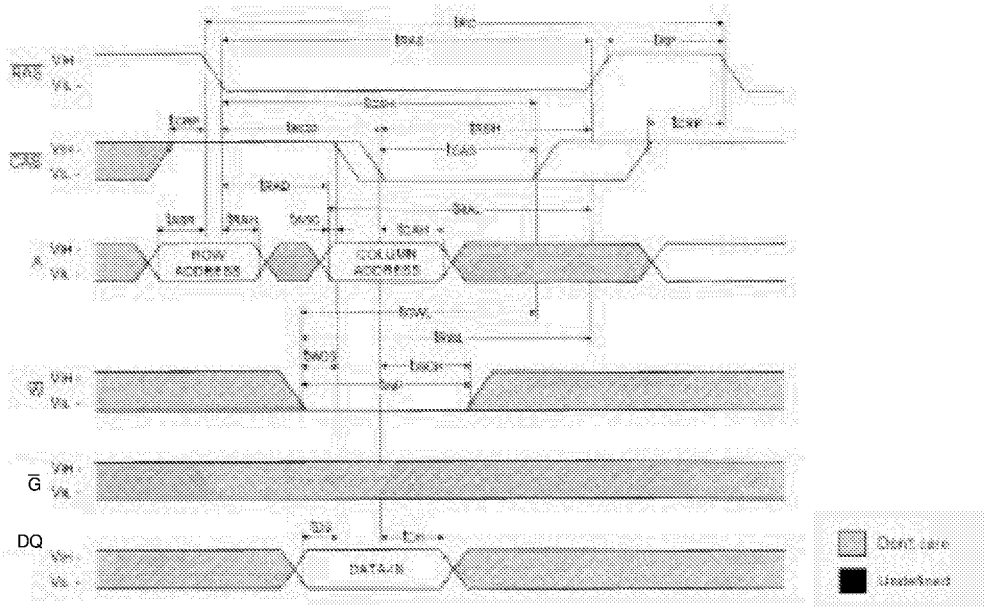
Notes:
1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load of equivalent to 2 TTL(5V device) loads and 100pF.
4. Operation within the TRCD(max) limit insures that TRAC(max) can be met. TRCD(max) is specified as a reference point only. If TRCD is greater than the specified TRCD(max) limit, then access time is controlled exclusively by TCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
6. TWCS, TRWD, TCWD, TAWD and TCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If TWCS≥TWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If TCWD≥TCWD(min), TRWD≥TRWD(min), TAWD≥TAWD(min) and TCPWD≥TCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either TRCH or TRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the TRAD(max) limit insures that TRAC(max) can be met. TRAD(max) is specified as a reference point only. If TRAD is greater than the specified TRAD (max) limit, then access time is controlled by TAA.
10. Assumes that TCRD≥TCRD (max).

Timing Diagrams

READ CYCLE

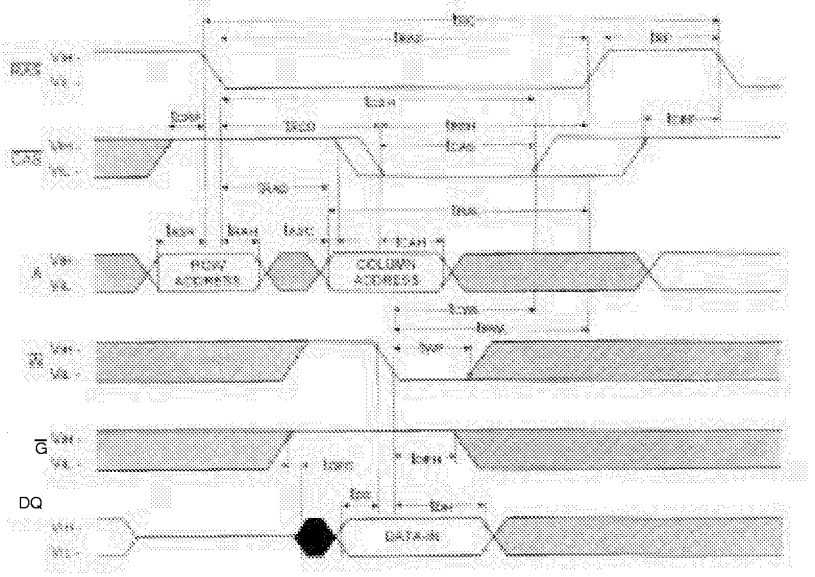


WRITE CYCLE (Early Write)

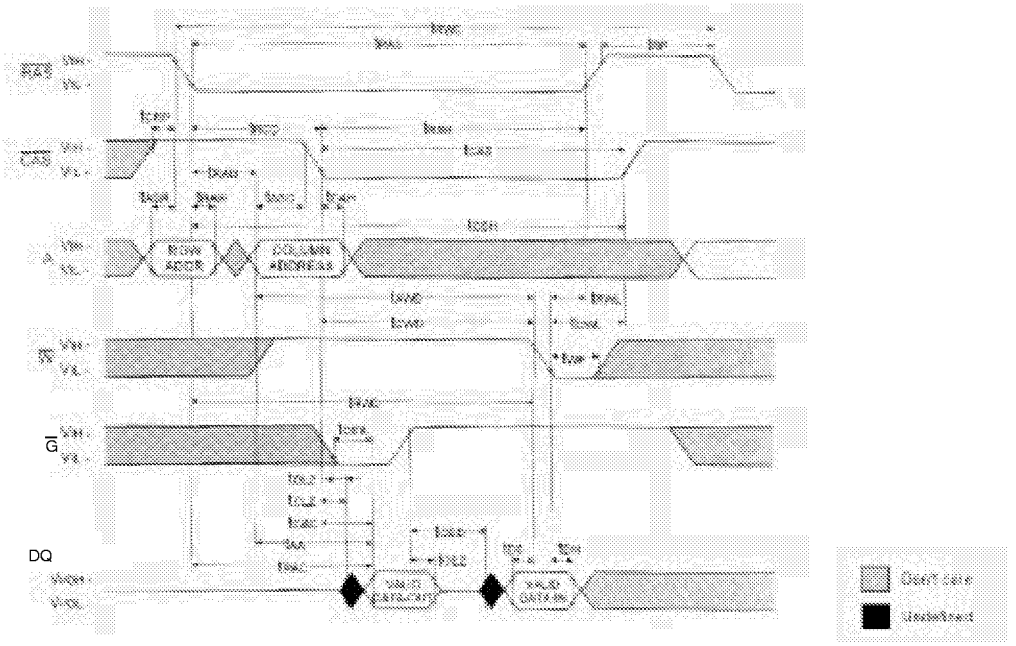


WRITE CYCLE ($\overline{OE}$ Controlled Write)

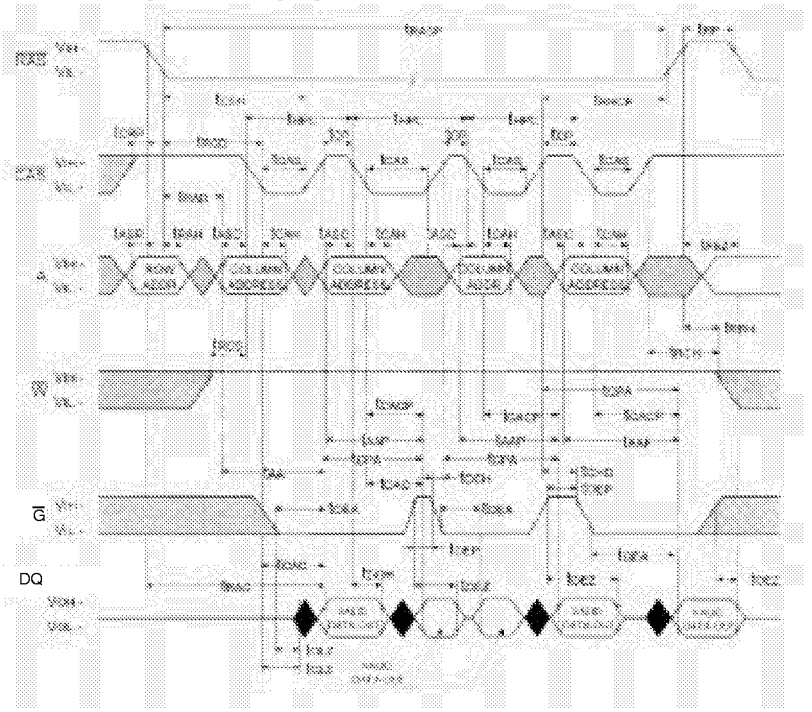
NOTE: DOUT=Open



READ - MODIFY - WRITE CYCLE

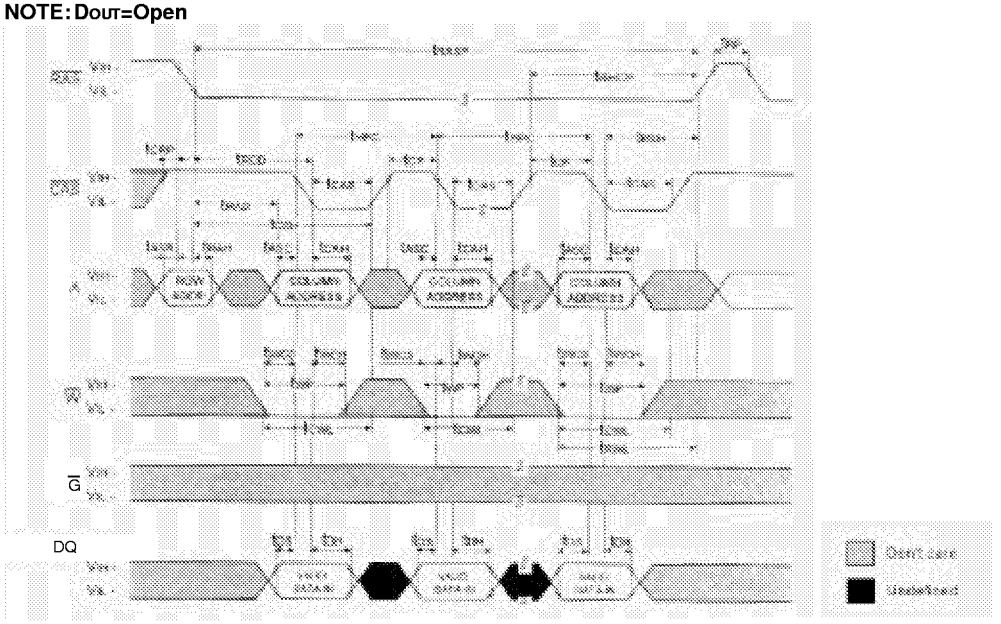


HYPER PAGE READ CYCLE

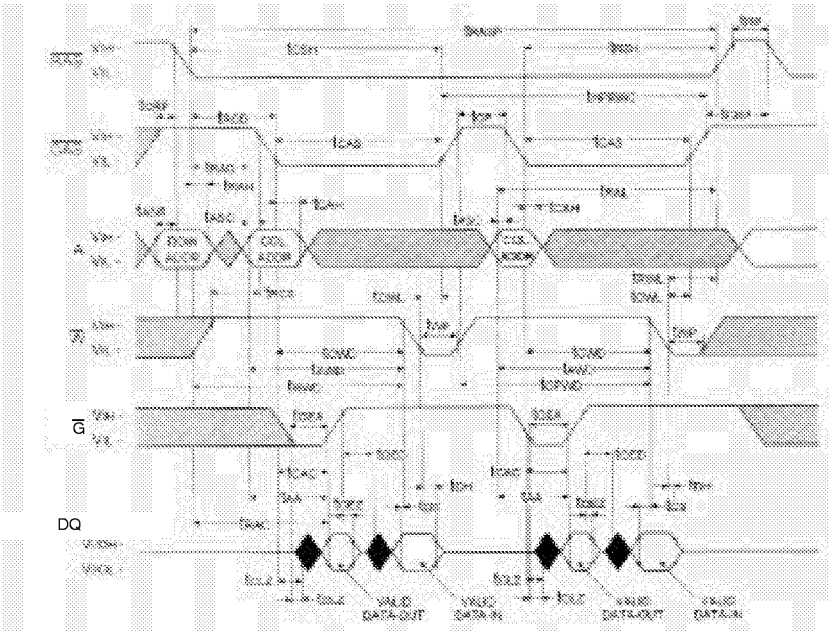


HYPER PAGE WRITE CYCLE (Early Write)

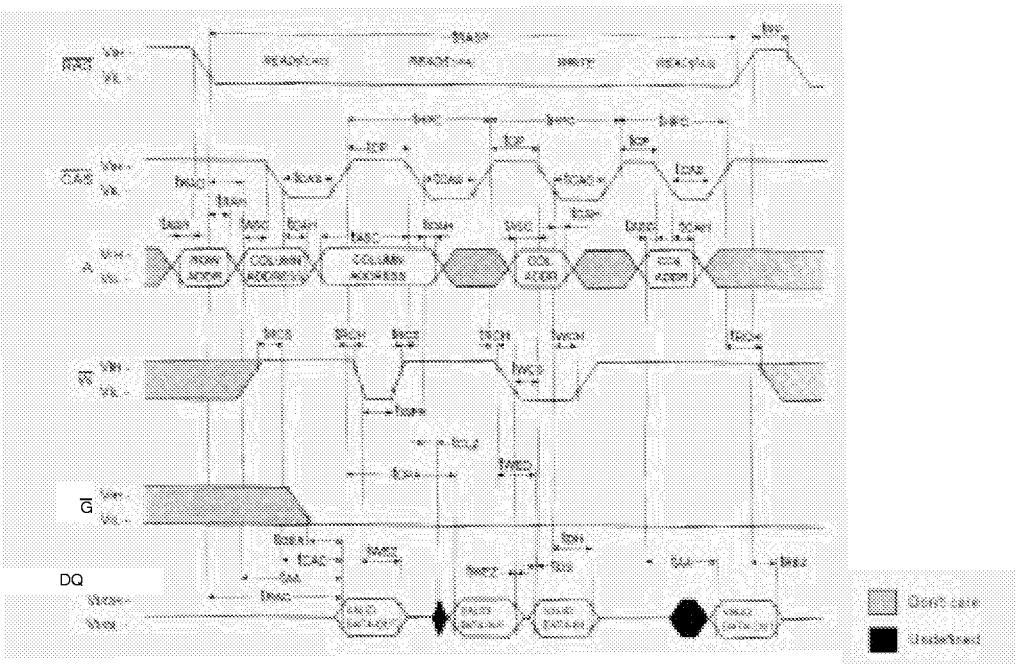
NOTE: DOUT=Open



HYPER PAGE READ - MODIFY - WRITE CYCLE

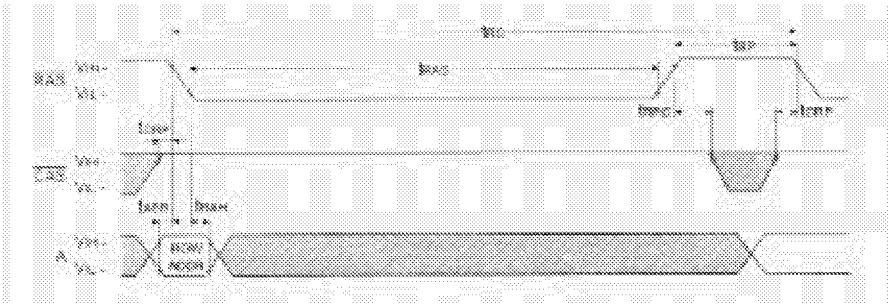


HYPER PAGE READ AND WRITE MIXED CYCLE



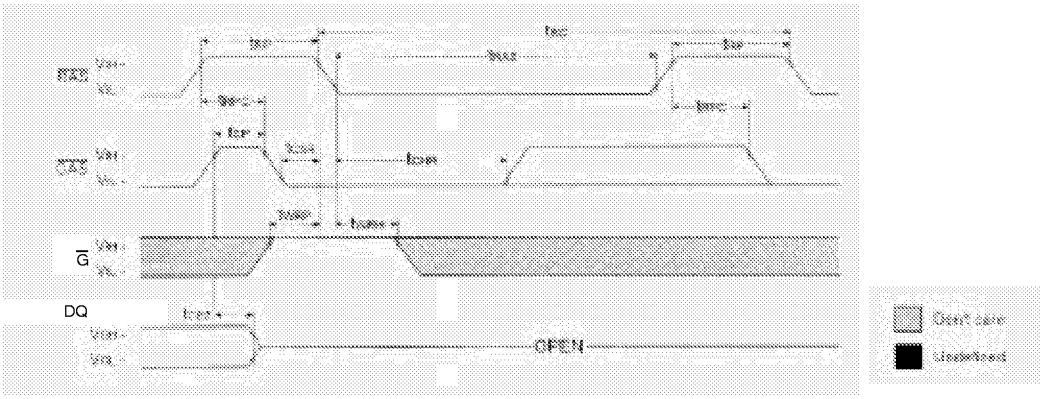
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{G}$, DIN=Don't Care
DOUT=Open

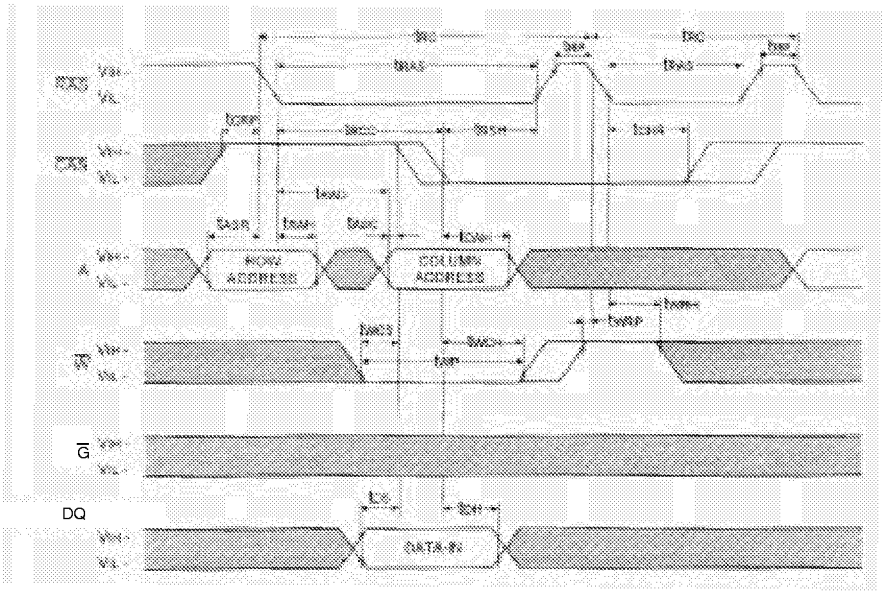


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{G}$, A=Don't Care

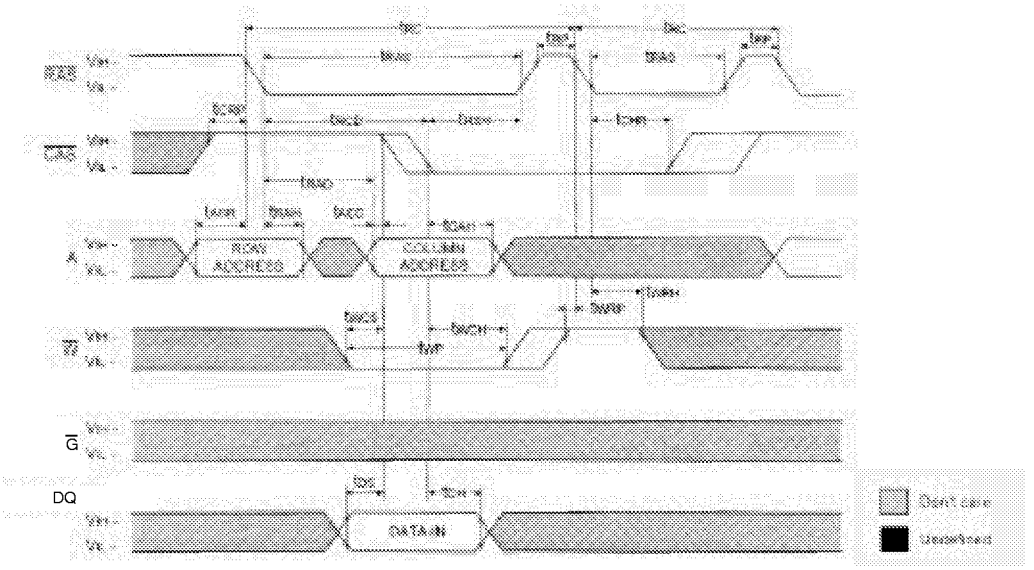


HIDDEN REFRESH CYCLE (Read)



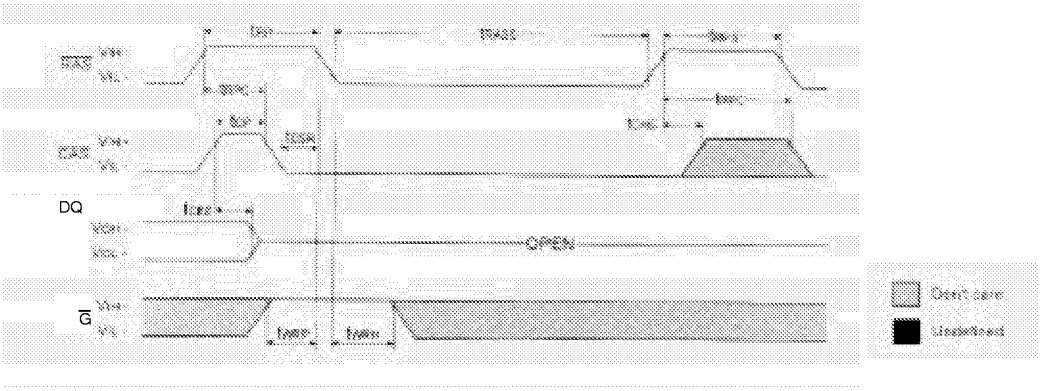
HIDDEN REFRESH CYCLE (Write)

DOUT=Open



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE: $\overline{\text{G}}$, A=Don't Care



Ordering Information

Part Number	Speed (ns)	Package No.	Temperature
EDI488MEV6SI	60	419	Industrial
EDI488MEV7SI	70	419	Industrial
EDI488MEV6SM	60	419	Military
EDI488MEV7SM	70	419	Military

Package Description

Package No. 419