DAC-7134B, DAC-7134U
14-Bit Microprocessor-compatible Multiplying D/A Converters

FEATURES

- 14-Bit linearity (0.003% FSR)
- Microprocessor-compatible with doubled-buffered inputs
- 3 Microsecond maximum output current settling time (0.9μS typical)
- Low power dissipation
- Full four-quadrant multiplication
- Gain Tempco of +/-8ppm/degree C maximum
- PROM-controlled correction circuits

GENERAL DESCRIPTION

The DAC-7134 achieves true 14-bit linearity by combining a four-quadrant, multiplying DAC with on-chip, PROM-controlled correction circuits. The DAC uses thin-film resistors and CMOS circuitry for stability while the PROM-controlled correction circuit eliminates errors introduced by the thermal stresses of packaging.

There are two versions of the DAC-7134, both represented by the block diagram, Figure 1. The DAC-7134U is programmed for unipolar operation while the DAC-7134B is programmed for bipolar applications. Microprocessor bus interfacing is easy using standard memory write cycle timing and control signals. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs.

There are two reference voltage inputs feeding the resistor ladder network. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder.

For unipolar use, the two reference inputs are tied together. For bipolar applications, the polarity of the MSB reference is reversed through an external operational amplifier. This flexibility gives the DAC a true 2's complement input transfer function. The DAC-7134 contains two resistors used along with the external op-amp to invert the reference. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

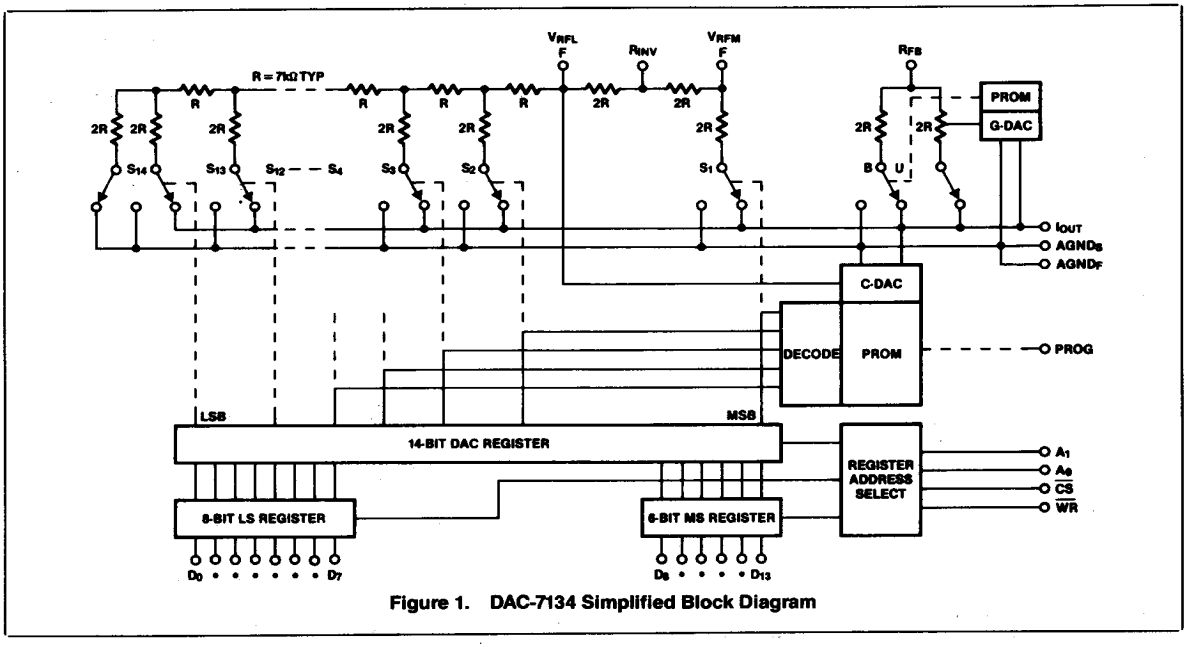

Figure 1. DAC-7134 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
V^+ to DGND -0.3V dc to +7.5V dc

Analog Signals:
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND +/-15V dc
I_{OUT}, $AGND_F$, $AGND_S$ -0.1V dc to V^+
Current in $AGND_S$, $AGND_F$ 25 mA

Digital Signals:
A_0, A_1, D_0 to D_{13}, $\overline{WR}$, $\overline{CS}$, PROG -0.3V to V^+ +0.3V dc

FUNCTIONAL SPECIFICATIONS

Valid at +25 degrees C, +5V dc power supply, and V_{REF} = +10V dc, unless otherwise specified.

DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
INPUT				
Resolution	14	-	-	bits
Logic Levels				
Logical 0	-	-	0.8	V
Logical 1	2.4	-		V
Logic Input Currents	-	-	1.0	µA
Reference Input Resistance	4.0	7.0	10	K ohms
Reference Input Voltage Range	-	-	±12	V
Coding				
Unipolar	straight binary			
Bipolar	2's complement			
ACCURACY				
Non-linearity [1,2]				
J	-	-	0.012	% FSR
K	-	-	0.006	% FSR
L	-	-	0.003	% FSR
Non-linearity Temp. Coef.	-	1	2	ppm/°C
Gain Error [1,2]				
J	-	-	0.024	% FSR
K	-	-	0.012	% FSR
L	-	-	0.006	% FSR
Gain Error Temp. Coef.	-	2	8	ppm/°C
Monotonicity				
J	12	-	-	bits
K	13	-	-	bits
L	14	-	-	bits
Settling Time	-	0.9	3	µSec.
Power Supply Rejection	-	10	100	ppm/V
OUTPUT				
Output Current Range	-	2.14	±3.75	mA
Output Capacitance				
DAC all 0's	-	160	-	pf
DAC all 1's	-	235	-	pf
Output Noise (Equiv. Johnson Noise)	-	7	-	K ohm
Feedthrough Error				
DAC-7134U	-	250	-	µVp-p
DAC-7134B	-	500	-	µVp-p

FOOTNOTES:
1. Full-scale range (FSR) is 10 volts for unipolar mode, 20 volts (± 10 volts) for bipolar mode.
2. Using internal feedback and reference inverting resistors.

DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
POWER				
Supply Voltage Range	+3.5	-	+6.0	V dc
Supply Current (Excluding ladder)	-	1.0	2.5	mA
Power Dissipation	-	-	500	mW
PHYSICAL / ENVIRONMENTAL				
Operating Temperature Range	0	-	+70	°C
Storage Temperature Range	-65	-	+150	°C
Package	28-pin CERDIP only			

The timing diagram represented in Figure 2 shows the relationships between the various bus interface signals. These AC characteristics are listed in Table 1.

DETAILED DESCRIPTION

The DAC-7134 consists of a 14-bit primary DAC, two PROM-controlled correction DAC's, input buffer registers, and microprocessor interface logic (refer back to Figure 1). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC (G-DAC) diverts up to 2% of the feedback resistor's current to analog ground and reduces the gain error to less than 1 LSB, or 0.006%.

The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC (C-DAC). For every combination of the primary DAC's most significant bits, a different C-DAC code is selected. This corrects summation errors (caused when more than one bit is turned on simultaneously) and voltage non-linearity in the feedback resistor.

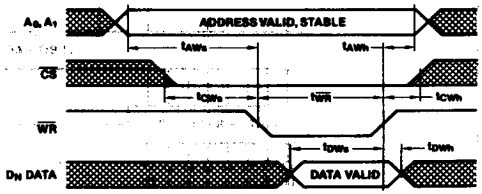

Figure 2. DAC-7134 Timing Diagram

Table 1. AC Characteristics

PARAMETER (V+ = +5V dc)	SYMBOL	MINIMUM (nS)
Address write set-up time	T_{AWs}	100
Address-write hold time	T_{AWh}	0
Chip select-write set-up time	T_{CWs}	0
Chip select-write hold time	T_{CWh}	0
WRITE pulse width, low	$T_{\overline{WR}}$	200
Data write set-up time	T_{DWs}	200
Data write hold time	T_{DWh}	0

PIN DESCRIPTIONS

The input and output pins for both the analog and digital signals used by the DAC-7134 are listed in Table 2 and shown in Figure 3.

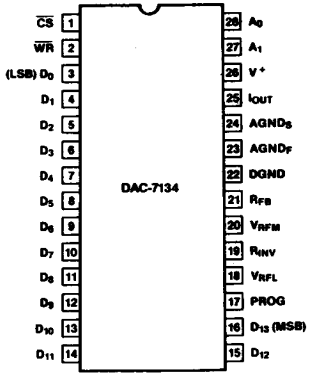

Figure 3. DAC-7134 Pin Configuration

Table 2. Pin Assignment and Function Description

PIN	DESCRIPTION	
1	$\overline{\text{CHIP SELECT}}$ (active low). Enables writing to the register.	
2	$\overline{\text{WRITE}}$, (active low). Enables writing to the register along with $\overline{\text{CHIP SELECT}}$.	
3	Bit 0	Least Significant Bit
4	Bit 1	INPUT DATA BITS High = True
5	Bit 2	
6	Bit 3	
7	Bit 4	
8	Bit 5	
9	Bit 6	
10	Bit 7	
11	Bit 8	
12	Bit 9	
13	Bit 10	
14	Bit 11	
15	Bit 12	
16	Bit 13	Most Significant Bit
17	Used for programming only. Tie to +5V dc for normal operation.	
18	V_{REF} for lower bits	
19	Summing node for reference inverting amplifier	
20	V_{REF} for MSB only (bipolar).	
21	Feedback resistor for voltage output applications	
22	Digital ground return	
23	Analog ground force line. Carries current from internal analog ground connections. Tied internally to $AGND_S$.	
24	Analog ground sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	Current output pin	
26	Positive supply voltage	
27	Address 1	Control register lines
28	Address 0	

ANALOG SECTION

The DAC-7134 provides both unipolar and bipolar operation. The bipolar application circuit (Figure 4) requires one additional operational amplifier, but no external resistors. Two on-chip resistors (R_{INV1}, R_{INV2}), together with the op-amp, form a voltage inverter which drives the MSB reference terminal (V_{RFM}) to $-V_{REF}$.

V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

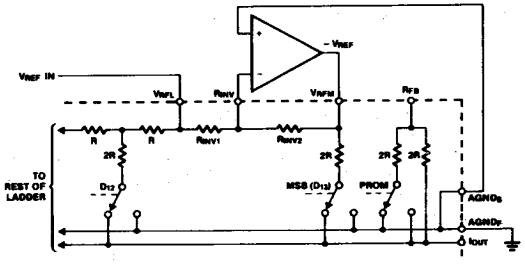

Figure 4. Bipolar Operation, with Inverted V_{REF} to MSB

Since the PROM correction codes required are different for bipolar and unipolar operation, the DAC-7134 is available in two different versions; the DAC-7134U, which is corrected for unipolar operation, and the DAC-7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from "R" in the unipolar device to "2R" in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

DIGITAL SECTION

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations:

1. Load the LS buffer register with the data at inputs D_0 to D_7,
2. Load the MS buffer register with the data at inputs D_8 to D_{13},
3. Load the DAC register with the contents of the MS and LS buffer registers, and,
4. Load the DAC register directly from the data input pins. (See Table 3).

The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfer to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low), the registers are transparent and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V dc).

Table 3. Data Loading Controls

CONTROL LINES				DAC-7134 OPERATION
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected
X	X	1	X	
0	0	0	0	Load registers from data bus
0	1	0	0	Load LS register from data bus
1	0	0	0	Load MS register from data bus
1	1	0	0	Load DAC register from MS and LS register

Note: Data is latched on low-to-high transitions of either $\overline{WR}$ or $\overline{CS}$.

UNIPOLAR BINARY OPERATION

Figure 5 shows a typical circuit configuration for unipolar mode operation using a DAC-7134U. With positive and negative V_{REF} values, the circuit is capable of two-quadrant multiplication. Table 4 presents a digital input code/analog output value' reference for unipolar mode operation. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers.

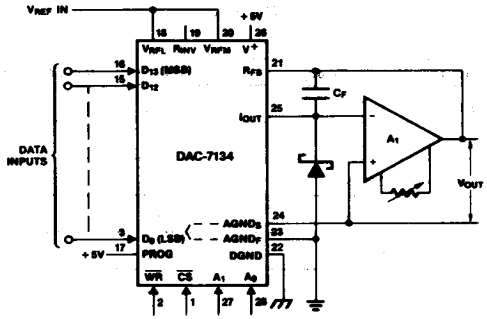

Figure 5. Unipolar Binary, Two-Quadrant Multiplying Circuit

Table 4. Code Table—Unipolar Binary Operation

DIGITAL INPUT MSB ... LSB	ANALOG OUTPUT
1 1 1 ... 1 1 1	$-(V_{REF} + 1\ LSB)$
1 1 0 ... 0 0 0	$-0.75 \times (V_{REF})$
1 0 0 ... 0 0 0	$-0.5 \times (V_{REF})$
0 1 0 ... 0 0 0	$-0.25 \times (V_{REF})$
0 0 0 ... 0 0 0	0

Zero Offset Adjustment
(See Figure 5)

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND. (Connect pins 1 through 16, 27, and 28 to pin 22).
2. Adjust the offset zero-adjust trim-pot of op-amp A2, if used, for a maximum of 0V ±50μV dc at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of output op-amp A1 for a maximum of 0V ±50μV dc at V_{OUT}.

Gain Adjustment (Optional)

1. Connect all data inputs (pins 1 through 16) to V^+ (pin 26). Connect $\overline{CS}$, $\overline{WR}$, A_1 and A_0 (pins 1, 2, 27, and 28 respectively) to DGND (pin 22).
2. Monitor V_{OUT} for a $-(V_{REF} + 1\ LSB)$ reading.
3. To decrease V_{OUT}, connect a series resistor of 100 ohms or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 100 ohms or less between OP-AMP A1's output and the R_{FB} terminal (pin 21).

For applications where the output reference ground point is established somewhere other than at the DAC, a circuit similar to that shown in Figure 6 could be used. Here, op-amp A2 removes the slight error due to IR voltage drop between the internal analog ground node and the external ground connection. For 13-bit or lower accuracy, omit A2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

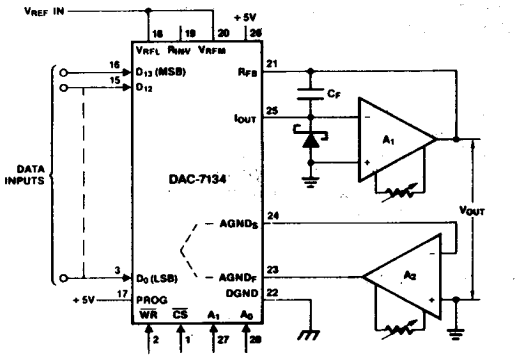

Figure 6. Unipolar Binary Operation with Forced Ground

BIPOLAR (2's COMPLEMENT) OPERATION

Figure 7 shows a circuit configuration for bipolar mode operation using a DAC-7134B. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. Table 5 lists the digital input codes and their respective analog output values for bipolar mode operation.

Amplifier A2, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the DAC-7134B's feedback resistance switches to 2R under PROM control.

The resultant bipolar output range is $+V_{REF}$ to $-(V_{REF} + 1\ LSB)$. Again, the grounding arrangement of Figure 6 can be used.

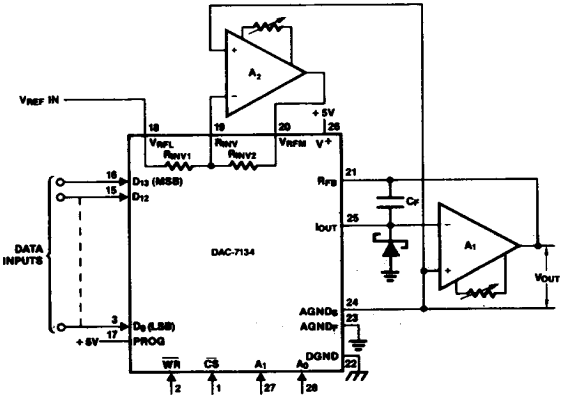

Figure 7. Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

Table 5. Code Table—Bipolar (2's complement) Operation

DIGITAL INPUT MSB ... LSB	ANALOG OUTPUT	
0 1 1 ... 1 1 1	$+V_{REF}$—1LSB	$-V_{REF}$ + 1LSB
0 1 0 ... 0 0 0	0.5($+V_{REF}$)	0.5($-V_{REF}$)
0 0 0 ... 0 0 0	0	0
1 1 0 ... 0 0 0	0.5($-V_{REF}$)	0.5($+V_{REF}$)
1 0 0 ... 0 0 0	$-V_{REF}$	$+V_{REF}$

Offset Adjustment
(See Figure 7)

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND. (Connect pins 1 through 16, 27, and 28 to pin 22).
2. Set data to 00000 . . . . 00. Adjust the offset zero adjust trim-pot of output op-amp A1 for a maximum of 0V ±50μV dc V_{OUT}.
3. Connect D_{13} (MSB, pin 16) data input to V+ (pin 26).
4. Adjust the offset zero-adjust trim-pot of op-amp A2 for a maximum of 0V ±50uV dc at the R_{INV} terminal (pin 19).

Gain Adjustment (Optional)

1. Connect $\overline{CS}$, $\overline{WR}$, A_1 and A_0 (pins 1, 2, 27, and 28 respectively) to DGND (pin 22).
2. Connect D_0 through D_{12} (pins 3 through 15) to V+ (pin 26). Connect D_{13} (MSB, pin 16) to DGND (pin 22).
3. Monitor V_{OUT} for a $-V_{REF}$ + 1LSB reading.
4. To increase V_{OUT}, connect a series resistor of 200 ohms or less between op-amp A1's output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 100 ohms or less between the reference voltage and the V_{RFL} terminal (pin 18).

APPLICATIONS

General Recommendations

Ground Loops

Careful consideration must be given to ground loops in any system with 14-bit accuracy. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, and $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point. Thus, output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

Power Supplies

The V+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V+, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V+ for proper operation.

Operational Amplifier Selection

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus, output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10Vdc range also requires that the output amplifier has a high open loop gain (A_{VOL} > 400k for effective input offset less than 25μV).

The reference inverting amplifier used in the biopolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the analog ground line (op-amp A_2 in Figure 6). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

The op-amp requirements can be readily met using an AM-7650 chopper stabilized device. For faster settling time, DATEL's AM-460 or AM-462 can be used with an AM-7650 providing automatic offset null.

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trimpots should be selected.

PACKAGE DIMENSIONS

The DAC-7134B and DAC-1734U differ only in the programming instructions. Therefore, the same package dimensions, as shown in Figure 8, apply to both model numbers. The device is available only in a standard 28-pin CERDIP package.

PACKAGE DIMENSIONS All dimensions in inches (millimeters)

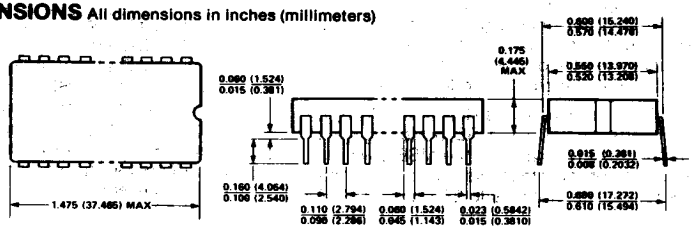

Figure 8. 28-Pin CERDIP Package Dimensions

ORDERING INFORMATION

DAC-7134-

- J = 12-Bit Linearity (0.01% FSR)
- K = 13-Bit Linearity (0.006% FSR)
- L = 14-Bit Linearity (0.003% FSR)

- B = Bipolar Version
- U = Unipolar Version