## Features

- **Low-voltage and Standard-voltage Operation**
  - **2.7 ($V_{CC}$ = 2.7V to 5.5V)**
  - **1.8 ($V_{CC}$ = 1.8V to 5.5V)**
- **Three-wire Serial Interface**
- **2 MHz Clock Rate (5V) Compatibility**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade, Extended Temperature, and Lead-free/Halogen-free Devices Available**
- **8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages**

## Description

The AT93C46A provides 1024 bits of serial electrically-erasable programmable read-only memory (EEPROM) organized as 64 words of 16 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT93C46A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages.

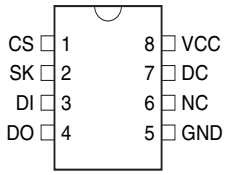
The AT93C46A is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output DO pin. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the erase/write enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the ready/busy status of the part.

The AT93C46A is available in 2.7V to 5.5V and 1.8V to 5.5V versions.

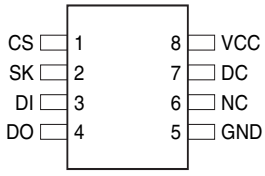
**Table 1.** Pin Configuration

| Pin Name | Function |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| VCC | Power Supply |

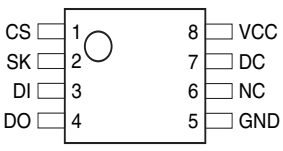
8-lead PDIP




8-lead SOIC




8-lead TSSOP




# Three-wire Serial EEPROM

**1K (64 x 16)**

# AT93C46A

Note: Not recommended for new design; please refer to AT93C46E datasheet.

Rev. 0539K–SEEPR–2/07

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | –1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 1.** Block Diagram

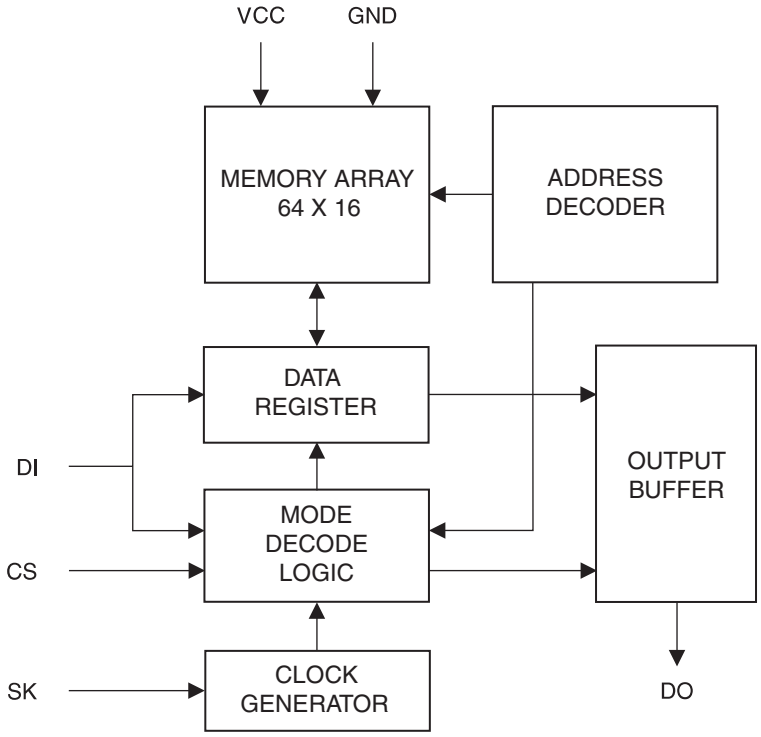


**Table 2.** Pin Capacitance[1]

Applicable over recommended operating range from $T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = +5.0V (unless otherwise noted)

| Symbol | Test Conditions | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (DO) | 5 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$ | Input Capacitance (CS, SK, DI) | 5 | pF | $V_{IN}$ = 0V |

Note: This parameter is characterized and is not 100% tested.

**Table 3.** DC Characteristics

Applicable over recommended operating range from: $T_{AI}$ = –40°C to +85°C, $V_{CC}$ = +1.8V to +5.5V, (unless otherwise noted)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | | | 1.8 | | 5.5 | V |
| $V_{CC2}$ | Supply Voltage | | | 2.7 | | 5.5 | V |
| $V_{CC3}$ | Supply Voltage | | | 4.5 | | 5.5 | V |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.0V | Read at 1.0 MHz | | 0.5 | 2.0 | mA |
| | | | Write at 1.0 MHz | | 0.5 | 2.0 | mA |
| $I_{SB1}$ | Standby Current | $V_{CC}$ = 1.8V | CS = 0V | | 14.0 | 20.0 | µA |
| $I_{SB2}$ | Standby Current | $V_{CC}$ = 2.7V | CS = 0V | | 14.0 | 20.0 | µA |
| $I_{SB3}$ | Standby Current | $V_{CC}$ = 5.0V | CS = 0V | | 35.0 | 50.0 | µA |
| $I_{IL}$ | Input Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | | 0.1 | 1.0 | µA |
| $I_{OL}$ | Output Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | | 0.1 | 1.0 | µA |
| $V_{IL1}$[1]<br>$V_{IH1}$[1] | Input Low Voltage<br>Input High Voltage | 2.7V ≤ $V_{CC}$ ≤ 5.5V | | –0.6<br>2.0 | | 0.8<br>$V_{CC}$ + 1 | V |
| $V_{IL2}$[1]<br>$V_{IH2}$[1] | Input Low Voltage<br>Input High Voltage | 1.8V ≤ $V_{CC}$ ≤ 2.7V | | –0.6<br>$V_{CC}$ x 0.7 | | $V_{CC}$ x 0.3<br>$V_{CC}$ + 1 | V |
| $V_{OL1}$<br>$V_{OH1}$ | Output Low Voltage<br>Output High Voltage | 2.7V ≤ $V_{CC}$ ≤ 5.5V | $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| | | | $I_{OH}$ = –0.4 mA | 2.4 | | | V |
| $V_{OL2}$<br>$V_{OH2}$ | Output Low Voltage<br>Output High Voltage | 1.8V ≤ $V_{CC}$ ≤ 2.7V | $I_{OL}$ = 0.15 mA | | | 0.2 | V |
| | | | $I_{OH}$ = –100 µA | $V_{CC}$ – 0.2 | | | V |

Note: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.

**Table 4.** AC Characteristics

Applicable over recommended operating range from $T_A$ = –40°C to + 85°C, $V_{CC}$ = +2.5V to + 5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $f_{SK}$ | SK Clock Frequency | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | 0<br>0<br>0 | | 2<br>1<br>0.25 | MHz |
| $t_{SKH}$ | SK High Time | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | 250<br>250<br>1000 | | | ns |
| $t_{SKL}$ | SK Low Time | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | 250<br>250<br>1000 | | | ns |
| $t_{CS}$ | Minimum CS Low Time | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | 250<br>250<br>1000 | | | ns |
| $t_{CSS}$ | CS Setup Time | Relative to SK | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | 50<br>50<br>200 | | | ns |
| $t_{DIS}$ | DI Setup Time | Relative to SK | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | 100<br>100<br>400 | | | ns |
| $t_{CSH}$ | CS Hold Time | Relative to SK | | 0 | | | ns |
| $t_{DIH}$ | DI Hold Time | Relative to SK | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | 100<br>100<br>400 | | | ns |
| $t_{PD1}$ | Output Delay to “1” | AC Test | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | | 250<br>250<br>1000 | ns |
| $t_{PD0}$ | Output Delay to “0” | AC Test | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | | 250<br>250<br>1000 | ns |
| $t_{SV}$ | CS to Status Valid | AC Test | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | | 250<br>250<br>1000 | ns |
| $t_{DF}$ | CS to DO in High Impedance | AC Test<br>CS = $V_{IL}$ | $4.5V \le V_{CC} \le 5.5V$<br>$2.7V \le V_{CC} \le 5.5V$<br>$1.8V \le V_{CC} \le 5.5V$ | | | 100<br>100<br>400 | ns |
| $t_{WP}$ | Write Cycle Time | | | 0.1 | 3 | 10 | ms |
| Endurance(1) | 5.0V, 25°C | | | 1M | | | Write Cycle |

Note: 1. This parameter is characterized and is not 100% tested.

## Functional Description

The AT93C46A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a start bit (logic "1") followed by the appropriate op code and the desired memory address location.

**Table 5.** Instruction Set for the AT93C46A

| Instruction | SB | Op Code | Address x 16 | Comments |
|---|---|---|---|---|
| READ | 1 | 10 | $A_5 - A_0$ | Reads data stored in memory, at specified address |
| EWEN | 1 | 00 | 11XXXX | Write enable must precede all programming modes |
| ERASE | 1 | 11 | $A_5 - A_0$ | Erase memory location $A_n - A_0$ |
| WRITE | 1 | 01 | $A_5 - A_0$ | Writes memory location $A_n - A_0$ |
| ERAL | 1 | 00 | 10XXXX | Erases all memory locations. Valid only at $V_{CC}$ = 4.5V to 5.5V |
| WRAL | 1 | 00 | 01XXXX | Writes all memory locations. Valid only at $V_{CC}$ = 4.5V to 5.5V |
| EWDS | 1 | 00 | 00XXXX | Disables all programming instructions |

**READ (READ):** The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 16-bit data output string.

**ERASE/WRITE ENABLE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or $V_{CC}$ power is removed from the part.

**ERASE (ERASE):** The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ($t_{CS}$). A logic "1" at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

**WRITE (WRITE):** The Write (WRITE) instruction contains the 16 bits of data to be written into the specified memory location. The self-timed programming cycle, $t_{WP}$, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ($t_{CS}$). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A ready/busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, $t_{WP}$.*

**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ($t_{CS}$). The ERAL instruction is valid only at $V_{CC}$ = 5.0V ± 10%.

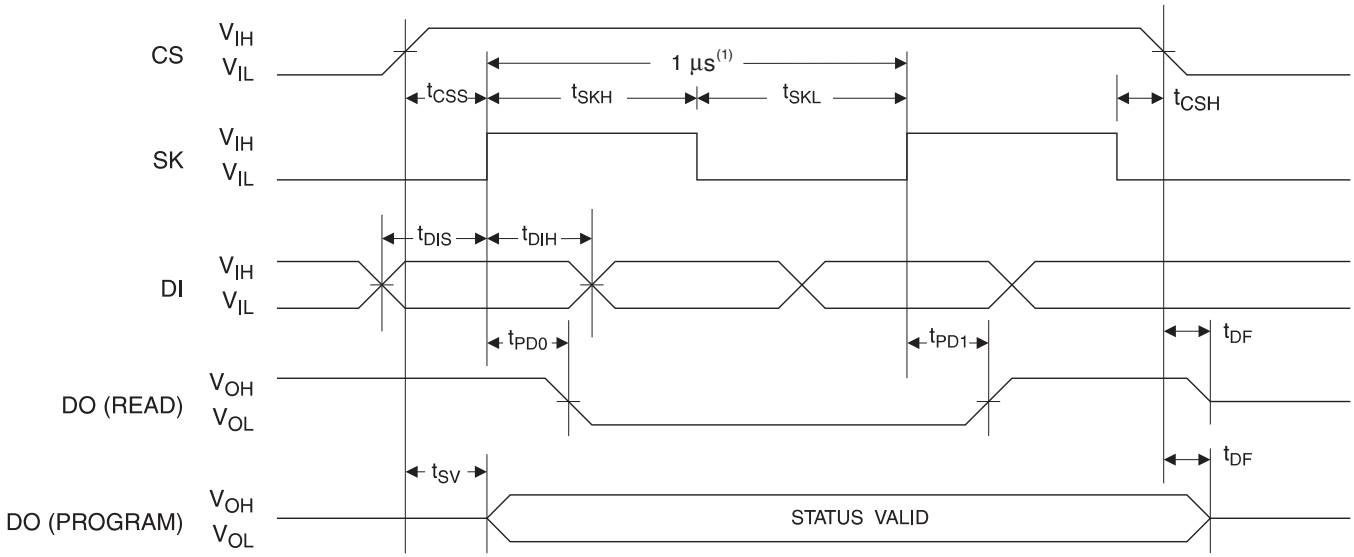
**WRITE ALL (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the ready/busy

status of the part if CS is brought high after being kept low for a minimum of 250 ns ($t_{CS}$). The WRAL instruction is valid only at $V_{CC}$ = 5.0V ± 10%.

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

## Timing Diagrams

**Figure 2.** Synchronous Data Timing




Note: 1. This is the minimum SK period.

**Table 6.** Organization Key for Timing Diagrams

| | AT93C46A |
|---|---|
| **I/O** | **x 16** |
| $A_N$ | $A_5$ |
| $D_N$ | $D_{15}$ |

**Figure 3.** READ Timing

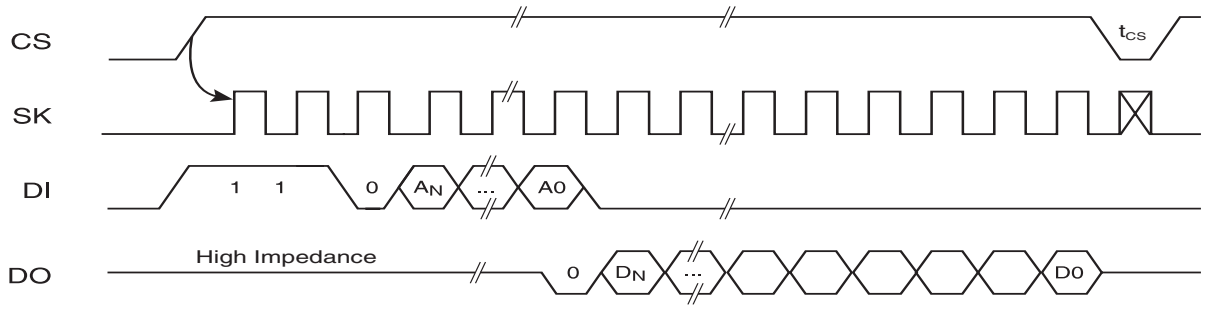
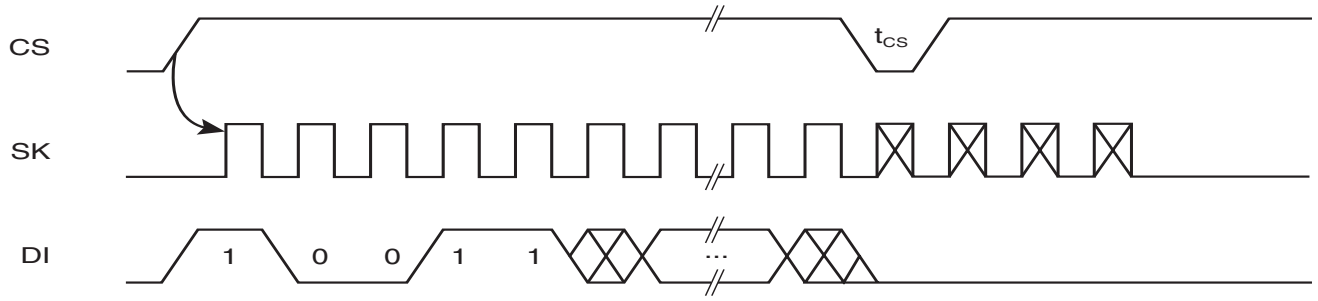
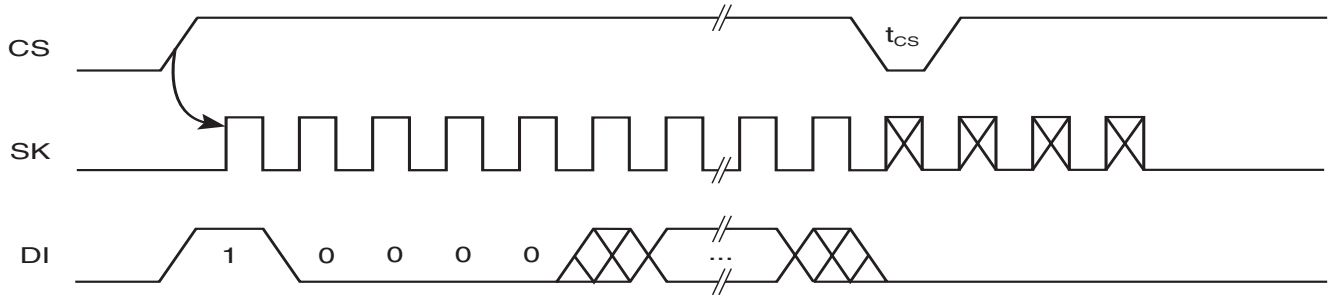



**Figure 4.** EWEN Timing[1]




Note: 1. Requires a minimum of nine clock cycles.

**Figure 5.** EWDS Timing[1]




Note: 1. Requires a minimum of nine clock cycles.

**Figure 6.** WRITE Timing

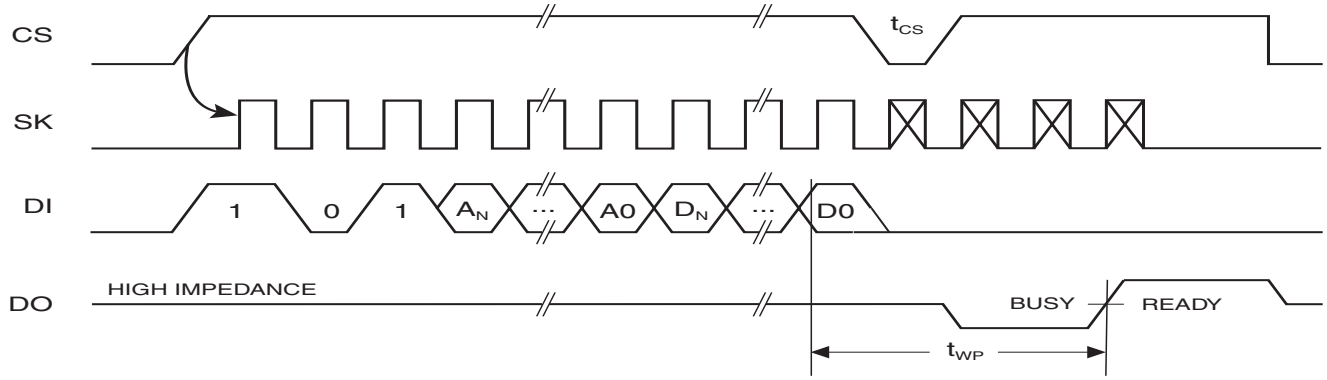
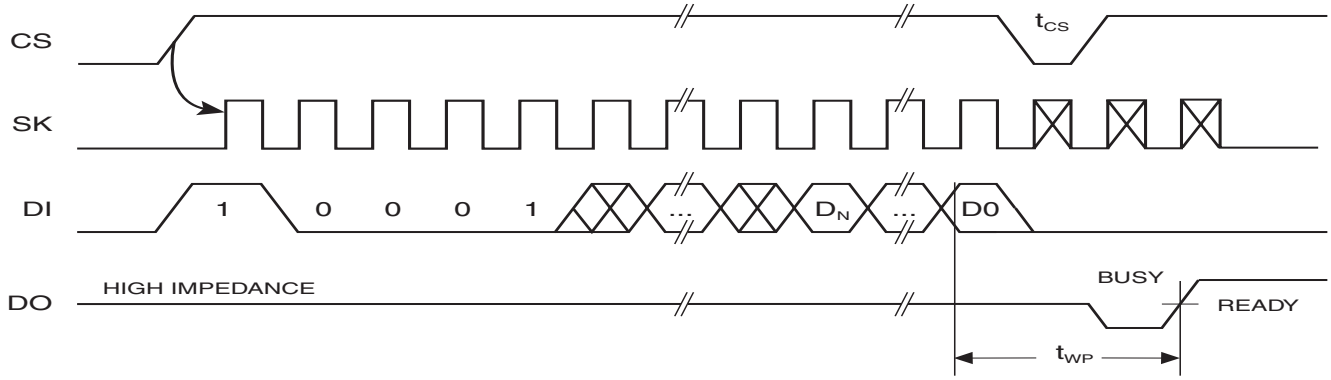



**Figure 7.** WRAL Timing[1],[2]




Notes: 1. Valid only at $V_{CC}$ = 4.5V to 5.5V.
2. Requires a minimum of nine clock cycles.

**Figure 8.** ERASE Timing

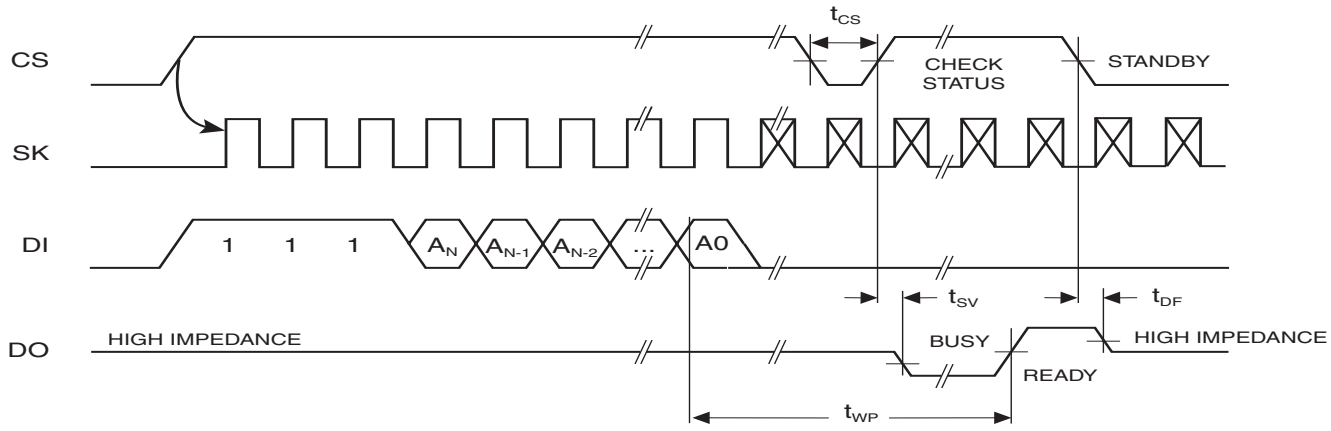
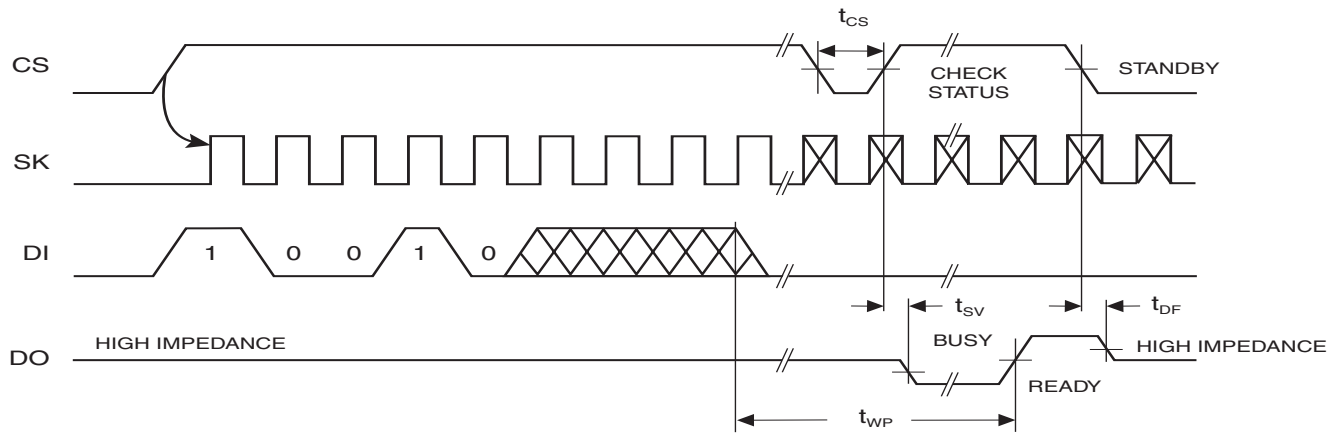


**Figure 9.** ERAL Timing[1]




Note: 1. Valid only at $V_{CC}$ = 4.5V to 5.5V.

## Ordering Information[1]

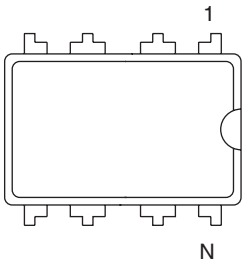
| Ordering Code | Package | Operation Range |
|---|---|---|
| AT93C46A-10PU-2.7 | 8P3 | Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C) |
| AT93C46A-10PU-1.8 | 8P3 | |
| AT93C46A-10SU-2.7 | 8S1 | |
| AT93C46A-10SU-1.8 | 8S1 | |
| AT93C46A-10TU-2.7 | 8A2 | |
| AT93C46A-10TU-1.8 | 8A2 | |

Notes: 1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in Table 3 on page 3 and Table 4 on page 4. Not recommended for new design. Please see AT93C46E datasheet.

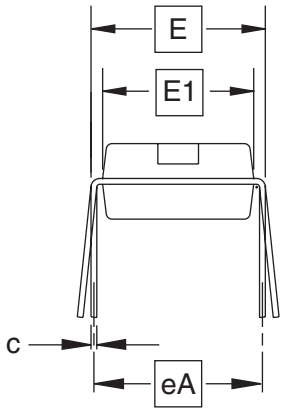
| Package Type | |
|---|---|
| **8P3** | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| **8A2** | 8-lead, 0.170" Wide, Thin Small Outline Package (TSSOP) |
| **Options** | |
| –**2.7** | Low Voltage (2.7V to 5.5V) |
| –**1.8** | Low Voltage (1.8V to 5.5V) |

## Packaging Information

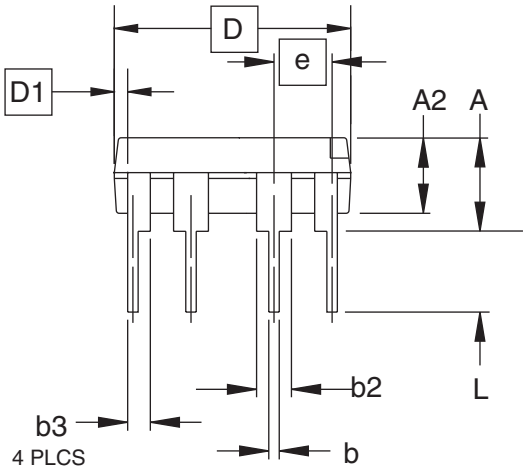
### 8P3 – PDIP




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = inches)

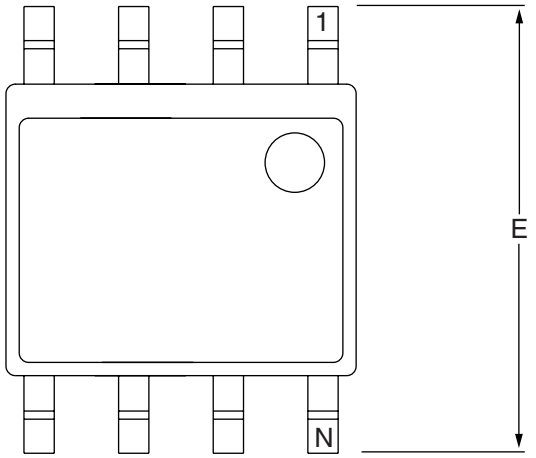
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

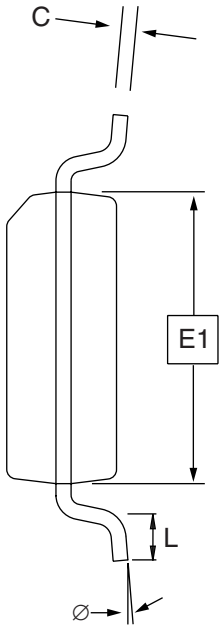
01/09/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP) | 8P3 | B |

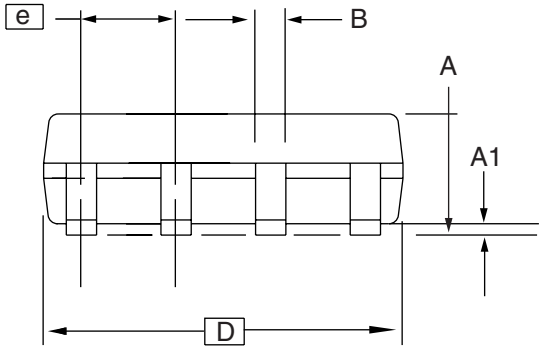
## 8S1 – JEDEC SOIC




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

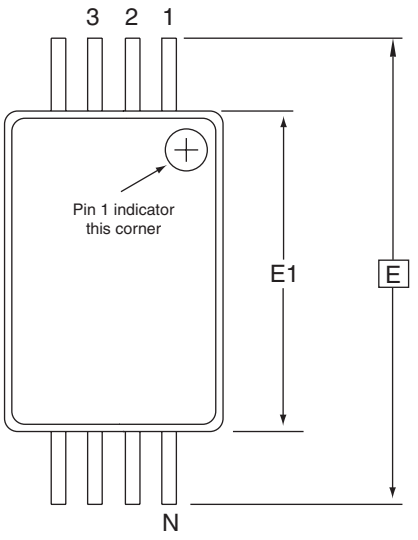
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.35 | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | 4.80 | – | 5.00 | |
| E1 | 3.81 | – | 3.99 | |
| E | 5.79 | – | 6.20 | |
| e | 1.27 BSC | | | |
| L | 0.40 | – | 1.27 | |
| ∅ | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

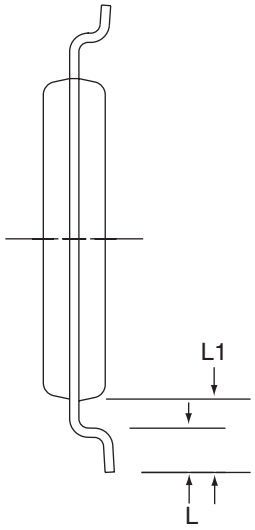
10/7/03

| | | | |
|---|---|---|---|
| 1150 E. Cheyenne Mtn. Blvd.<br>Colorado Springs, CO 80906 | **TITLE**<br>**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | **DRAWING NO.**<br>8S1 | **REV.**<br>B |

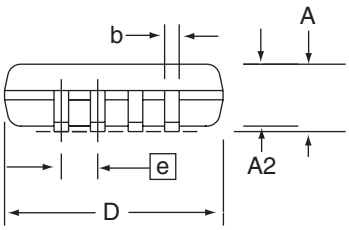
## 8A2 – TSSOP




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| A | – | – | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | – | 0.30 | 4 |
| e | | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 REF | | |

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8A2**, 8-lead, 4.4 mm Body, Plastic<br>Thin Shrink Small Outline Package (TSSOP) | 8A2 | B |

## Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 0539K | 2/2007 | Implemented revision history.<br>Added Note to page 1 and ordering information; Not recommended for new design; please refer to AT93C46E datasheet. |

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