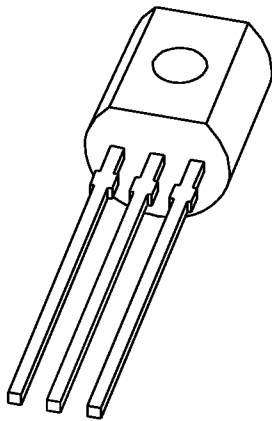


DATA SHEET



2PA733

PNP general purpose transistor

Product specification
Supersedes data of 1997 Mar 25
File under Discrete Semiconductors, SC04

1998 Jul 21

PNP general purpose transistor

2PA733

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 50 V).

APPLICATIONS

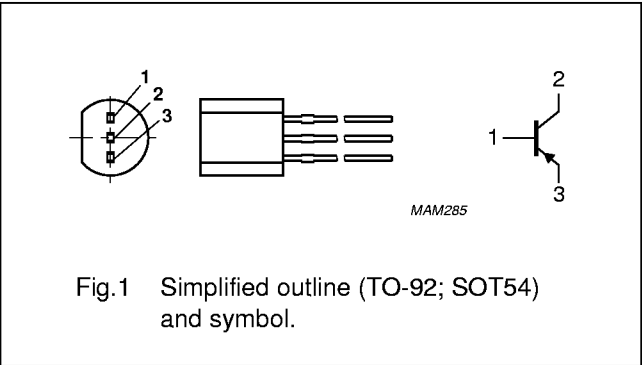
- General purpose switching and amplification.

DESCRIPTION

PNP transistor in a TO-92; SOT54 plastic package.
NPN complement: 2PC945.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–	–60	V
V_{CEO}	collector-emitter voltage	open base	–	–	–50	V
I_{CM}	peak collector current		–	–	–200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	–	–	500	mW
h_{FE}	DC current gain	$I_C = -1\text{ mA}; V_{CE} = -6\text{ V}$	135	–	600	
f_T	transition frequency	$I_C = -10\text{ mA}; V_{CE} = -6\text{ V}; f = 100\text{ MHz}$	100	180	–	MHz

PNP general purpose transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	—	−60	V
V_{CEO}	collector-emitter voltage	open base	—	−50	V
V_{EBO}	emitter-base voltage	open collector	—	−5	V
I_C	collector current (DC)		—	−100	mA
I_{CM}	peak collector current		—	−200	mA
I_{BM}	peak base current		—	−100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	—	500	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		—	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	250	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless other specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = -60\text{ V}$	—	—	−100	nA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = -5\text{ V}$	—	—	−100	nA
h_{FE}	DC current gain	$I_C = -1\text{ mA}$; $V_{CE} = -6\text{ V}$				
	2PA733		135	—	600	
	2PA733Q		135	—	270	
	2PA733P		200	—	400	
	2PA733K		300	—	600	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -100\text{ mA}$; $I_B = -10\text{ mA}$	—	—	−300	mV
V_{BE}	base-emitter voltage	$I_C = -1\text{ mA}$; $V_{CE} = -6\text{ V}$	−600	—	−700	mV
C_c	collector capacitance	$I_E = I_C = 0$; $V_{CB} = -10\text{ V}$; $f = 1\text{ MHz}$	—	4.5	6	pF
C_e	emitter capacitance	$I_C = I_E = 0$; $V_{EB} = -0.5\text{ V}$; $f = 1\text{ MHz}$	—	10	—	pF
f_T	transition frequency	$I_C = -10\text{ mA}$; $V_{CE} = -6\text{ V}$; $f = 100\text{ MHz}$	100	180	—	MHz
F	noise figure	$I_C = -200\text{ }\mu\text{A}$; $V_{CE} = -5\text{ V}$; $R_S = 2\text{ k}\Omega$; $f = 1\text{ kHz}$; $B = 100\text{ Hz}$	—	—	10	dB

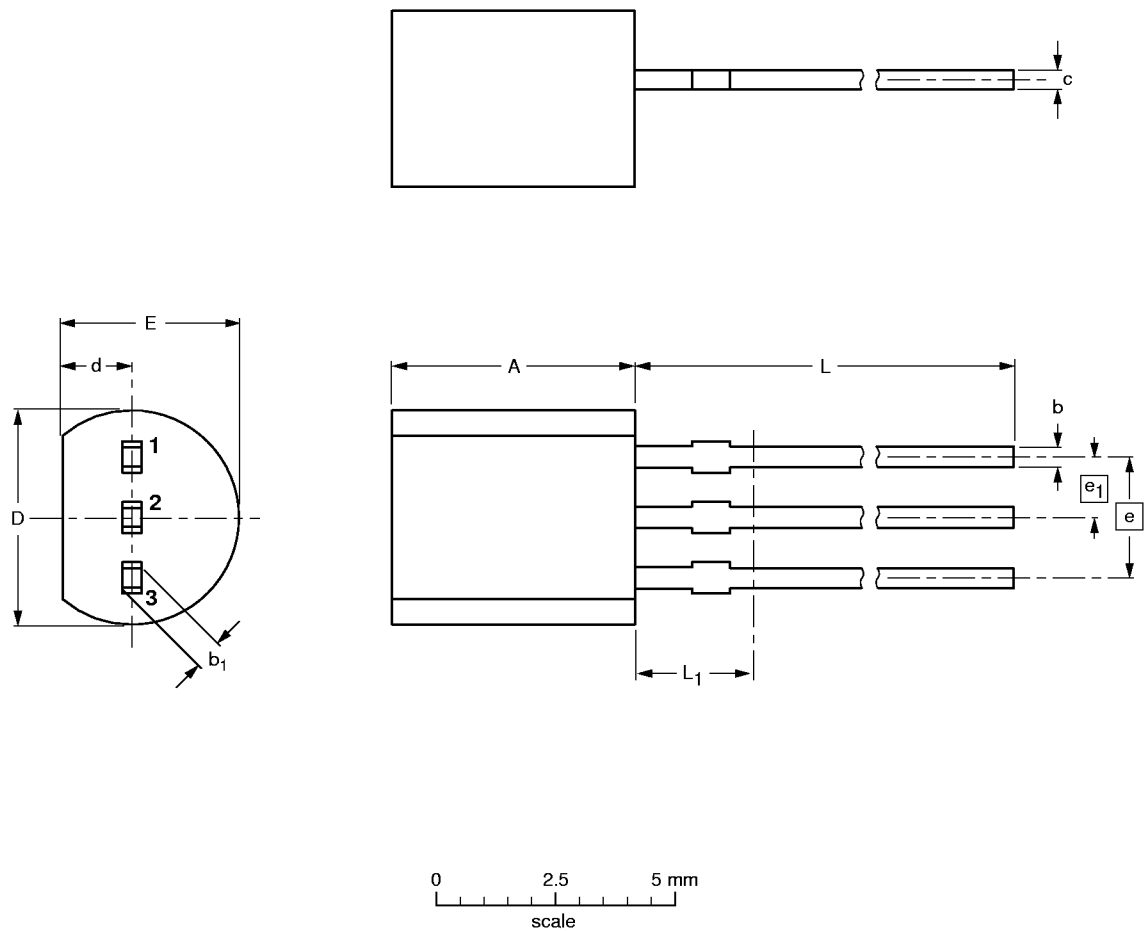
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28