VNQ810PEP-E

QUAD CHANNEL HIGH SIDE DRIVER

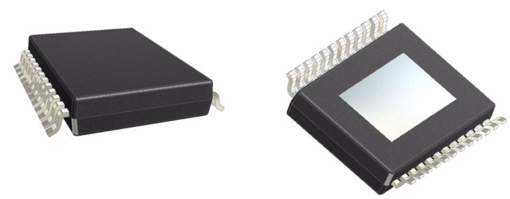
Table 1. General Features

TYPE	V_{CC}	$R_{DS(on)}$	I_{out}
VNQ810PEP-E	36V	160mΩ	5A(*)

(*) Per channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- LOSS OF GROUND PROTECTION
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



PowerSSO-24

DESCRIPTION

The VNQ810PEP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the deviceagainst low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects open load condition both in on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VNQ810PEP-E	VNQ810PEPTR-E

Note: (**) See application schematic at page 8.

Figure 2. Block Diagram

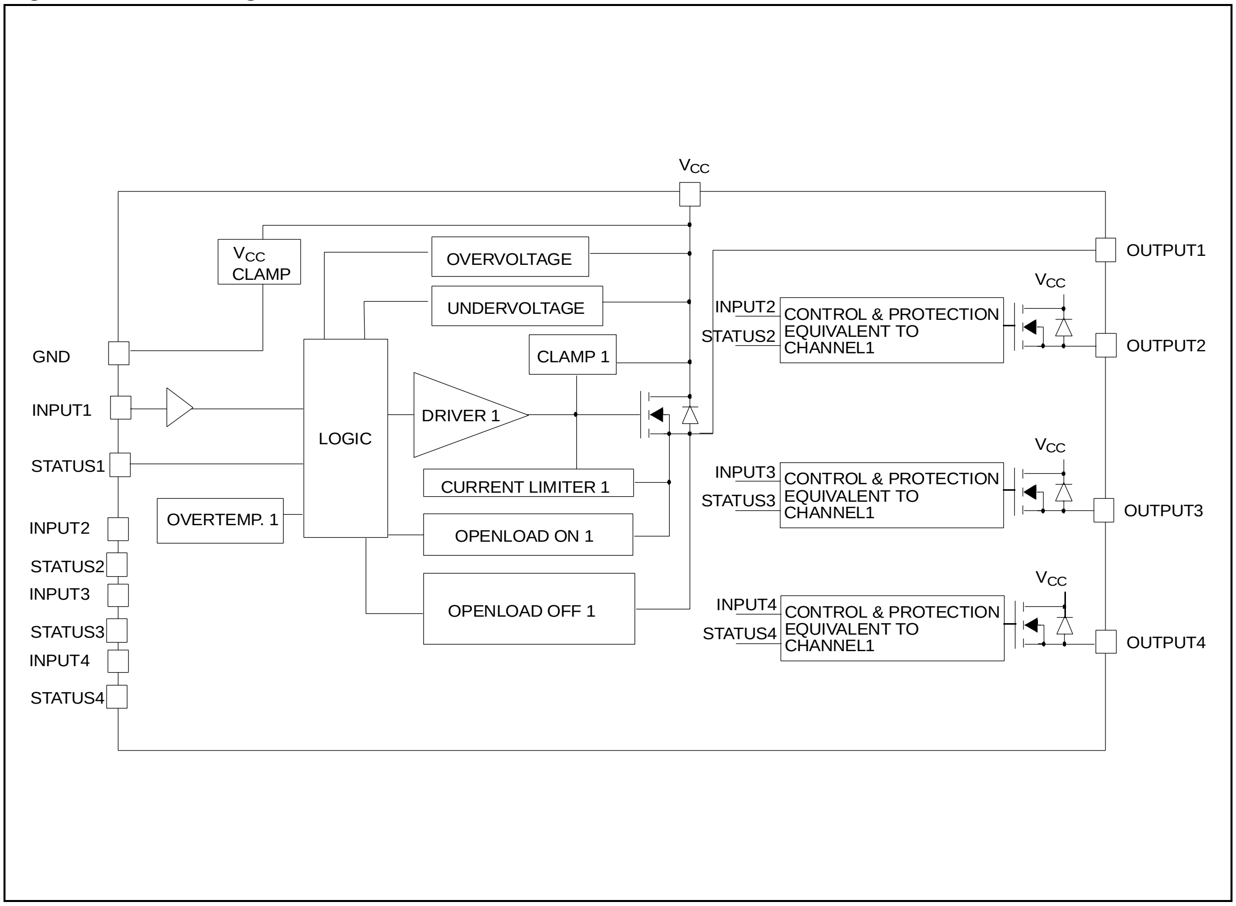
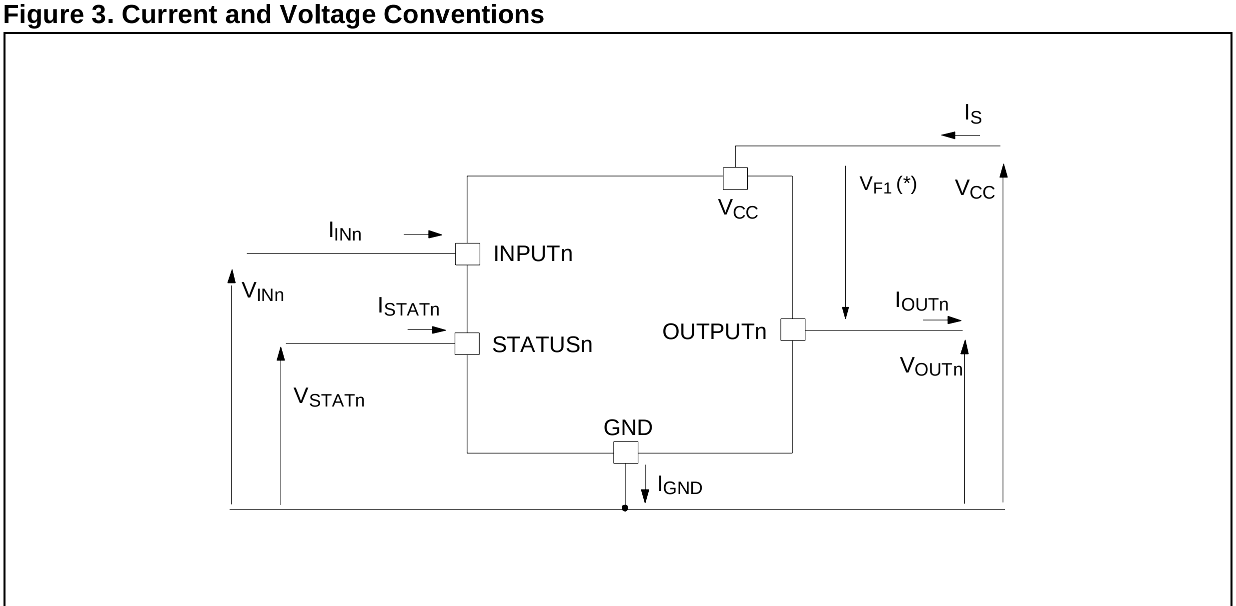
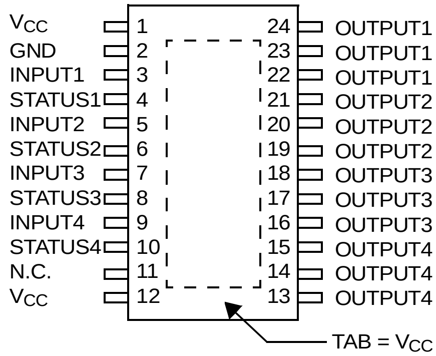


Figure 3. Current and Voltage Conventions



(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

Figure 4. Configuration Diagram (Top View) & Suggested Connections For Unused and n.c. Pins



Connection / Pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To Ground		X		Through 10KΩ resistor

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{STAT}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
P_{tot}	Power Dissipation T_C=25°C	66	W
T_j	Junction Operating Temperature	Internally Limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

Table 4. Thermal Data

Symbol	Parameter	Value		Unit
$R_{thj-case}$	Thermal Resistance Junction-case	1.9		°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	56 (1)	42 (2)	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.

Note: 2. When mounted on a standard single-sided FR-4 board with 8cm^2 of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C< T_j <150°C, unless otherwise specified)

Table 5. Power Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON} (**)	On State Resistance	I_{OUT} =1A; T_j =25°C I_{OUT} =1A; V_{CC}> 8V			160 320	mΩ mΩ
I_S	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		20 20 8.5	60 40 13.5	µA µA mA
$I_{L(off1)}$ (**)	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$ (**)	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$ (**)	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$ (**)	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

Note: (**) Per each channel

Table 6. Switching (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=13Ω from V_{IN} rising edge to V_{OUT}=1.3V		30		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=13Ω from V_{IN} falling edge to V_{OUT}=11.7V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=13Ω from V_{OUT}=1.3V to V_{OUT}=10.4V		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=13Ω from V_{OUT}=11.7V to V_{OUT}=1.3V		See relative diagram		V/µs

ELECTRICAL CHARACTERISTICS (continued)

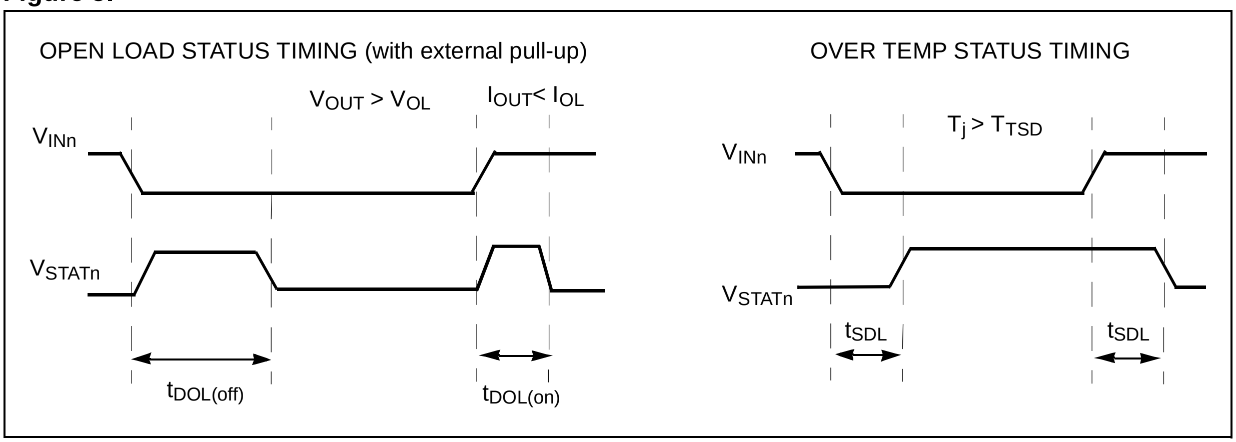
Table 7. Logic Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN} = 1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 -0.7	8	V V

Table 8. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	V_{IN}=5V	20	40	80	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	I_{OUT}=0A			200	µs
V_{OL}	Openload OFF State Voltage Detection Threshold	V_{IN}=0V	1.5	2.5	3.5	V
$T_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	µs

Figure 5.



ELECTRICAL CHARACTERISTICS (continued)

Table 9. V_{CC}- Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}$=0.5A; T_j=150°C			0.6	V

Table 10. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	I_{STAT}= 1.6 mA			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; V_{STAT}= 5V			10	µA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; V_{STAT}= 5V			100	pF
V_{SCL}	Status Clamp Voltage	I_{STAT}=1mA I_{STAT}= - 1mA	6	6.8 -0.7	8	V V

Table 11. Protections and Diagnostics (see note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
t_{SDL}	Status Delay in Overload Conditions	T_j>T_{TSD}			20	µs
I_{lim}	Current limitation	V_{CC}=13V 5.5V < V_{CC} < 36V	5	7.5	10 10	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=1A; L= 6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 12. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H (T_j < T_{TSD}) H (T_j > T_{TSD}) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

Figure 6. Switching Time Waveforms

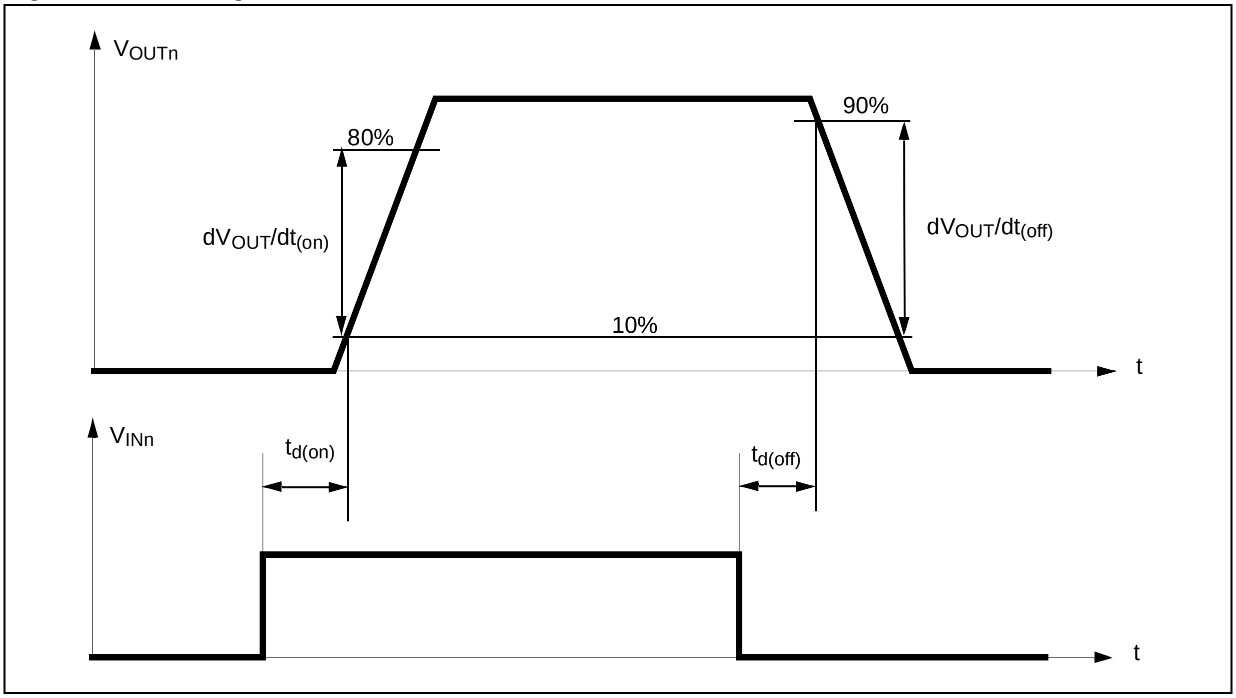


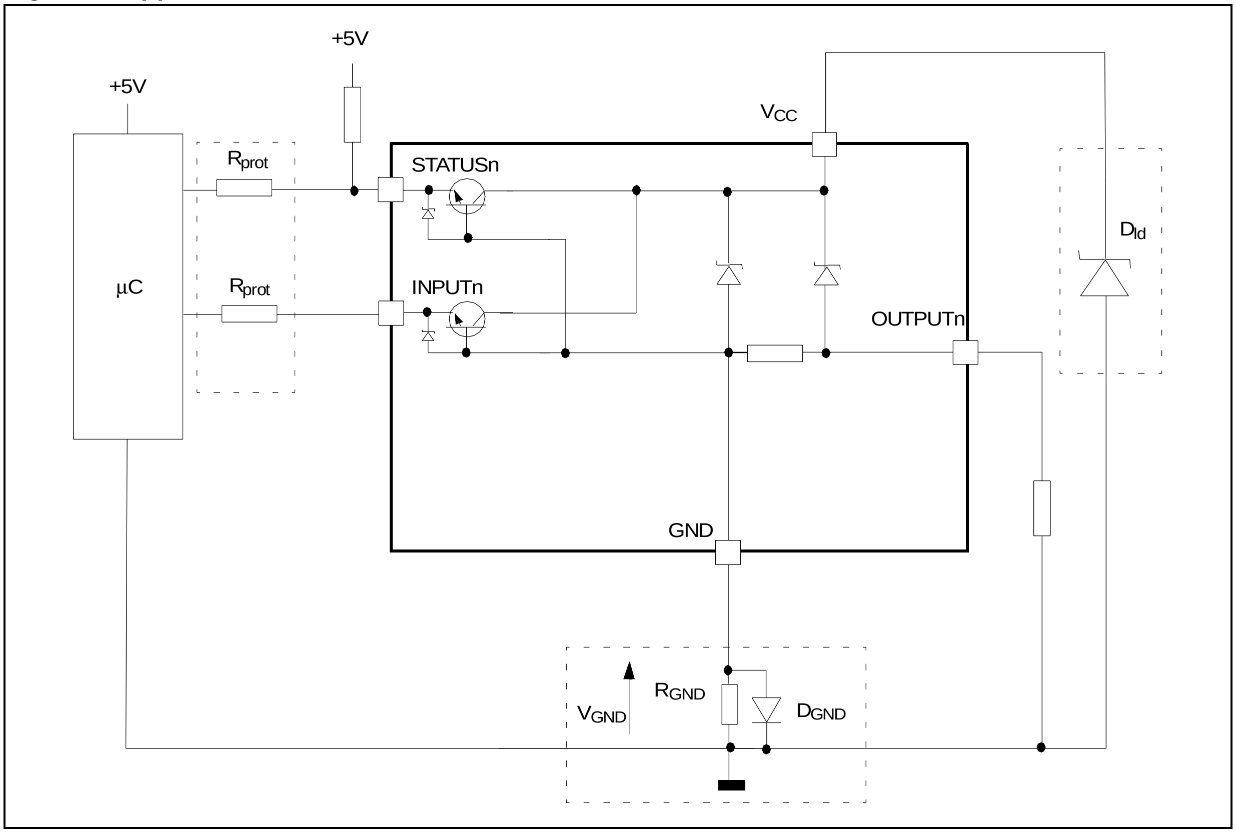
Table 13. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 7. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / I_{S(on)max}$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.

2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}-V_{OLmax})/I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

Figure 8. Open Load detection in off state

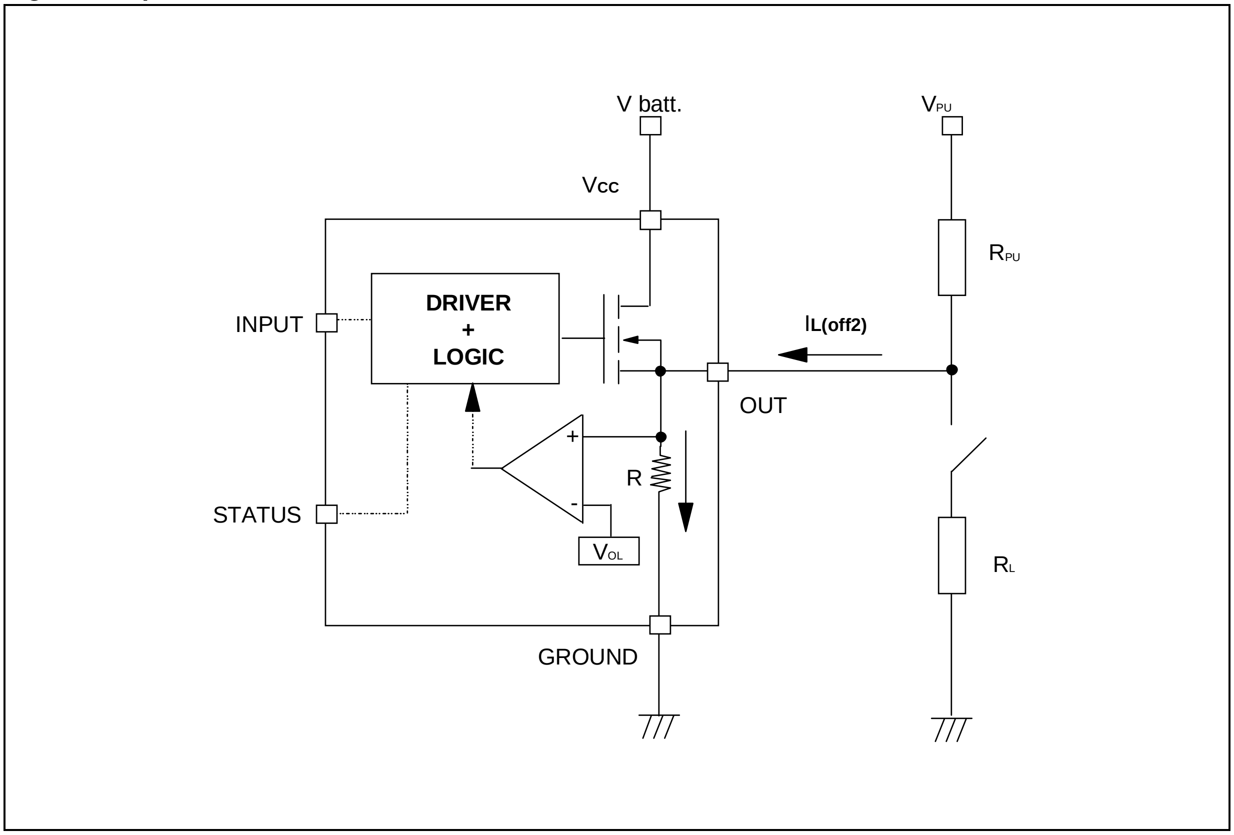


Figure 9. Waveforms

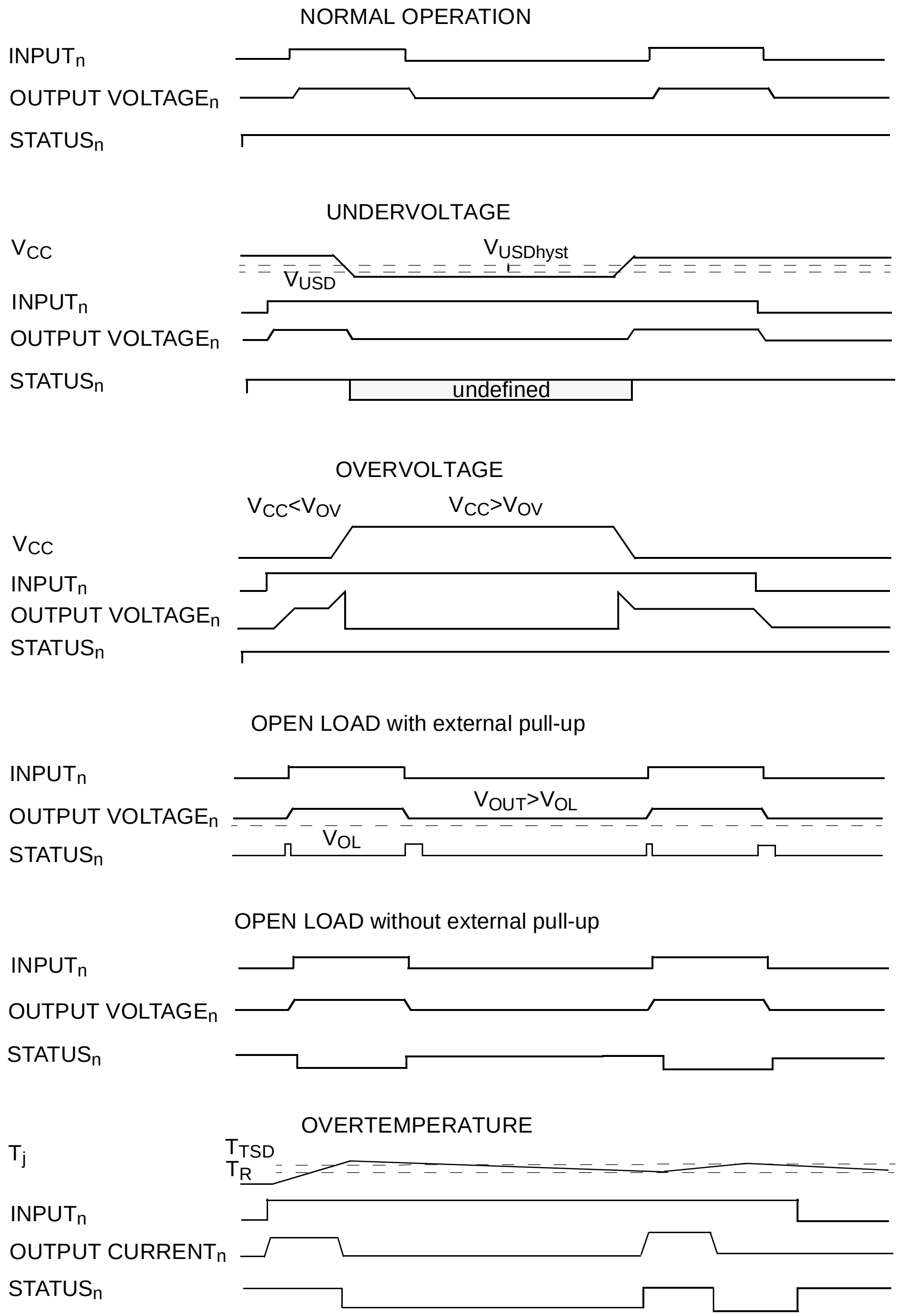


Figure 10. Off State Output Current

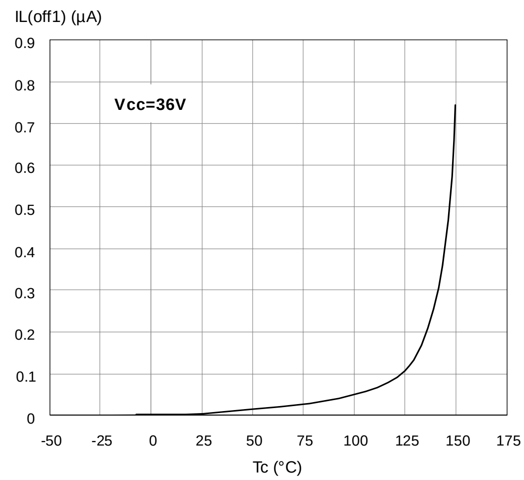


Figure 11. High Level Input Current

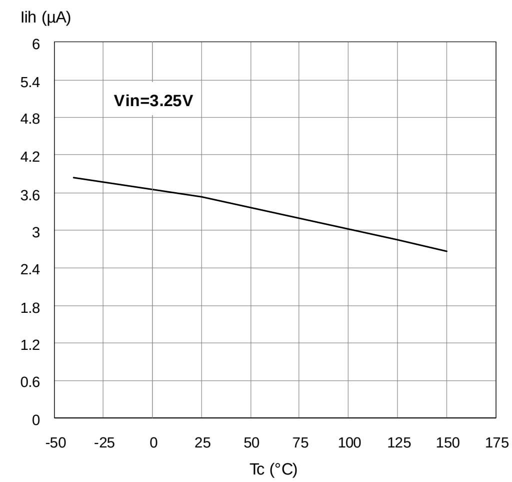


Figure 12. Input Clamp Voltage

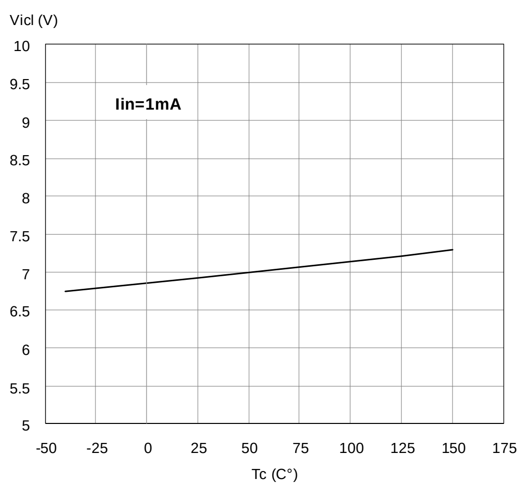


Figure 14. Status Leakage Current

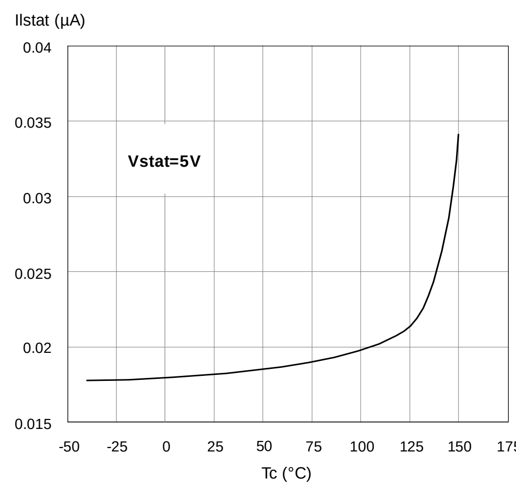


Figure 13. Status Low Output Voltage

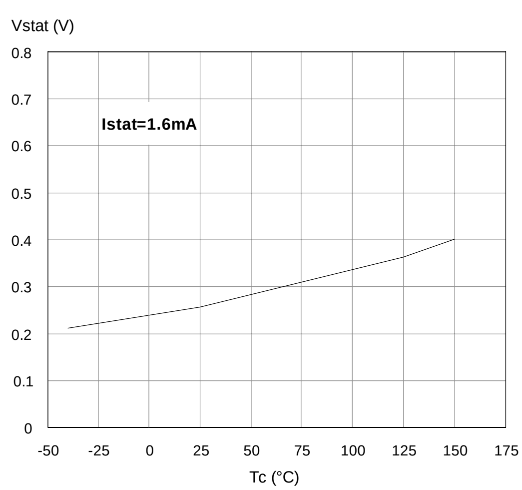


Figure 15. Status Clamp Voltage

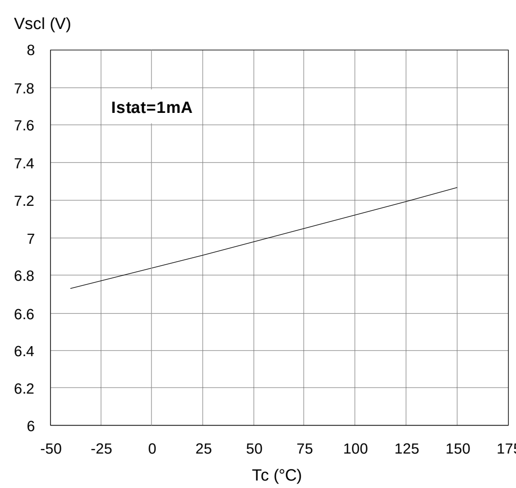


Figure 16. Turn-on Voltage Slope

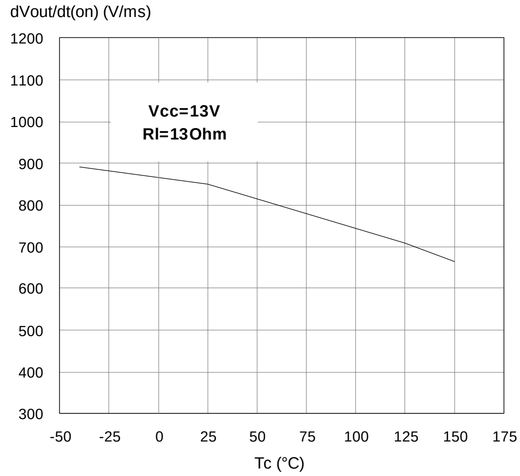


Figure 19. Turn-off Voltage Slope

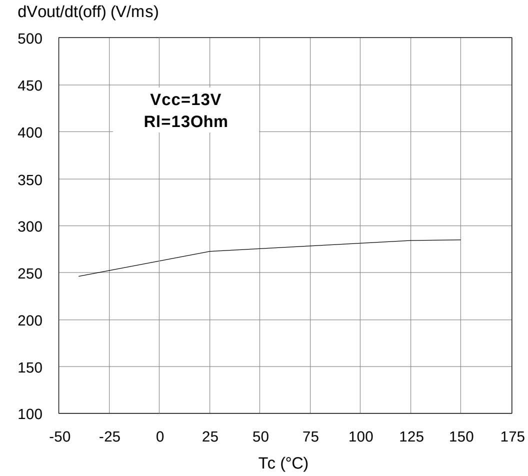


Figure 17. On State Resistance Vs T_{case}

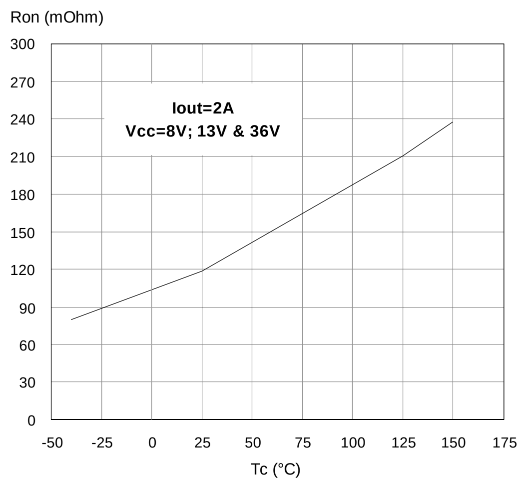


Figure 20. On State Resistance Vs V_{CC}

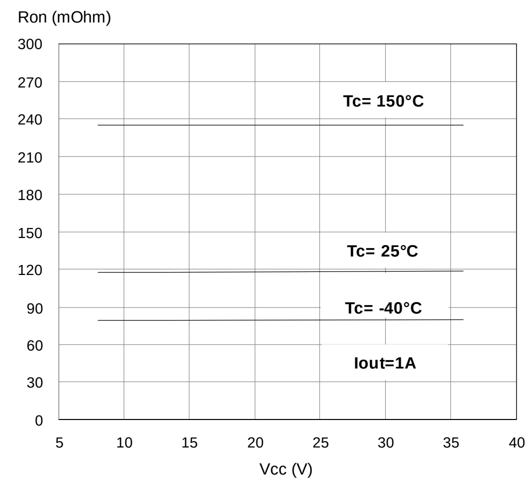


Figure 18. I_{LIM} Vs T_{case}

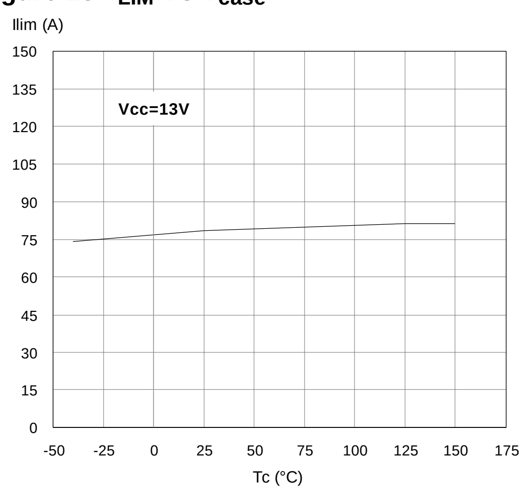


Figure 21. Input High Level

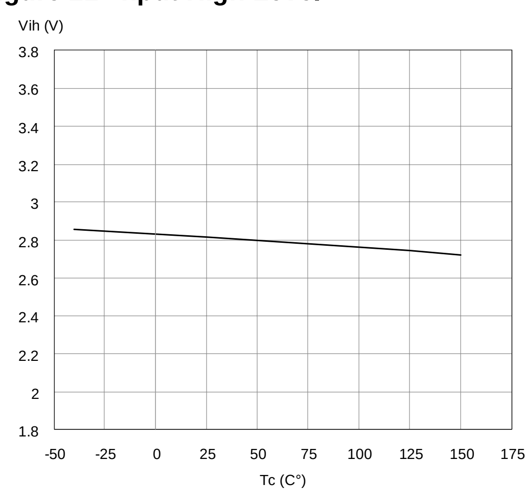


Figure 22. Openload On State Detection Threshold

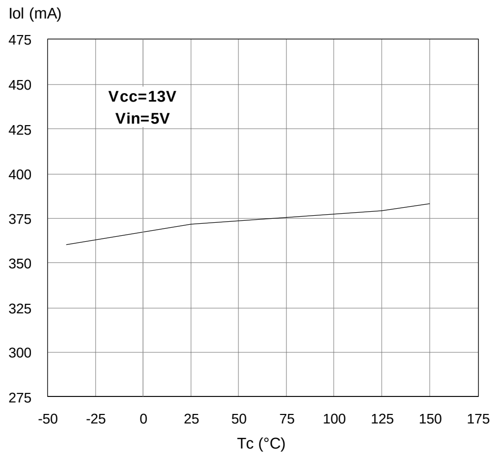


Figure 23. Input Hysteresis Voltage

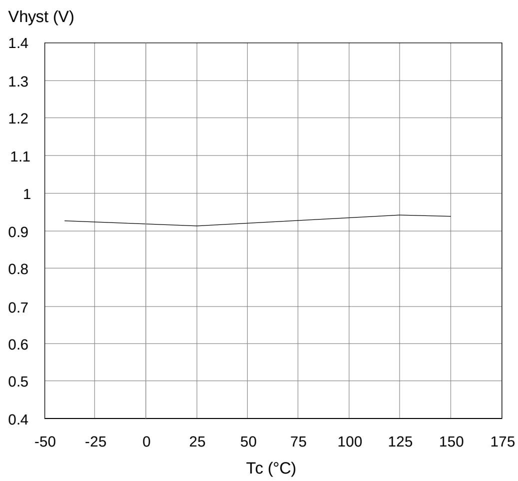


Figure 24. Overvoltage Shutdown

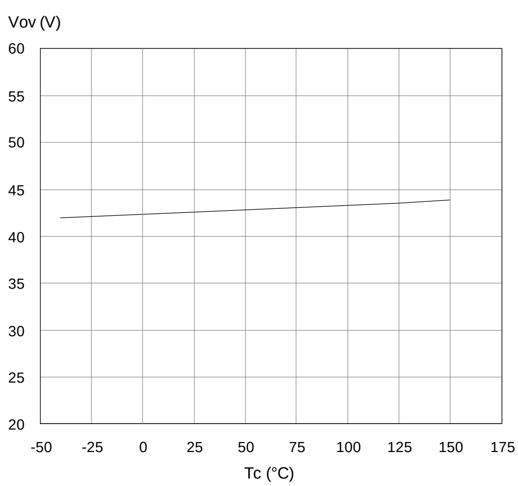


Figure 25. Openload Off State Detection Threshold

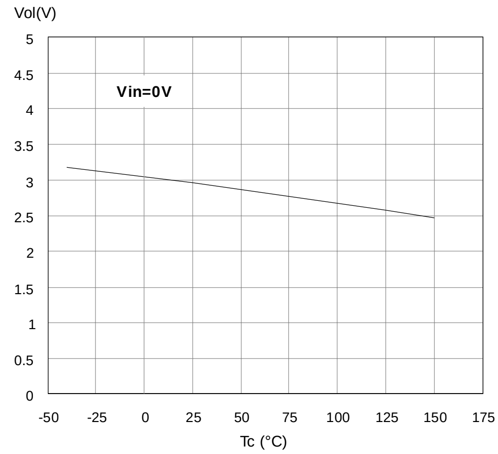


Figure 26. Input Low Level

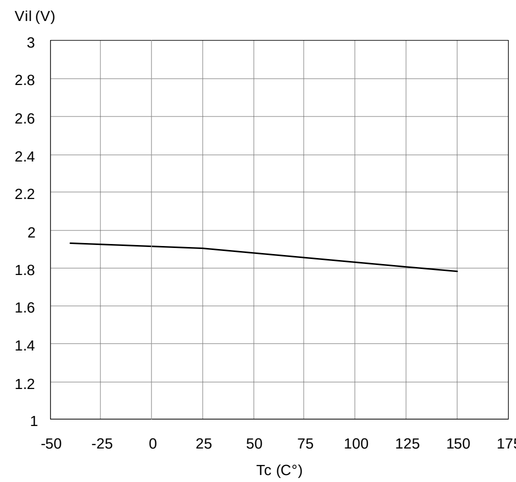
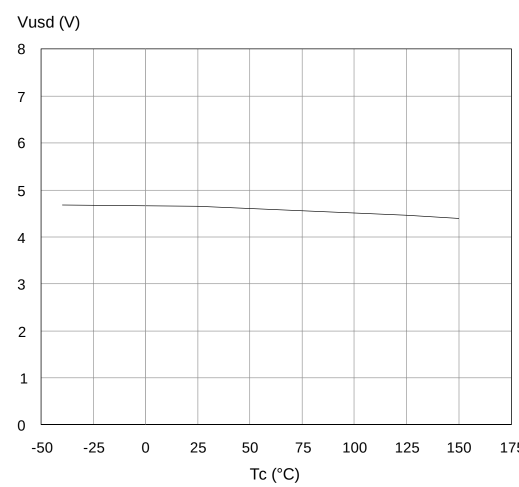
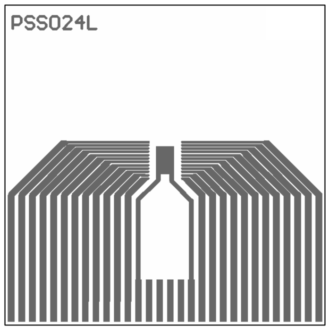


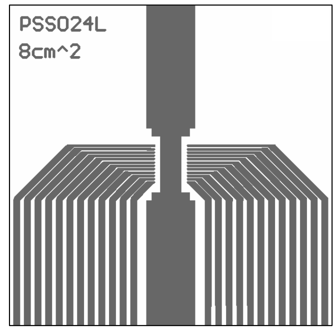
Figure 27. Undervoltage Shutdown



PowerSSO-24 Thermal Data

Figure 28. PowerSSO-24 PC Board





Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 78mm x 78mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 8cm^2).

Figure 29. $R_{thj-amb}$ Vs PCB Copper Area in Open Box Free Air Condition

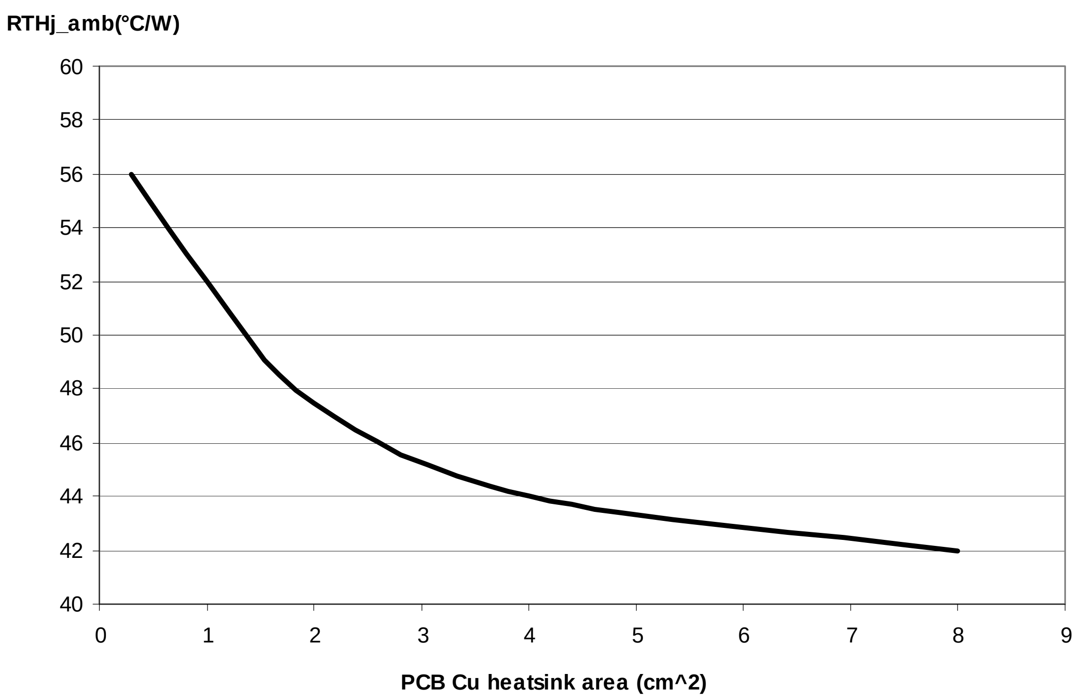


Figure 30. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse

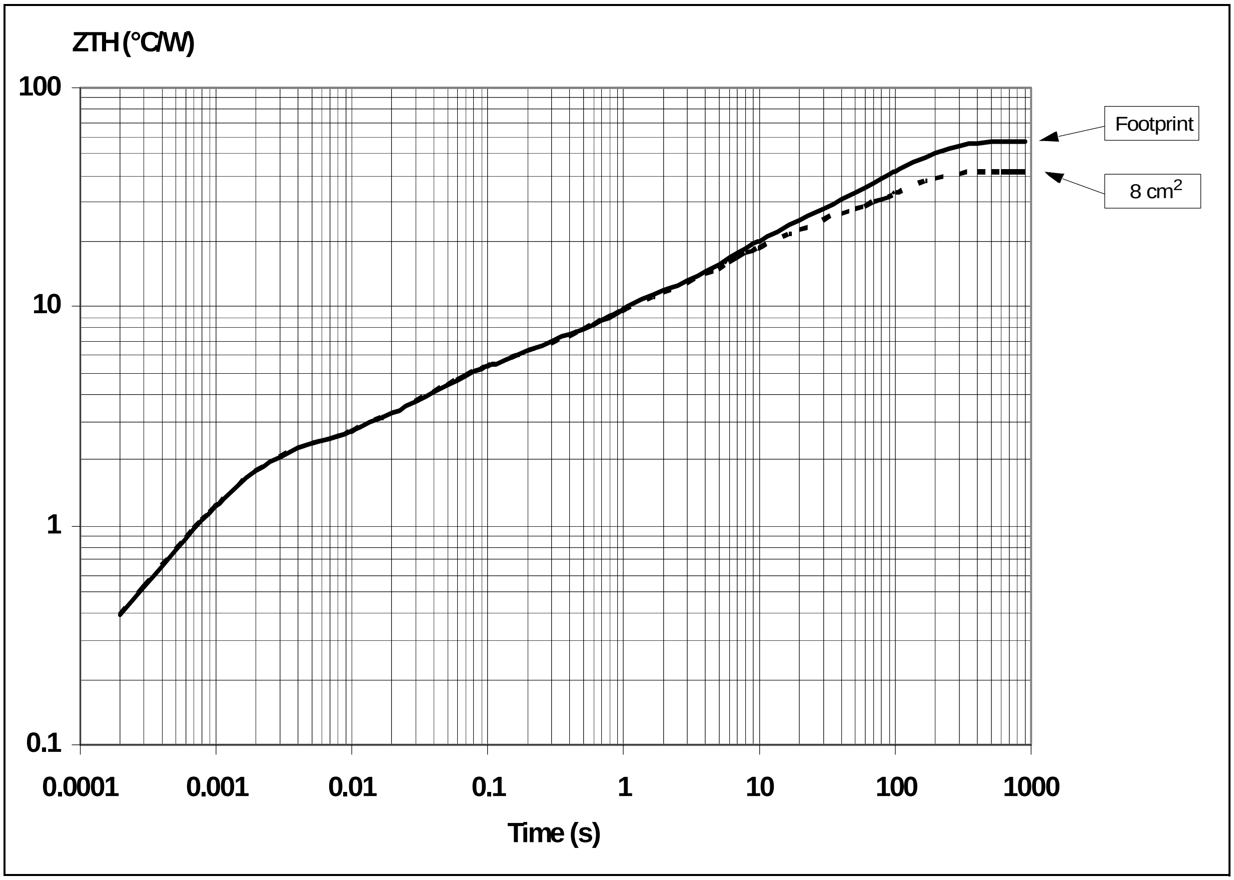
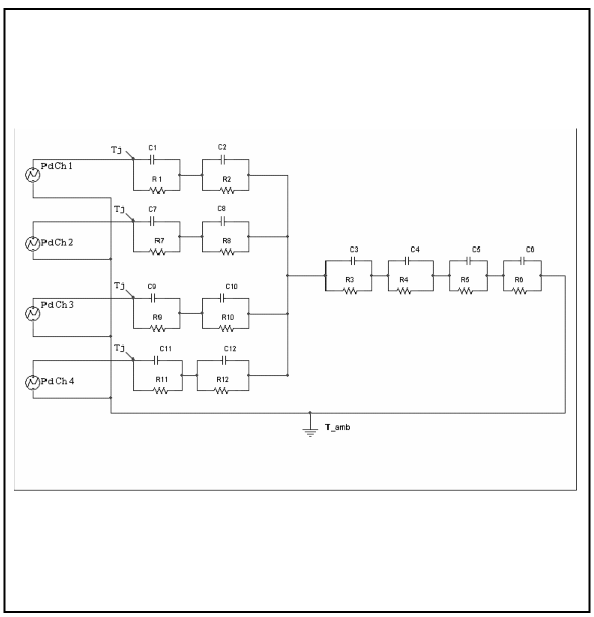


Figure 31. Thermal Fitting Model of a Quad Channel HSD in PowerSSO-24



Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 14. Thermal Parameter

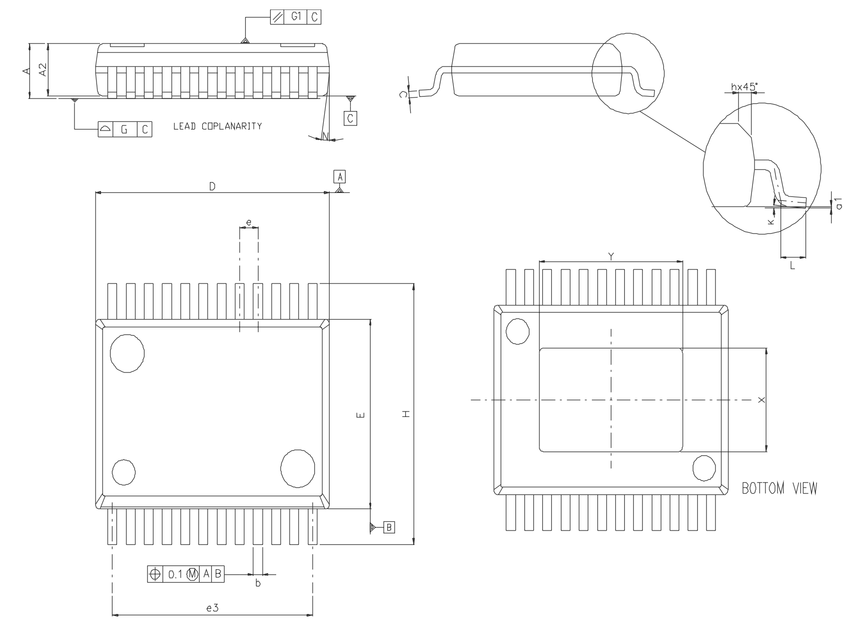
Area/island (cm^2)	Footprint	8
R1/R7/R11(°C/W)	25	
R2/R8(°C/W)	1.8	
R3(°C/W)	2.8	
R4 (°C/W)	4	
R5 (°C/W)	11	
R6 (°C/W)	37	22
R8/R10/R12 (°C/W)	1.8	
C1/C7/C9/C11(W.s/°C)	0.0001	
C2/C8/C10/C12(W.s/°C)	0.0007	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

PACKAGE MECHANICAL

Table 15. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 32. PowerSSO-24™ Package Dimensions



REVISION HISTORY

Table 16. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.
Nov. 2004	2	- Mechanical data updating. - PowerSSO-24 Thermal Charact. insertion
Dec. 2004	3	- Electrical Charact. curves insertion. - PC Board copper area correction.