SPECIFICATION FOR LCD MODULE

Model No. TM128128CCBWT4

Prepared by:	**Date:**
Checked by :	**Date:**
Verified by :	**Date:**
Approved by:	**Date:**

TIANMA MICROELECTRONICS CO., LTD

Ver 1.0

REVISION RECORD

Date	Ref. Page	Revision No.	Revision Items	Check & Approval

1. General Specifications:

1.1 Display type: FSTN

1.2 Display color*[1]:

Display color: Blue-Black

Background*[2]: White

1.3 Polarizer mode: Transflective/Positive

1.4 Viewing Angle: 12:00

1.5 Driving Method: 1/128 Duty 1/12Bias

1.6 Logic Voltage: 3.0V

LCD Operating Voltage: 12.3V

1.7 Backlight: EL

1.8CONTROLLER: S6B0741X01-23XN

1.9 Data Transfer: SERIAL/8 Bits Parallel

1.10 Operating Temperature: -20----+70℃

Storage Temperature: -30----+80℃

1.11 Outline Dimensions: Refer to outline drawing on the fifths page

1.12 Dot Matrix: 128 X 128 Dots

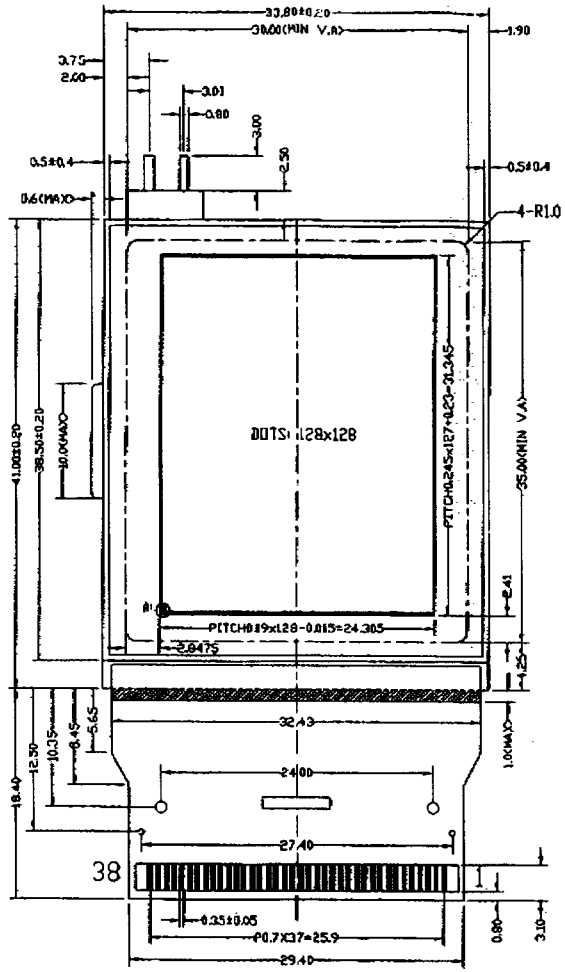
1.13 Dot Size: 0.225 X 0.175 (mm)

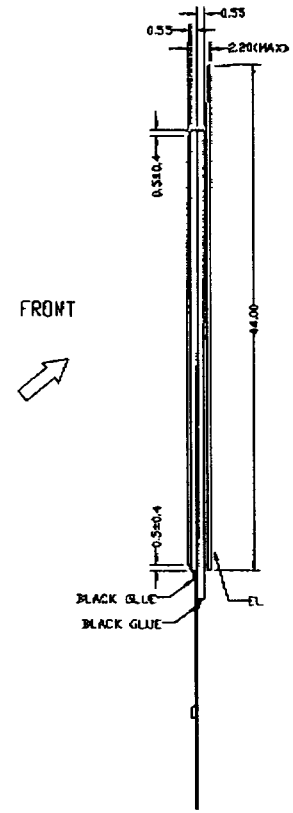
1.14 Dot Pitch: 0.245 X 0.19(mm)

1.15 Weight: 10g (Approx.)

*[1] Color tone is slightly changed by temperature and driving voltage.

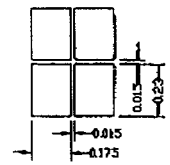
*[2] Color tone will be changed by backlight.





PIN	SYMBOL	PIN	SYMBOL
1	NC	20	VOUT
2	PS0	21	C5+
3	PS1	22	C3+
4	CSB	23	C1-
5	RESETB	24	C1+
6	RS	25	C2+
7	RW_WR	26	C2-
8	E_RD	27	C4+
9	DB0	28	REF
10	DB1	29	VEXT
11	DB2	30	INTRS
12	DB3	31	V4
13	DB4	32	V3
14	DB5	33	V2
15	DB6	34	V1
16	DB7	35	V0
17	VDD	36	VR
18	VCI	37	OSC1
19	VSS	38	NC

DETAIL A:



NOTES:

1. DISPLAY TYPE: FSTN
2. VIEWING DIRECTION: 6:00
3. POLARIZER MODE: TRANSFLECTIVE/POSITIVE
4. DRIVE METHOD: 1/128 DUTY 1/12 BIAS
5. LCD OPERATING VOLTAGE: 12.3V
6. VDD: 3.0V
7. OPERATING TEMP.: -20°C-70°C
8. STORAGE TEMP.: -30°C-80°C
9. CONTROLLER: S6B0741X01-30XN
10. BACKLIGHT: EL
11. UNMARKED TOLERANCE: ±0.30mm

TIAN-MA MICROELECTRONICS CO.

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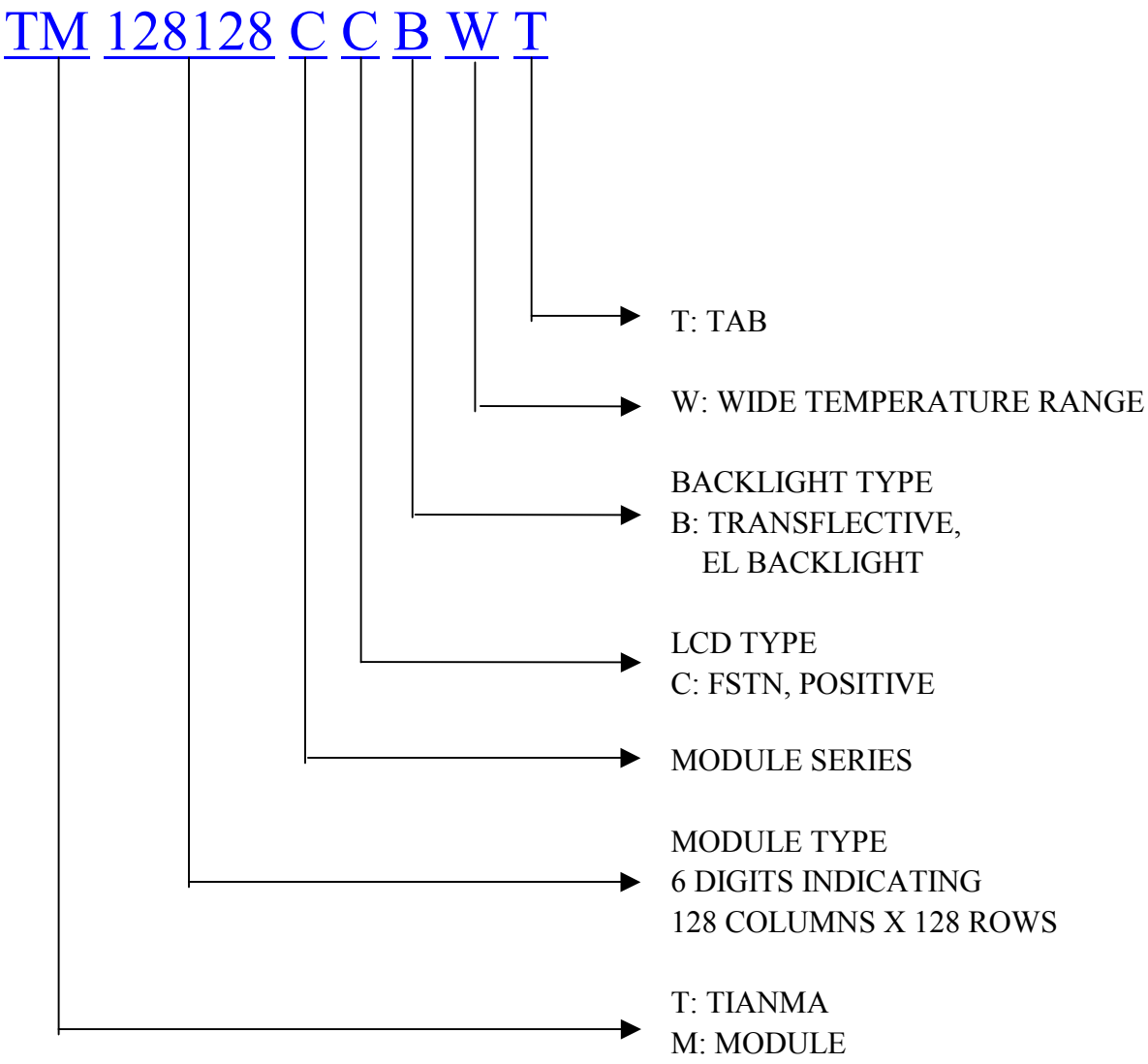
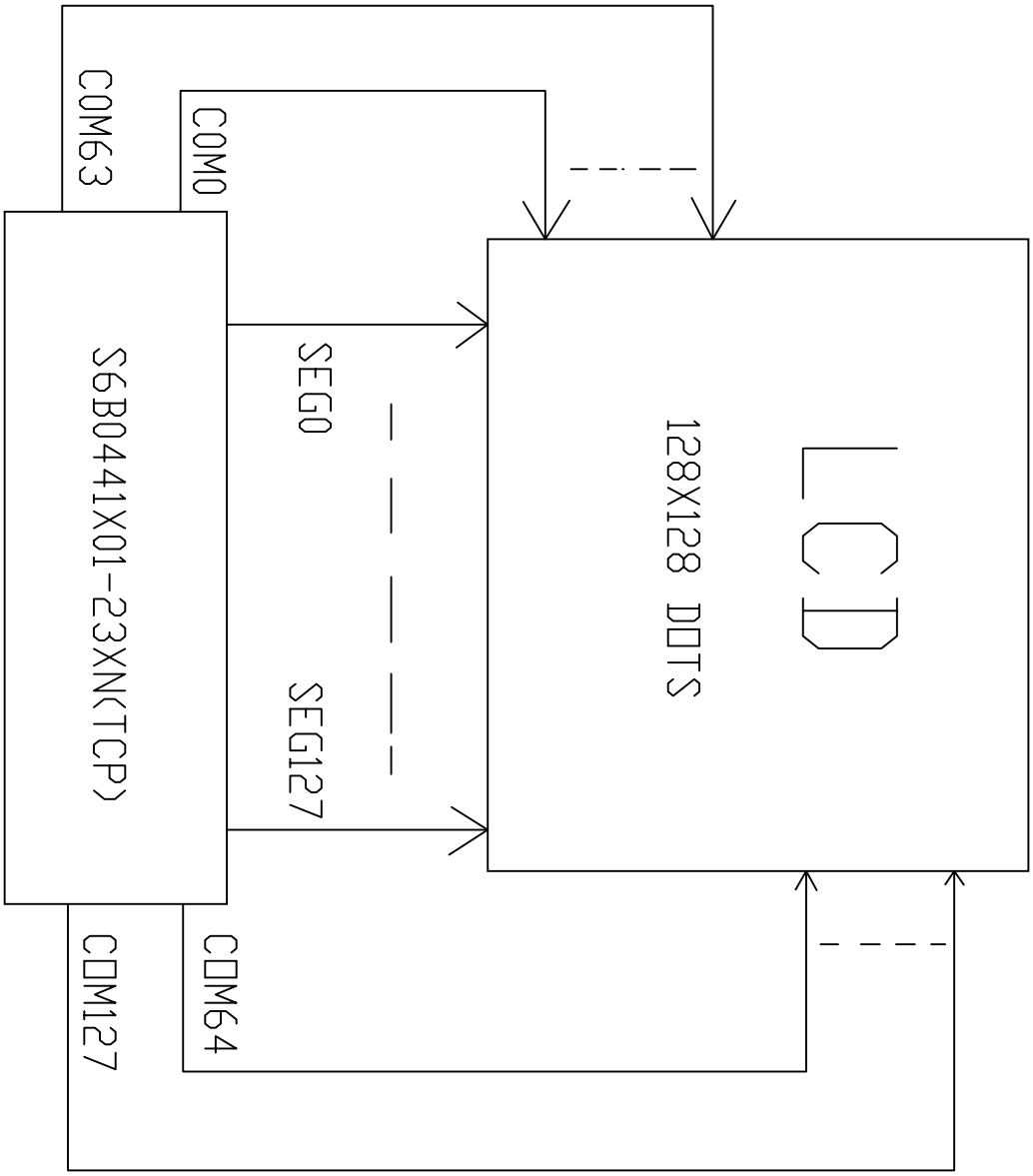
DRAWN BY:		TITLE: TM128128CCBWT4	
CHECKED BY:	9/8-03		
APPROVED BY:	9/8-03	DWG NO: G-1	SCALE:
CONFIRMED BY:		DWG NAME: TM128128CCBWT4G-1	UNIT: mm
			SHEET NO: 1 OF 1

3. LCD Module Part Numbering System



4. Circuit Block Diagram



5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	$V_{DD}-V_{SS}$	-0.3	7.0	V	
LCD Driving Voltage	V_{LCD}	-	17.0		
Operating Temperature Range	T_{OP}	-20	+70	℃	No Condensation
Storage Temperature Range	T_{ST}	-30	+80		

6. Electrical Specifications and Instruction Code

6.1 Electrical characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (Logic)		$V_{DD}-V_{SS}$	2.85	3.0	3.15	V
Supply Voltage (LCD Drive)		V_{LCD}	-	12.3	-	V
Input Signal Voltage	High	V_{IH} (V_{DD}=3.0V)	0.8V_{DD}	-	V_{DD}	V
	Low	V_{IL} (V_{DD}=3.0V)	0	-	0.2V_{DD}	V
Supply current (Logic) (Display character)		I_{DD} (V_{DD}-V_{SS}=3.0V)	-	-	500.0	uA
Supply current (LED)		I_{EL}	-	-	1.7	mA

6.2 Interface Signals

Pin No.	Symbol	Level	Description
1	NC	-	NO Signal
2	PS0	H/L	Parallel/Serial data input select input
3	PS1	H/L	Microprocessor interface select input pin PS0=H,PS1=H:6800-series parallel mpu interface PS0=H,PS1=L:8080-series parallel mpu interface PS0=L,PS1=H:4-pin-spi mpu interface PS0=L,PS1=L: 3-pin-spi mpu interface
4	CSB	H/L	Chip select input pins(Data/instruction I/O is enabled when csb is L)
5	RESETB	H/L	Reset input pin (when resetb is L,initialization is executed)
6	RS	H/L	Register select input pins RS=H:D0-7are display data;RS=L,D0-7 are control data
7	RW_WR	H/L	Read/Write execution control pin
8	E_RD	H/L	Read/Write execution control pin
9	DB0	H/L	Data bit0
10	DB1	H/L	Data bit1
11	DB2	H/L	Data bit2
12	DB3	H/L	Data bit3
13	DB4	H/L	Data bit4
14	DB5	H/L	Data bit5
15	DB6	H/L	Data bit6
16	DB7	H/L	Data bit7
17	VDD	3.0V	Power supply
18	VCI	H/L	Voltage converter input voltage pin
19	VSS	0V	Ground

20	VOUT	-	Voltage converter input/output pin
21	C5+	-	Capacitor 5 positive connection pin for voltage converter
22	C3+	-	Capacitor 3 positive connection pin for voltage converter
23	C1-	-	Capacitor1 negative connection pin for voltage converter
24	C1+	-	Capacitor 1 positive connection pin for voltage converter
25	C2+	-	Capacitor 2 positive connection pin for voltage converter
26	C2-	-	Capacitor 2 negative connection pin for voltage converter
27	C4+	-	Capacitor 4 positive connection pin for voltage converter
28	REF	H/L	Selects the external vref voltage via the vext pin REF=H:using the internal VREF REF=L:using the external VREF
29	VEXT	H/L	Externally input reference voltage for the internal voltage regulator,it is valid only when REF is L,When using internal voltage regulator,connect to VDD,Vss or open this pin
30	INTRS	H/L	Internal resistor select pin
31	V4	-	Bias voltage
32	V3	-	Bias voltage
33	V2	-	Bias voltage
34	V1	-	Bias voltage
35	V0	12.3V	Bias voltage
36	VR	-	V0 voltage adjustment pin
37	OSC1	-	When using internal clock oscillator,connect a resistor between OSC1 and VDD.
38	NC	-	No Signal

6.3 Interface Timing Chart

Serial Interface Characteristics

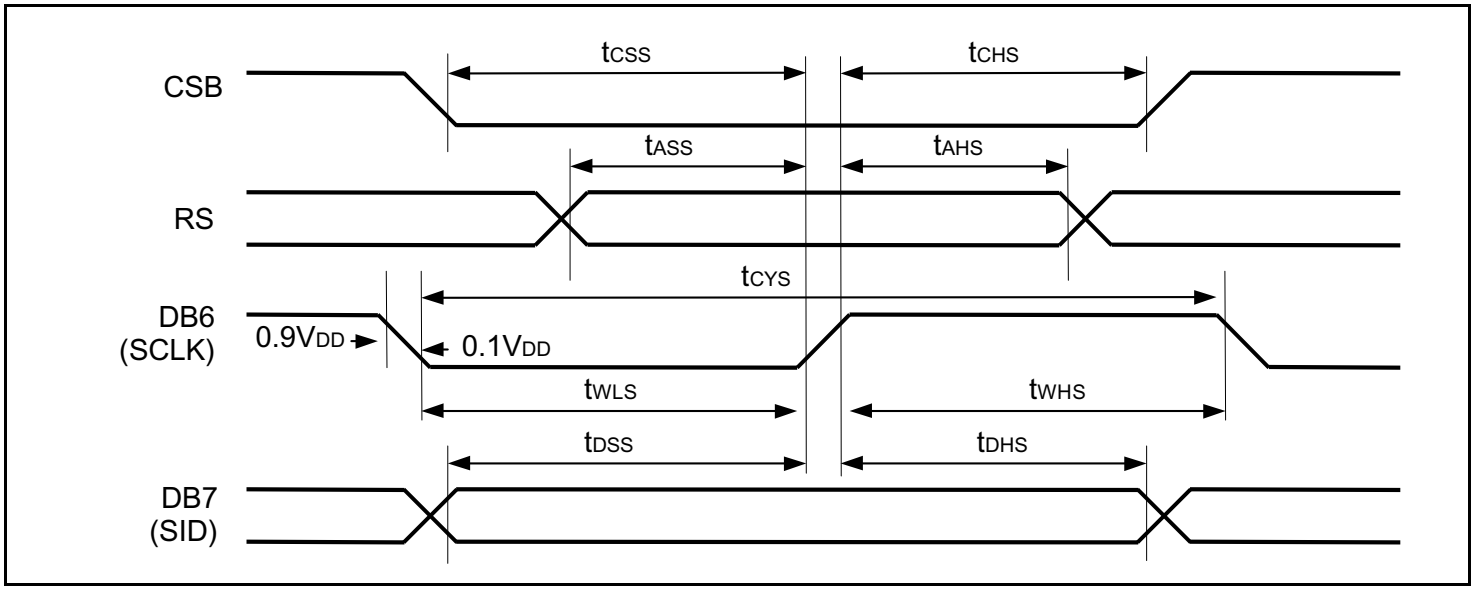


Figure 41. Serial Interface Characteristics

(V_{DD} = 1.8V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		111 60 60	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		60 60	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		60 60	- -	ns
CSB setup time CSB hold time	CSB	t_{CSS} t_{CHS}		60 1/2 * t_{CYS}	- -	ns

(V_{DD} = 2.7V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		58.8 30 30	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		30 30	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		30 30	- -	ns
CSB setup time CSB hold time	CSB	t_{CSS} t_{CHS}		30 1/2 * t_{CYS}	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

6.4 Instruction code

INSTRUCTION DESCRIPTION

Table 17. Instruction Table

×′ : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable (default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: display OFF D=1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×′	×′	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×′	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×′	×′	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×′	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×′	×′	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	×′	×′	2-byte instruction to set N-line inversion register
	0	0	×′	×′	×′	N4	N3	N2	N 1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line Inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display, REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display. EON=1: entire display ON

Table 17. Instruction Table (Continued)

×′ : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the Reference voltage
	0	0	×′	×′	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×′	×′	×′	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
Set data direction & display data length(DDL)	×′	×′	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI Mode)
	×′	×′	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	1	1	1	0	0	0	1	1	*No operation*
Test Instruction	0	0	1	1	1	1	×′	×′	×′	×′	*Don't use this instruction.*

Table 17. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 9PWM 0 1 9PWM 1 0 12PWM 1 1 15PWM
Set white mode and $1^{st}/2^{nd}$ frame, set pulse width	0	0	1	0	0	0	1	0	0	0	Set white mode and $1^{st}/2^{nd}$ frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	
Set white mode and $3^{rd}/4^{th}$ frame, set pulse width	0	0	1	0	0	0	1	0	0	1	Set white mode and $3^{rd}/4^{th}$ frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	
Set light gray mode and $1^{st}/2^{nd}$ frame, set pulse width	0	0	1	0	0	0	1	0	1	0	Set light gray mode and $1^{st}/2^{nd}$ frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	
Set light gray mode and $3^{rd}/4^{th}$ frame, set pulse width	0	0	1	0	0	0	1	0	1	1	Set light gray mode and $3^{rd}/4^{th}$ frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	
Set dark gray mode and $1^{st}/2^{nd}$ frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and $1^{st}/2^{nd}$ frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	
Set dark gray mode and $3^{rd}/4^{th}$ frame, set pulse width	0	0	1	0	0	0	1	1	0	1	Set dark gray mode and $3^{rd}/4^{th}$ frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	
Set black mode and $1^{st}/2^{nd}$ frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set black mode and $1^{st}/2^{nd}$ frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	
Set black mode and $3^{rd}/4^{th}$ frame, set pulse width	0	0	1	0	0	0	1	1	1	1	Set black mode and $3^{rd}/4^{th}$ frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	