

DMA2

DATA SHEET

SBus DMA Controller

DESCRIPTION

The STP2012 SBus DMA Controller (DMA2) provides three channels for DMA transfers over the SBus. It has three external interfaces designed to provide DMA access to one AMD Am7990 Local Area Network Controller for the Ethernet (LANCE), one NCR 53C90 SCSI controller (ESP), and one programmable Centronics-type parallel port. The STP2012 contains internal buffering for these DMA channels in the form of a cache for the LANCE interface and FIFOs for the ESP and parallel port interfaces. It also contains control/status registers for each of the three interfaces, several ESP and parallel port support registers, and a write buffer for slave accesses to the LANCE.

The STP2012 incorporates a number of features for increasing performance and allowing different modes of operation from earlier versions. Software enables additional features by changing the default values of appropriate mode bits in the control/status registers. By default, the STP2012 is software compatible with earlier versions.

FEATURES

- Supports 10 Mbyte/sec ESP transfers, 1.25 Mbyte/sec Ethernet transfers, and 4 Mbyte/sec parallel port transfers
- Supports 4-word, 8-word, and "no burst" SBus burst modes
- 64-byte internal cache for Ethernet data buffering
- 64-byte internal FIFOs for ESP and parallel port data buffering
- 16-bit write buffer for slave writes to LANCE
- Improved cache and FIFO draining algorithms for better SBus utilization
- Internal address and byte count registers and "NEXT" address/byte count features for data block chaining on ESP and parallel port interfaces
- JTAG test interface
- 160-pin PQFP package

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

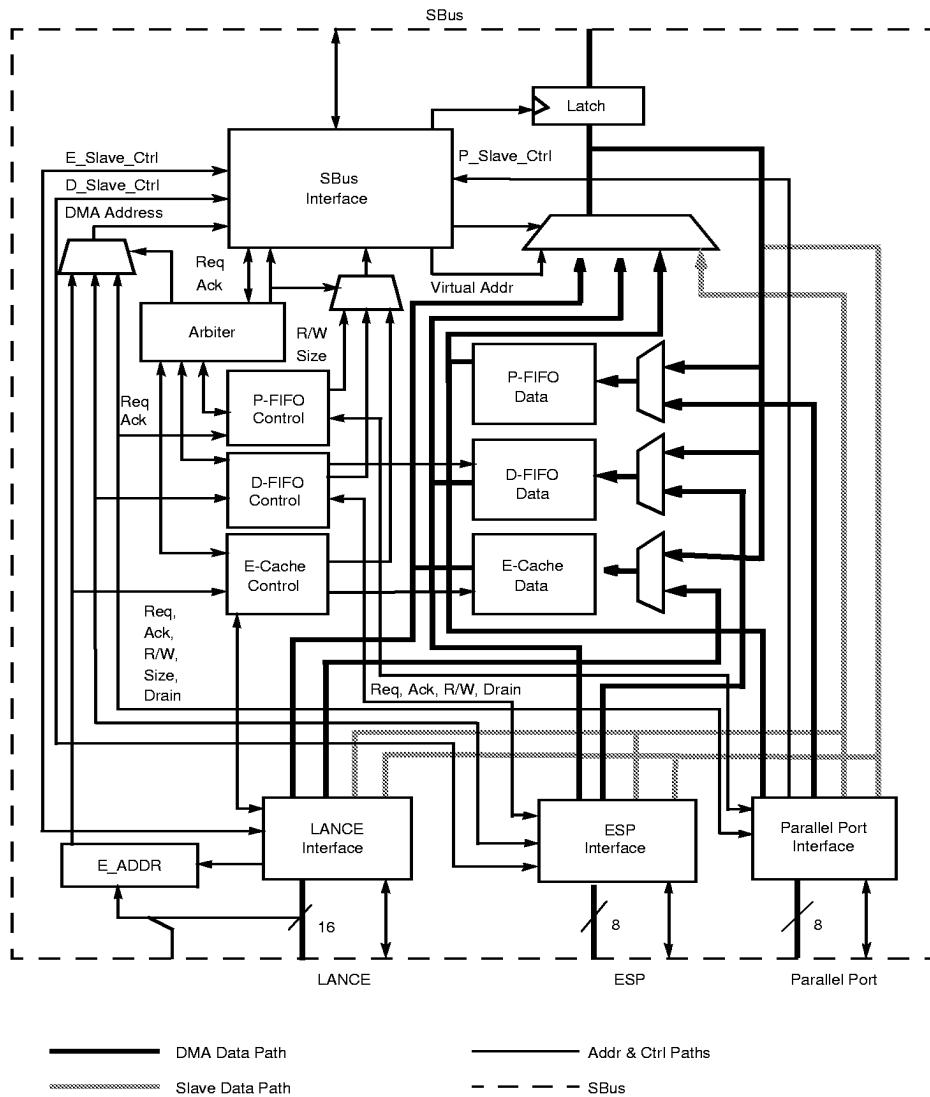


Figure 1. STP2012 Block Diagram

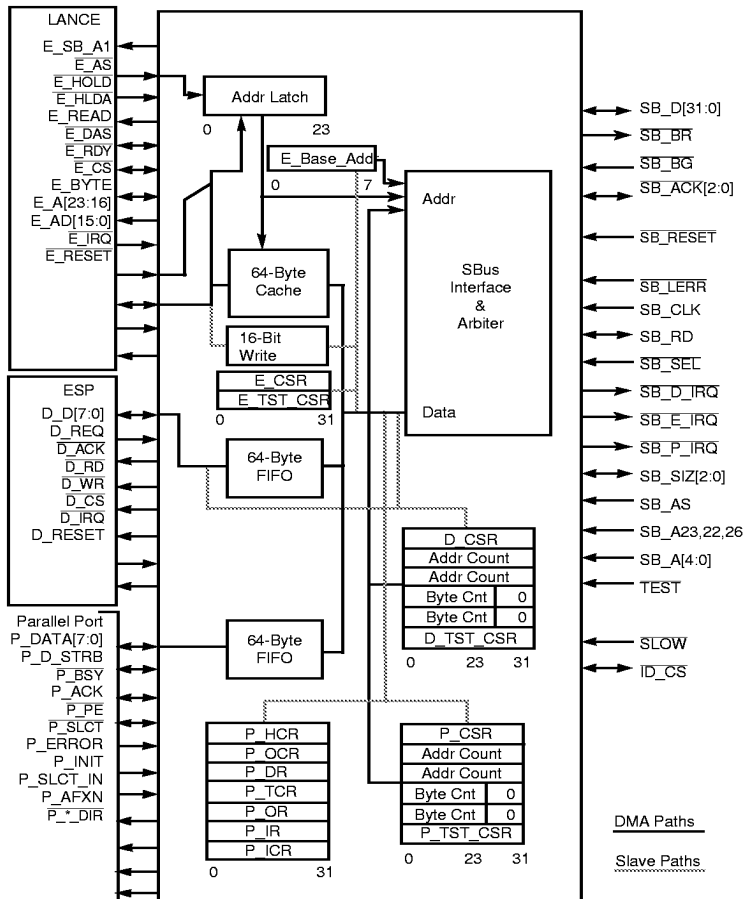


Figure 2. STP2012 Logical Connections

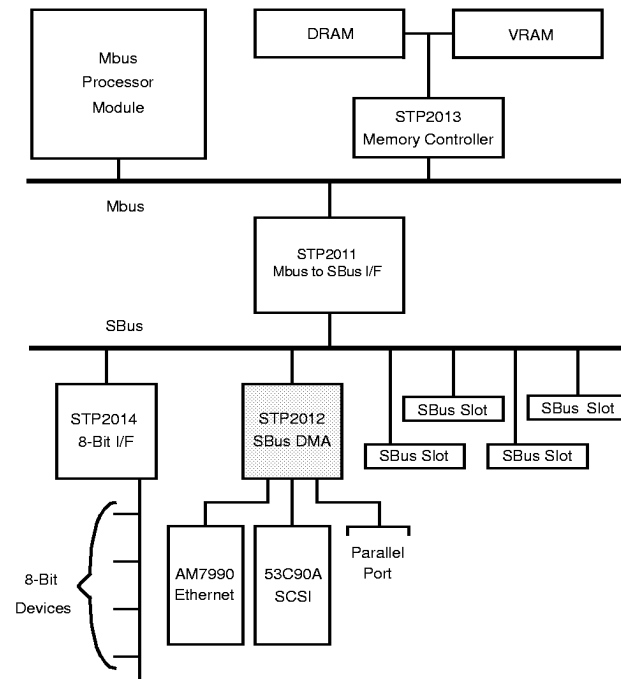


Figure 3. STP2012 Typical Application

SIGNAL DESCRIPTIONS

SBus Interface

Signal	Type	Description
SB_A[4:0]	Input	Low order physical address bits
SB_ACK[2:0]	Input/Output	SBus acknowledge
SB_AS	Input	SBus address strobe
SB_AX	Input	High-order physical address bit (for slave decodes)
SB_AY	Input	High-order physical address bit
SB_AZ	Input	High-order physical address bit
SB_BG	Input	SBus bus grant
SB_BR	Output	SBus bus request
SB_CLK	Input	SBus clock
SB_D[31:0]	Input/Output	SBus data bus
SB_D_IRQ	Input/Output	SBus interrupt for ESP transfers
SB_E_IRQ	Input/Output	SBus interrupt for LANCE transfers
SB_LERR	Input	SBus late error (INT15)
SB_P_IRQ	Input/Output	SBus interrupt for parallel port transfers
SB_RD	Input/Output	SBus read/write
SB_RESET	Input	SBus reset
SB_SEL	Input	SBus select
SB_SIZ[2:0]	Input/Output	SBus transfer size

LANCE Interface

Signal	Type	Description
E_A[23:16]	Input	LANCE high order address
E_AD[15:0]	Input/Output	LANCE address/data bus
E_AS	Input	LANCE address strobe
E_BYTE	Input	LANCE byte marker
E_CS	Output	LANCE chip select
E_DAS	Input/Output	LANCE data strobe
E_HLDA	Output	LANCE hold acknowledge
E_HOLD	Input	LANCE hold
E_IRQ	Input	LANCE interrupt request
E_RDY	Input/Output	LANCE ready
E_READ	Input/Output	LANCE read
E_RESET	Output	LANCE reset
E_SB_A1	Output	Buffered version of SBA1 for LANCE

ESP Interface

Signal	Type	Description
D_ACK	Output	ESP DMA acknowledge
D_CS	Output	ESP chip select
D_D[7:0]	Input/Output	ESP data bus
D_IRQ	Input	ESP interrupt request
D_RD	Output	ESP read strobe
D_REQ	Input	ESPI DMA request
D_RESET	Output	ESP reset
D_WR	Output	ESP write strobe
ID_CS	Input/Output	Secondary device select (boot PROM)

Parallel Port Interface

Signal	Type	Description
P_ACK	Input/Output	Parallel port acknowledge
P_ACK_DIR ^[1]	Output	Parallel port acknowledge direction
P_AFXN	Output	Parallel port auto feed
P_BSY	Input/Output	Parallel port busy
P_BSY_DIR ^[1]	Output	Parallel port busy direction
P_DATA[7:0]	Input/Output	Parallel port data bus
P_D_DIR ¹	Output	Parallel port data direction
P_DS_DIR ¹	Output	Parallel port data strobe direction
P_DS_TRB	Input/Output	Parallel port data strobe
P_ERROR	Input	Parallel port error
P_INIT	Output	Parallel port initialize
P_PE	Input	Parallel port paper error
P_SLCT	Input	Parallel port select
P_SLCT_IN	Output	Parallel port select in

1. The parallel port direction bits, P_ACK_DIR, P_BSY_DIR, P_D_DIR, and P_DS_DIR, have the following polarity: asserted (P*_DIR=0) sets transfer direction toward the STP2012, unasserted (P*_DIR=1) sets transfer direction away from the STP2012.

Miscellaneous

Signal	Type	Description
B_SB_CLK	Output	Buffered SBus clock output
CONFIG	Input	Package selection
JTAGCLK	Input	JTAG clock
JTAGDI	Input	JTAG data input
JTAGDO	Output	JTAG data output
JTAGTMS	Input	JTAG test mode select
SLOW	Input	Fast (high) or slow (low) DMA acknowledge cycles
TEST	Input	Test control. Low enables BSBCLK as parametric test output and 3-states all 3-statable outputs and bidirectionals
TP_AUI	Output	Ethernet select output

ELECTRICAL SPECIFICATIONS***Absolute Maximum Ratings***^[1]

Symbol	Parameter	Min	Max	Units
V _{CC}	DC supply	-0.3	7.0	V
V _{IN}	Input voltage	-0.3	GND ≤ V _{IN} ≤ V _{CC}	V
I _{IN}	DC input current	-10	+10	mA
T _{STG}	Storage temperature range (plastic)	-40	125	°C

1. Referenced to GND.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V _{CC}	DC supply	4.75	5.25	V
T _A	Ambient temperature	0	70	°C

DC Characteristics

Symbol	Parameter	Conditions ^[1]	Min	Typ	Max	Units
V _{IH}	Voltage input high	4.75 < V _{CC} < 5.25	2.0	—	—	V
V _{IL}	Voltage input low	4.75 < V _{CC} < 5.25	—	—	0.8	V
V _{OH}	Voltage output high	I _{OH} = -4.0, -8.0 mA	2.4	4.5	—	V
V _{OL}	Voltage output low	I _{OL} = 4.0, 8.0 mA	—	0.2	0.4	V
I _{IL}	Current input leakage	V _{CC} = MAX, V _{IN} = V _{CC} or GND	-10	±1	10	μA
I _{IPU}	Current input pull-up	V _{CC} = MAX, V _{IN} = GND or 3.5 V	-175	—	-2	μA
I _{IPD}	Current input pull-down	V _{CC} = MAX, V _{IN} = GND or 0.8 V	2	—	179	μA
I _{OZ}	Current 3-state output leakage	V _{CC} = MAX, V _{OUT} = GND or V _{CC}	-10	±1	10	μA
I _{OZU}	Current 3-state output w/ pull-up	V _{OUT} = GND or 3.5 V	-175	—	-2	μA
I _{OZD}	Current 3-state output w/ pull-down	V _{OUT} = GND or 0.8 V	2	—	179	μA
I _{OSP4}	Current P-channel output short circuit (4 mA output buffers) ^[2]	V _{CC} = MAX, V _{OUT} = GND	-140	-70	-25	mA
I _{OSN4}	Current N-channel output short circuit (4 mA output buffers) ^[2]	V _{CC} = MAX, V _{OUT} = V _{CC}	30	75	140	mA
I _{DD}	Quiescent supply current	V _{IN} = V _{CC} or GND	—	—	2	mA
I _{CC}	Dynamic supply current	V _{CC} = MAX, f = 25 MHz	—	125	200	mA

1. Specified at V_{CC} equals 5V ± 5% at ambient temperature over the specified range.

2. Not more than one output may be shorted at a time for a maximum duration of one second.

Capacitance

Symbol	Parameter	Condition	Min	Max	Units
C _{IN}	Input capacitance	CLK input	V _{IN} = 5.0 V, T _A = 25°C, f = 1 MHz	12	pF
		All other inputs	V _{IN} = 5.0 V, T _A = 25°C, f = 1 MHz	6	pF
C _{OUT}	Output capacitance	V _{IN} = 5.0 V, T _A = 25°C, f = 1 MHz	5.5	pF	
C _{BID}	Bidirectional capacitance	V _{IN} = 5.0 V, T _A = 25°C, f = 1 MHz	6	pF	

AC Characteristics: Output Delay Timing

Signal Relative to SB_CLK	Output Delay (ns)
B_SB_CLK	39
D_ACK	30
D_CS	30
D_D[7:0]	30
D_RD	30
D_RESET	30
D_WR	30
E_AD[15:0]	30
E_CS	30
E_DAS	30
E_HLDA	30
E_RDY	30
E_READ	30
E_RESET	30
E_SB_A1	30
ID_CS	30
JTAGDO	30
TP_AUI	30
P_ACK	30
P_ACK_DIR	30
P_AFXN	30
P_BSY	30
P_BSY_DIR	30
P_DATA[7:0]	30
P_DS_DIR	34
P_D_DIR	30
P_D_STRB	30
P_INIT	30
P_SLCT_IN	30
SB_ACK[2:0]	26
SB_BR	26
SB_D[31:0]	26
SB_D_IRQ	26
SB_E_IRQ	26
SB_P_IRQ	26
SB_RD	26
SB_SIZ[2:0]	26

The following table lists the minimum setup and hold time of each output or bidirectional signal relative to SB_CLK. The second and third columns contain the setup and hold time measured from the *rising* edge of each signal to the rising edge of SB_CLK. The fourth and fifth columns contain the same times but measured from the *falling* edge of each signal to the rising edge of SB_CLK.

AC Characteristics: Setup and Hold Times

Signal Relative to SB_CLK	Rising Edge		Falling Edge	
	Setup (Min)	Hold (Min)	Setup (Min)	Hold (Min)
CONFIG	15	3	15	3
D_D[7:0]	15	3	15	3
D_IRQ	15	3	15	3
D_REQ	15	3	15	3
E_A[23:16]	15	3	15	3
E_AD[15:0]	15	3	15	3
E_AS	15	10	15	10
E_BYTE	15	10	15	10
E_DAS	15	10	15	10
E_HOLD	15	10	15	10
E_IRQ	15	10	15	10
E_RDY	15	10	15	10
E_READ	15	10	15	10
ID_CS	15	3	15	3
JTAGCLK	15	3	15	3
JTAGDI	15	3	15	3
JTAGTMS	15	3	15	3
P_ACK	15	3	15	3
P_BSY	15	3	15	3
P_DATA[7:0]	15	3	15	3
P_D_STRB	15	3	15	3
P_ERROR	15	3	15	3
P_PE	15	3	15	3
P_SLCT	15	3	15	3
SB_A[4:0]	15	3	15	3
SB_ACK	15	3	15	3
SB_AS	15	3	15	3
SB_AX	15	3	15	3

AC Characteristics: Setup and Hold Times (Continued)

Signal Relative to SB_CLK	Rising Edge		Falling Edge	
	Setup (Min)	Hold (Min)	Setup (Min)	Hold (Min)
SB_AY	15	3	15	3
SB_AZ	15	3	15	3
SB_BG	15	3	15	3
SB_D[31:0]	15	3	15	3
SB_D_IRQ	15	3	15	3
SB_E_IRQ	15	3	15	3
SB_LERR	15	3	15	3
SB_RD	15	3	15	3
SB_RESET	38	1	38	1
SB_SEL	15	3	15	3
SB_SIZ[2:0]	15	3	15	3
SLOW	15	3	15	3
TEST	38	1	38	1

TIMING DIAGRAM

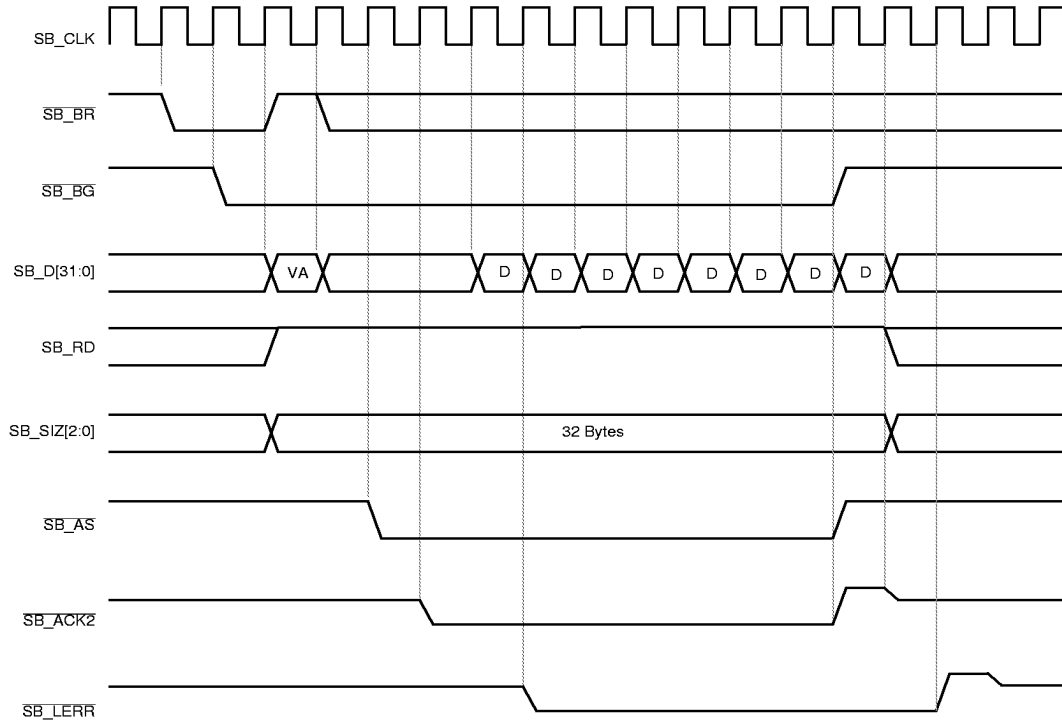


Figure 4. SBus DMA Burst Read

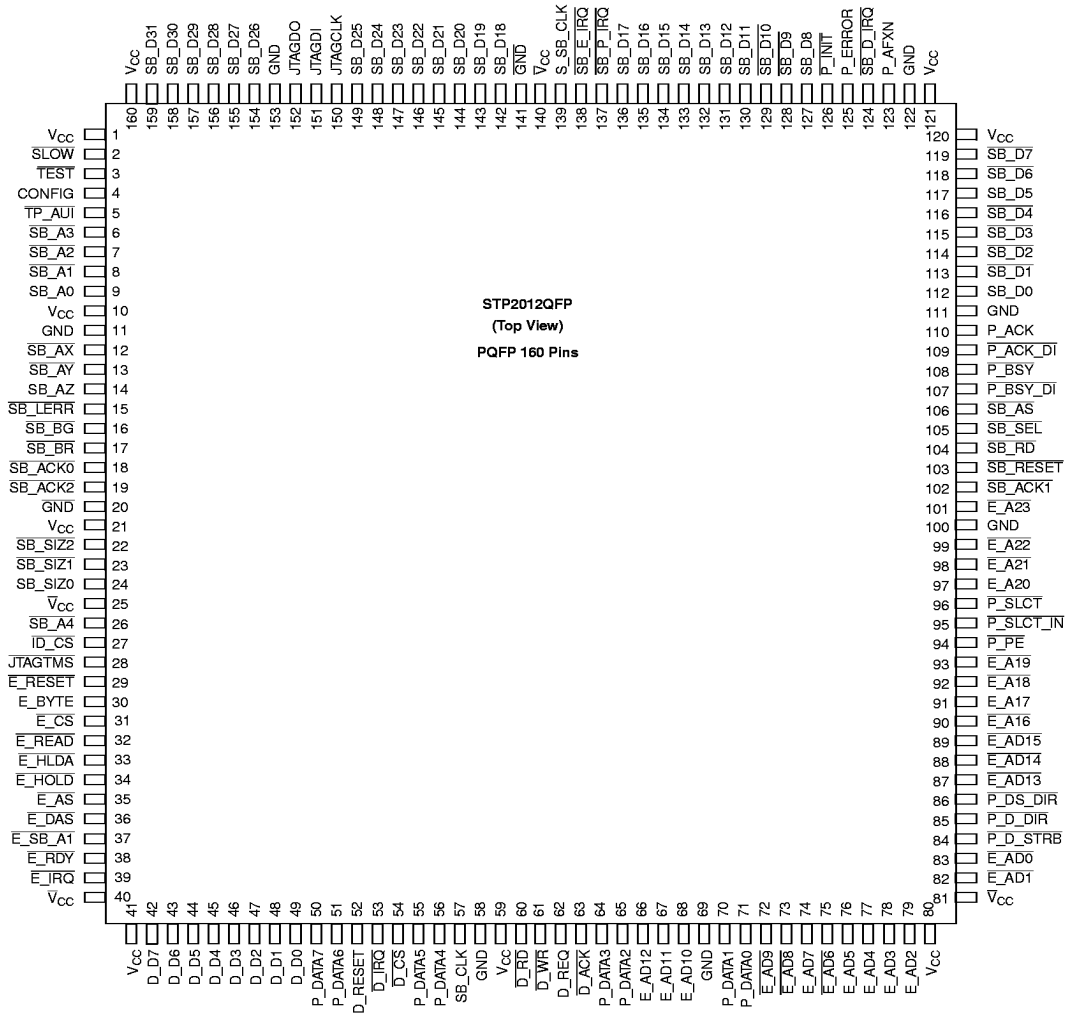
STP2012QFP

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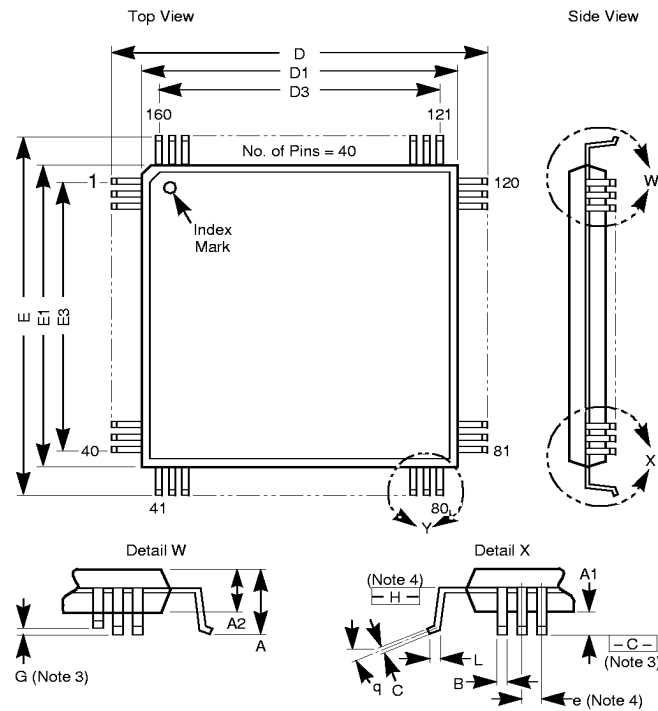
PACKAGE INFORMATION

160-Pin PQFP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	V _{CC}	33	E_HLDA	65	P_DATA2	97	E_A20	129	SB_D10
2	SLOW	34	E_HOLD	66	E_AD12	98	E_A21	130	SB_D11
3	TEST	35	E_AS	67	E_AD11	99	E_A22	131	SB_D12
4	CONFIG	36	E_DAS	68	E_AD10	100	GND	132	SB_D13
5	TP_AUI	37	E_SB_A1	69	GND	101	E_A23	133	SB_D14
6	SB_A3	38	E_RDY	70	P_DATA1	102	SB_ACK1	134	SB_D15
7	SB_A2	39	E_JRQ	71	P_DATA0	103	SB_RESET	135	SB_D16
8	SB_A1	40	V _{CC}	72	E_AD9	104	SB_RD	136	SB_D17
9	SB_A0	41	V _{CC}	73	E_AD8	105	SB_SEL	137	SB_P_JRQ
10	V _{CC}	42	D_D7	74	E_AD7	106	SB_AS	138	SB_E_JRQ
11	GND	43	D_D6	75	E_AD6	107	P_BSY_DIR	139	S_SB_CLK
12	SB_AX	44	D_D5	76	E_AD5	108	P_BSY	140	V _{CC}
13	SB_AY	45	D_D4	77	E_AD4	109	P_ACK_DIR	141	GND
14	SB_AZ	46	D_D3	78	E_AD3	110	P_ACK	142	SB_D18
15	SB_LERR	47	D_D2	79	E_AD2	111	GND	143	SB_D19
16	SB_BG	48	D_D1	80	V _{CC}	112	SB_D0	144	SB_D20
17	SB_BR	49	D_D0	81	V _{CC}	113	SB_D1	145	SB_D21
18	SB_ACK0	50	P_DATA7	82	E_AD1	114	SB_D2	146	SB_D22
19	SB_ACK2	51	P_DATA6	83	E_AD0	115	SB_D3	147	SB_D23
20	GND	52	D_RESET	84	P_D_STRB	116	SB_D4	148	SB_D24
21	V _{CC}	53	D_JRQ	85	P_D_DIR	117	SB_D5	149	SB_D25
22	SB_SIZ2	54	D_CS	86	P_DS_DIR	118	SB_D6	150	JTAGCLK
23	SB_SIZ1	55	P_DATA5	87	E_AD13	119	SB_D7	151	JTAGDI
24	SB_SIZ0	56	P_DATA4	88	E_AD14	120	V _{CC}	152	JTAGDO
25	V _{CC}	57	SB_CLK	89	E_AD15	121	V _{CC}	153	GND
26	SB_A4	58	GND	90	E_A16	122	GND	154	SB_D26
27	ID_CS	59	V _{CC}	91	E_A17	123	P_AFXN	155	SB_D27
28	JTAGTMS	60	D_RD	92	E_A18	124	SB_D_JRQ	156	SB_D28
29	E_RESET	61	D_WR	93	E_A19	125	P_ERROR	157	SB_D29
30	E_BYTE	62	D_REQ	94	P_PE	126	P_INIT	158	SB_D30
31	E_CS	63	D_ACK	95	P_SLCT_IN	127	SB_D8	159	SB_D31
32	E_READ	64	P_DATA3	96	P_SLCT	128	SB_D9	160	V _{CC}



160-Pin PQFP Package Dimensions

**Note:**

1. Total number of pins is 160.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ± 0.200 mm.

Dimension		mm
A	Max	4.01
	Min	0.25
A1	Max	0.36
A2	Min	3.17
	Nom	3.42
	Max	3.65
B	Min	0.22
	Max	0.38
C	Min	0.13
	Max	0.23
D	Min	31.60
	Nom	32.00
	Max	32.40
D1	Min	27.90
	Nom	28.00
	Max	28.10
D3	Ref	25.35
e	BSC	0.65
E	Min	31.60
	Nom	32.00
	Max	32.40
E1	Min	27.90
	Nom	28.00
	Max	28.10
E3	Ref	25.35
L	Min	0.65
	Nom	0.80
	Max	0.95
q	Min	0°
	Max	7°

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SBus DMA Controller

STP2012QFP

ORDERING INFORMATION

Part Number	Description
STP2012PQFP	160-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2012

July 1997

SUN MICROELECTRONICS

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