EG&G RETICON

SI Series
PtSi Solid State Line Scanners

General Description

Reticon has successfully combined the advantages of thin-film platinum silicide Schottky-barrier diode (PtSi SBD) technology with self-scanned readout methods to produce a self-scanned PtSi infrared linear array for scientific applications. This device is available in a standard 34-pin dual-inline ceramic package (which accommodates backside-illumination of the chip and simplifies the cryogenic cooling requirement) as shown in Figure 1. Table 1 shows the pin definition of the PtSi "SI" series arrays.

Since the substrate material is silicon, backside-illumination of the chip has the inherent advantage of blocking the visible and very near infrared photons (i.e., by absorption) from reaching the photo-detector area. In addition, long wavelength infrared photons lack sufficient energy to excite carriers to jump the metal-semiconductor (i.e., Schottky) barrier thus limiting the photoresponse from the shortwave infrared (SWIR) to the midwave infrared (MWIR) spectral region. The result is an array which is sensitive to wavelengths from 1.1 to 5 µm without the need for external filters.

The array comes in two sizes, 1024 and 512 elements. Each element of the array is 25 µm wide and 2500 µm long giving each a slit-like 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. Applications for this array include: IR spectroscopy, remote sensing, push-broom imaging, and industrial temperature monitoring.

Key Features

- PtSi Schottky-barrier diode
- 1024 and 512 element IR linear array
- 25 µm pixel-to-pixel spacing
- 2.5 mm pixel length
- 60% fill factor
- 1.1 to 5 µm infrared spectral response
- Self-scanned structure
- Excellent element-to-element nonuniformity: <1% rms

Sensor Characteristics

The photosensing area of this device is composed of an array of thin-film PtSi SBDs. The pixel-to-pixel spacing is 25 µm. The pixel length is 2.5 mm. Each PtSi SBD is surrounded by an n^+ guard ring for suppressing leakage current. A channel stop is used to separate two adjacent pixels. Figure 2 shows the sensor geometry. The photo sensitive area of each pixel is 15 µm x 2500 µm. The length of the sensor elements is 2.5 mm giving each element a slit-like geometry with 100:1 aspect ratio suitable for coupling to monochromators or spectrographs. Figure 3 shows the typical spectral response and quantum efficiency.

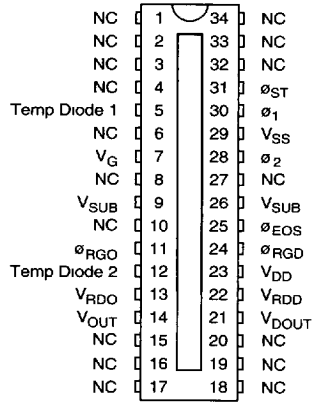

Figure 1. Pinout Configuration

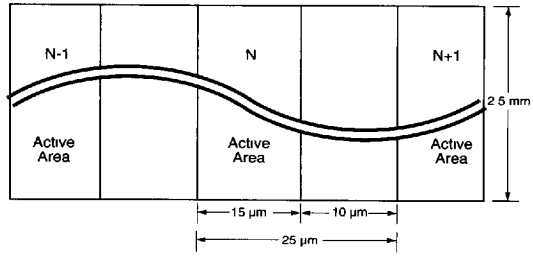

Figure 2. Sensor Geometry

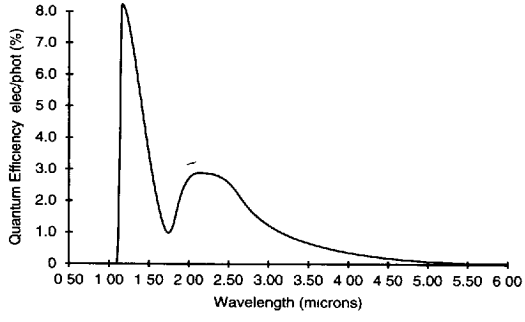

Figure 3. Absolute Quantum Efficiency versus Wavelength. Typical Reticon PtSi SBD shown. Optical cavity peaked for 3.5 µm wavelength.

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Operation

In order to understand the operation of the PtSi SBD array, it is helpful to know some of the similarities and differences that exist between a p-n junction diode and an SBD detector. The SBD operates in the storage mode just like the p-n junction diode. Its capacitance per unit area is about the same as the p-n junction diode and they both have a similar voltage compliance. Therefore, the saturation charge is comparable for similar diode areas. The SBD also has reverse bias characteristics similar to the p-n junction, however, its dark leakage current is several orders of magnitude larger than that of a p-n junction of the same area at the same temperature. As a result it is necessary to cool the SBD array in order to reduce the dark leakage current to a negligible value. In order to realize reasonable integration times, the array must be operated near liquid nitrogen temperatures (i.e., 77°K).

Both the SBD and the p-n junction diode are photon detectors. However, they differ significantly in sensitivity. In the visible and very near infrared region, photons are absorbed in the bulk silicon and a p-n junction will collect charge generated up to a distance of a diffusion length. As a result, a p-n junction detector has a collection volume much larger than the actual depletion region of the junction. In contrast to this, photons in the infrared spectral region are not absorbed in the bulk silicon but only in the thin silicide film, therefore, the collection volume of a SBD is much smaller than that of a p-n junction detector. This is one reason for the much lower sensitivity of the SBD as compared to the p-n junction detector of equal surface area.

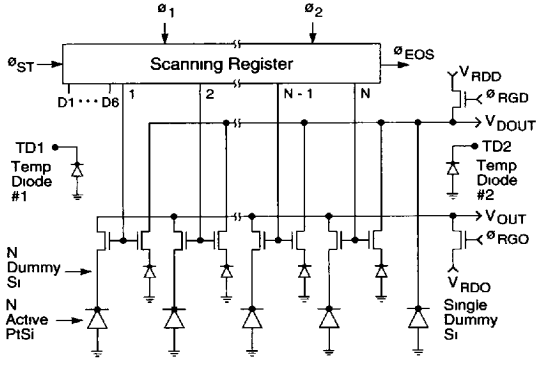

Figure 4. Equivalent Circuit

Scanning Circuit

The simplified equivalent circuit of an SI Series PtSi array is shown in Figure 4. Each cell consists of an active SBD photodiode and a dummy photodiode, both with an associated storage capacitance. These diodes are connected through MOS multiplex switches to active and dummy video lines. The shift register is driven by complimentary square wave clocks with periodic start pulses being introduced to initiate each scan. Cell-to-cell sampling rate is determined by the clock frequency. Integration time is the interval between start pulses. The output signal obtained from each scan of an N element array is a train of N charge pulses each proportional to the light intensity on the corresponding photodiode. In addition to the signal charge, switching transients are capacitively coupled into the active video line by the multiplex switches. These same transients are introduced into the dummy video line and, therefore, can be eliminated and a clean signal recovered by reading out the video and dummy lines differentially.

Clock and Voltage Requirements

Scanning is achieved by means of a digital shift register. The shift register is driven by complimentary square wave clocks, $ø_1$ and $ø_2$. The clock amplitude should be equal to V_{DD} - V_{SS}. With V_{DD} = 5V and V_{SS} = 0V, the clock inputs will be HCMOS compatible. Since each photodiode is read out on the positive transition of $ø_2$, the frequency of the clock signal should be set equal to the desired video data rate.

The start pulse of similar amplitude to the clocks is required to load the shift register and initiate each readout period. A timing diagram for the start and clock signals is shown in Figure 5. Note: $ø_1$ and $ø_2$ clocks need to be continuously applied to the device. The time between start pulses determines the integration period. Note: Six dummy diodes are provided for dark reference at the front of both the RL0512SIU and RL1024SIU.

End of Scan

An output pulse useful primarily for test purposes is provided after the last photodiode is sampled by the shift register scanning circuit. The timing of the EOS output is shown in Figure 5. The voltage levels on the EOS output will be determined by the V_{DD} and V_{SS} voltage levels supplied to the photodiode array. When V_{DD} is at +5V and V_{SS} is operated at 0V, the EOS output will be compatible with HCMOS family of logic devices.

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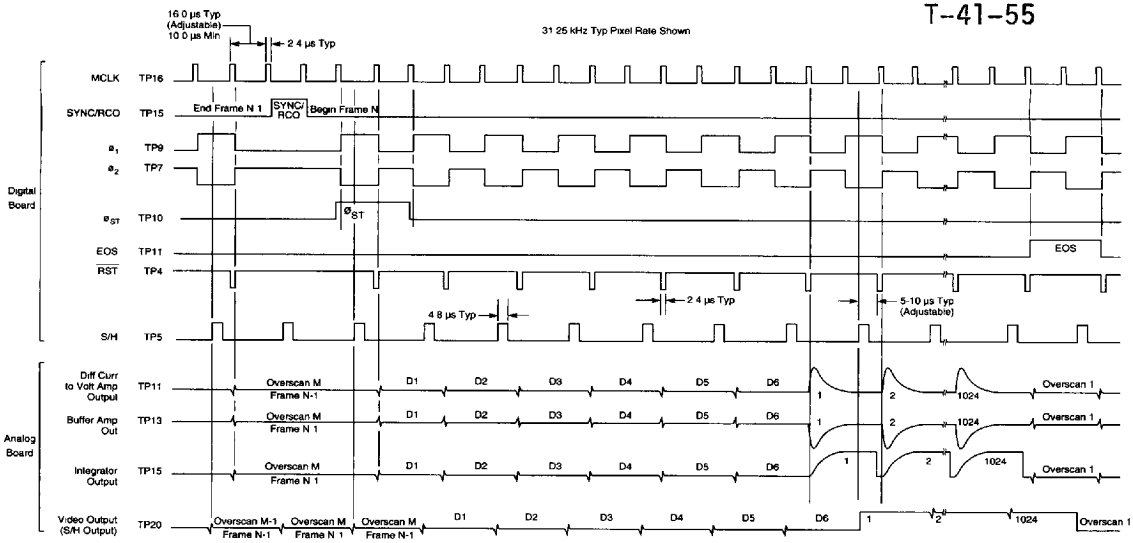

Figure 5. Timing Diagram

Amplifier Requirements

A recommended output circuit for use with SI devices is a simple current amplifier. A current amplifier holds the video line at a virtual ground and senses the current pulses flowing into the video line to recharge the diodes through their respective multiplex switches as they are sampled in sequence. These current pulses are converted to a train of voltage pulses corresponding to the light intensity on the various diodes. In this mode of operation, the current amplifier must provide a positive bias voltage to the video line since the PtSi photodiode is reverse biased in actual operation. Figure 6 shows a simple recharge amplifier suitable for use with SI series devices.

Dark Current

During normal operation, at liquid nitrogen (i.e., 77°K) temperatures, the array will saturate in ≈10 seconds due to dark current leakage. Under actual operating conditions, however, the maximum integration time is usually determined by the background photon flux hitting the detector and not the dark current leakage. For unfiltered 300°K blackbody radiation, the array saturates in ≈0.1 seconds with standard FOV apertures in Reticon's standard evaluation detector head.

Evaluation Detector Head

A complete, pour filled LN_2 cooled detector head useful for evaluating the performance and operating characteristics of the SI Series arrays is available from Reticon. The RH0512SIU or RH1024SIU consists of a 512 or 1024 element PtSi linear array, an LN_2 dewar with >8 hour hold time and complete drive and video processing circuitry. Contact EG&G Reticon for more information.

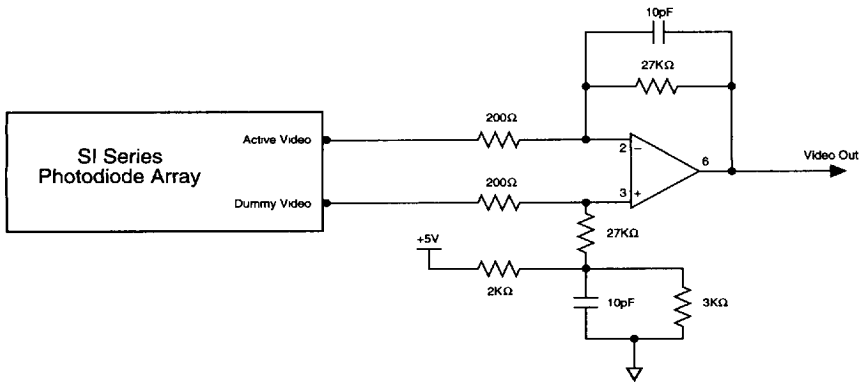

Figure 6. Simplified Recharge Mode Video Amplifier

Table 1. Pin Definition of the Wide Aperture, Linear PtSi IR SI Series Array

Pin Number	Pin Name	Pin Definition
1	NC	
2	NC	
3	NC	
4	NC	
5	TD1	Temperature diode #1
6	NC	
7	V_G	Guard ring voltage
8	NC	
9	V_{Sub}	Bottomside substrate contact
10	NC	
11	$ø_{RGO}$	Active video reset gate
12	TD2	Temperature diode #2
13	V_{RDO}	Active video reset drain
14	V_{Out}	Active video output
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	V_{DOut}	Dummy video output
22	V_{RDD}	Dummy video reset drain
23	V_{DD}	Scanning register (N-Well)
24	$ø_{RGD}$	Dummy video reset gate
25	$ø_{EOS}$	End of scan pulse output
26	V_{Sub}	Bottomside substrate contact
27	NC	
28	$ø_2$	Shift register clock; phase 2
29	V_{SS}	Topside substrate contact
30	$ø_1$	Shift register clock; phase 1
31	$ø_{ST}$	Start pulse input
32	NC	
33	NC	
34	NC	

Table 2. Electrical Characteristics (25°C)
(All voltages measured with respect to Pin 29, V_{SS})

Signal	Sym		Typ	Units
Scanning register (N-Well)	V_{DD}		5	V
Guard ring	V_G		5	V
Substrate	V_{SS}, V_{SUB}		0	V
Start pulse $ø_{st}$	V_{HS}	High	5	V
	V_{LS}	Low	0	V
Clock $ø_1$, $ø_2$	V_{H1}, V_{H2}	High	5	V
	V_{L1}, V_{L2}	Low	0	V
Reset gate $ø_{RGO}$, $ø_{RGD}$	V_{HRGO}, V_{HRGD}	High	5	V
	V_{LRGO}, V_{LRGD}	Low	0	V
Video bias	V_{Out}, V_{DOut}		2.5	V
Reset drain	V_{RDO}, V_{RDD}		2.5	V
Clock rate $ø_1$, $ø_2$ [1]	f_1, f_2		1	MHz (max)
Capacitance $ø_1$, $ø_2$ at 5V bias [1]	C_1, C_2			
RL0512SIU			31	pF
RL1024SIU			35	pF
Capacitance, each video line at 2.5V bias [1]	C_{Out}, C_{DOut}			
RL0512SIU			10	pF
RL1024SIU			18	pF

Note:
1 Calculated, not measured.

Table 3. Electro-Optical Characteristics (80°K)

Parameters	Typ	Units
Center-to-center spacing	25	µm
Pixel width (active area)	15	µm
Pixel length (active area)	2.5	mm
Fill factor	60	%
Number of pixels	1024 and 512	elements
Quantum efficiency @ 1.15 µm	8	%
Cutoff wavelength (λ_C)	5.0	µm
Maximum readout rate [1]	1	MHz
Saturation charge	7	pC
Saturation voltage [2]	7	V
Dark signal (80°K dark slide) [2]	0.15	V
Light on signal (300°K blackbody) [2]	3.5	V
Light off signal [2,3]	2.5	V
Thermodynamic noise (300°K blackbody) [2]	1.0	mV_{rms}
Dynamic range [2,4]	3500:1	rms
Pixel-to-pixel nonuniformity (300°K blackbody) [2]	<1%	rms

Notes:
1 Calculated, not measured
2 Measured using RH1024SIU Evaluation Dewar with no cold filters and a 41 ms integration time
3 Measured with the dewar window covered by a black anodized aluminum blank at ambient temperature
4 Dyn R = (V_{Sat} - Light on signal/thermodynamic noise)

Table 4. Absolute Maximum Ratings

	Min	Max	Units
Voltage applied to any terminal with respect to V_{SS}	0	+15	V

	A	B
RL0512SIU	0.567 ± .006	0.504 inch
RL1024SIU	1.071 ± .011	1.008 inch

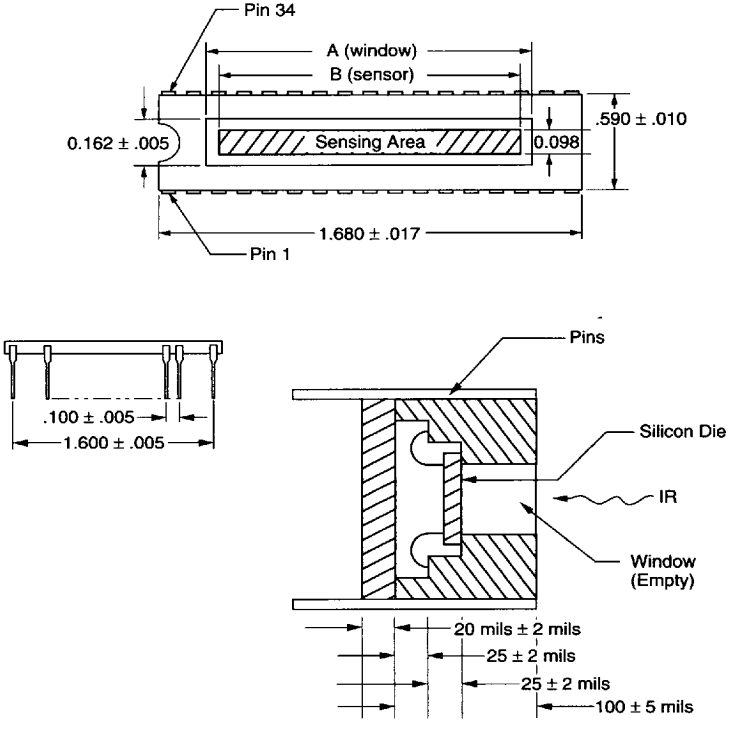

Figure 7. Package Dimensions (all dimensions are typical and in inches unless otherwise specified)

Ordering Information

Array Part Number	Evaluation Detector Head (includes detector)
RL0512SIU-011 RL1024SIU-011	RH0512SIU-011 RH1024SIU-011

055-0298
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