Data Sheet | November 2000 | File Number 4924

Low Power Ringing SLIC for Home Gateways

The RSLIC18 family of ringing subscriber line interface circuits (RSLIC) supports analog Plain Old Telephone Service (POTS) in short and medium loop length, wireless and wireline applications. Ideally suited for remote subscriber units, this family of products offers flexibility to designers with high ringing voltage and low power consumption system requirements. Other key features across the product family include: ringing using sinusoidal or trapezoidal waveforms and minimal external discrete application components.

The ISL5586 operates up to 100V which translates directly to the amount of ringing voltage supplied to the end subscriber. With the high operating voltage of 100V the RSLIC18 family can extend subscriber loop lengths to 500Ω (i.e., 5,000 feet) and beyond.

The receive and transmit ports of the ISL5586 are designed with differential interfaces to the CODEC. This implementation provides noise immunity and signal level compatibility with 3.3V CODECs. With a few external components, the transmit signal can be biased to within the common mode input range of the CODEC.

The ringing interface of the ISL5586 is DC coupled and has been implemented differentially. The interface allows both AC and DC control of the balanced ringing waveform.

Features

- Low Power Consumption
- Differential CODEC Interface
- Telecordia TR-57 Compliant
- Software Compatible with Existing RSLIC18 Designs
- Low Idle Channel Noise
- Programmable Transient Current Limit
- Integrated MTU DC Characteristics
- Low External Component Count
- Silent Polarity Reversal and On Hook Transmission
- Thermal Shutdown
- 28 Lead Surface Mount Packaging
- Dielectric Isolated (DI) High Voltage Design

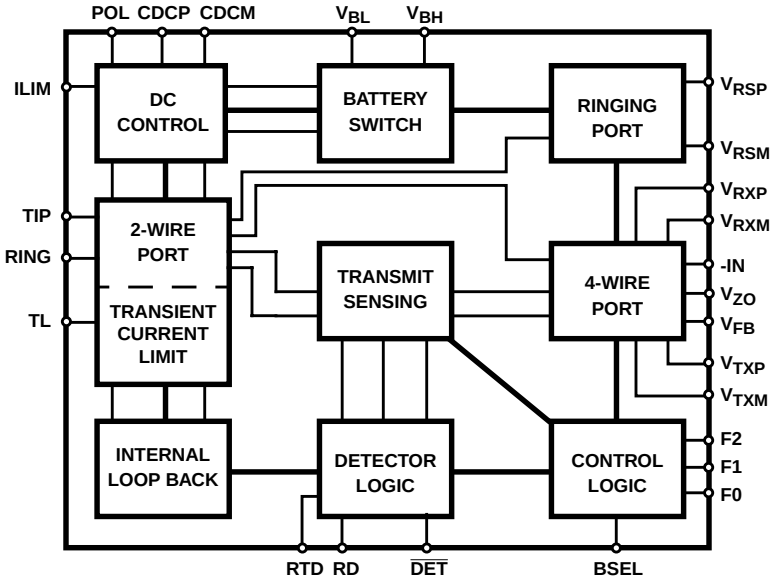
Applications

- Cable Modems
- Remote Subscriber Units
- Short Loop Access Platforms
- Voice Over Internet Protocol (VoIP)
- Voice Over DSL (VoDSL)
- Broadband Wireless Access

Related Literature

- User's Guide for Development Board
- Modeling of the AC Loop
- Interfacing to DSP CODECs (Contact Factory)
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Block Diagram



Ordering Information

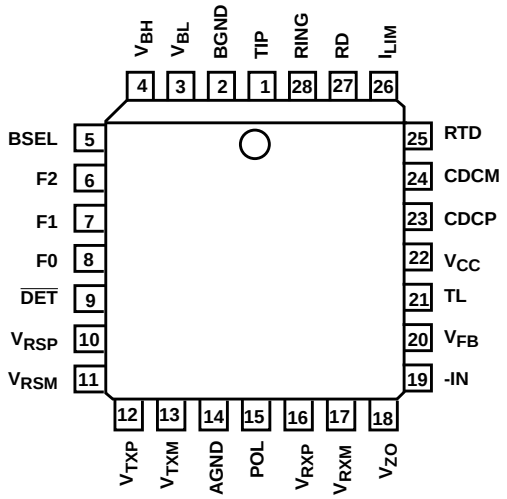
PART NUMBER	HIGH BATTERY (V_{BH})			LONGITUDINAL BALANCE		TEMP. RANGE ^{O}C	PACKAGE	PACKAGE NO.
	100V	85V	75V	58dB	53dB			
ISL5586FCM			•		•	0 to 75	28 Ld PLCC	N28.45
ISL5586BIM		•		•		-40 to 85	28 Ld PLCC	N28.45
ISL5586CIM	•				•	-40 to 85	28 Ld PLCC	N28.45
ISL5586DIM		•			•	-40 to 85	28 Ld PLCC	N28.45

Device Operating Modes

MODE	F2	F1	F0	DET	DESCRIPTION
Low Power Standby (LPS)	0	0	0	SHD	MTU compliant on hook operating mode.
Forward Active (FA)	0	0	1	SHD	MTU compliant and OHT capable on hook mode, off hook loop feed mode.
Unused	0	1	0	n/a	Reserved for internal purposes.
Reverse Active (RA)	0	1	1	SHD	Signalling mode which reverses direction of loop current, otherwise like Forward Active.
Ringing	1	0	0	RTD	Signalling mode used to generate high voltage balanced ringing signal.
Forward Loop Back (FLB)	1	0	1	SHD	Internal loop back mode which connects internal load across Tip and Ring terminals.
Tip Open/Ground Start (TO)	1	1	0	SHD	Signalling mode sets Tip to high impedance state, Ring output still active.
Power Denial (PD)	1	1	1	n/a	Loop disconnect mode which forces both Tip and Ring to high impedance.

Pinout

ISL5586 (PLCC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Maximum Supply Voltages
- V_{CC} . . . . . -0.5V to +7V
- V_{CC} - V_{BAT} 110V
- ESD (Human Body Model) 500V

Maximum Tip/Ring Negative Voltage Pulse (Note 7) . . . . . V_{BH}-15V
Maximum Tip/Ring Positive Voltage Pulse (Note 7) . . . . . + 8V

Operating Conditions

Temperature Range
- Industrial . . . . . -40^{o}C to 85^{o}C

Positive Power Supply (V_{CC}) . . . . . +5V
Negative Power Supply (V_{BH}, V_{BL}) . . . . . -100V to -24V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PLCC Package	53

Maximum Junction Temperature Plastic . . . . . .150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{o}C
(PLCC - Lead Tips Only)

Die Characteristics

Substrate Potential . . . . . -V_{BH}
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Unless Otherwise Specified, T_A = -40^{o}C to 85^{o}C, V_{BL} = -24V, V_{BH} = -100V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω, 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. These parameters apply generically to each product offering.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING PARAMETERS					
V_{RSP} Input Impedance (Note 2)		35	-	-	MΩ
V_{RSM} input impedance (Note 2)		10	-	-	MΩ
Differential Ringing Gain (Note 3)	V_{RS} to 2-Wire, R_{LOAD} = 5 REN	-	99.5	-	V/V
Ringing voltage Total Distortion	R_L = 1.3 kΩ, V_{T-R} = $\|V_{BH}\|$ -5	-	0.8	5	%
4-Wire to 2-Wire Ringing Off Isolation	Forward Active Mode, Referenced to V_{RS} Input.	-	100	-	dB
2-Wire to 4-Wire Transmit Isolation	Ringing Mode Referenced to the Differential Ringing Amplitude.	-	100	-	dB
Centering Voltage Accuracy	Tip, Referenced to V_{BH}/2 + 0.5V	-3.0	0.2	3.0	V
	Ring, Referenced to $V_{BH/2}$ + 0.5V	-3.0	0.2	3.0	V
AC TRANSMISSION PARAMETERS					
Receive Input Impedance, V_{RXP} (Note 2)		379	541	-	kΩ
Receive input Impedance, V_{RXM} (Note 2)		100	142	-	kΩ
Transmit Output Impedance (Note 2)	DC	-	0.01	-	Ω
Transmit Output Drive Capability (Note 2)	Current	0.30	1.0	-	mA
	Capacitance to Ground	-	1.0	100	pF
4-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PEAK}
2-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PEAK}
2-Wire Return Loss (Note 2)	200Hz ≤ f ≤ 1kHz	-	35	-	dB
	1kHz ≤ f ≤ 3.4kHz	-	23	-	dB
Longitudinal Current Capability per Wire (Note 2)	False Detect	20	-	-	mA_{RMS}
	False Detect in Low Power Standby	10	-	-	mA_{RMS}
2-Wire Longitudinal Balance (ON-Hook and OFF-Hook) (Notes 4, 5)	200Hz, 500Hz, 1000Hz	58	61	-	dB
	3000Hz	53	61	-	dB
4-Wire Longitudinal Balance (ON-Hook and OFF-Hook) (Notes 4, 5)	200Hz, 500Hz, 1000Hz	58	64	-	dB
	3000Hz	53	62	-	dB
4-Wire to 2-Wire Insertion Loss	0dBmo at 1kHz	2.72	2.92	3.12	dB
2-Wire to 4-Wire Insertion Loss	0dBmo at 1kHz	-0.2	0	0.2	dB
4-Wire to 4-Wire Insertion Loss	0dBmo at 1kHz	2.72	2.92	3.12	dB
Frequency Response, On Hook, 2-Wire to 4-Wire, 4-Wire to 2-Wire, 4-Wire to 4-Wire	Referenced to 0dBmo at 1004Hz, 400Hz ≤ f ≤ 2800Hz	-0.15	0.03	0.15	dB
Frequency Response, Off Hook 2-Wire to 4-Wire, 4-Wire to 2-Wire, 4-Wire to 4-Wire	Referenced to 0dBmo at 1004Hz, f = 400Hz, 2800Hz	-0.15	0.03	.15	dB

Electrical Specifications

Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -100V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω, 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. These parameters apply generically to each product offering. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Amplitude Tracking, Off Hook, 2-Wire to 4-Wire, 4-Wire to 2-Wire, 4-Wire to 4-Wire	+3dBmo to -37dBmo, f = 1004Hz, Referenced to 0dBmo	-	0.02	-	dB
	-37 to -50dBmo	-	0.05	-	dB
	-50 to -55dBmo	-	0.10	-	dB
Amplitude Tracking, ON-Hook	0dBmo to -37dBmo, f = 1004Hz, Referenced to 0dBmo	-	0.01	-	dB
Signal to Distortion, 2-Wire to 4-Wire, 4-Wire to 2-Wire, 4-Wire to 4-Wire, ON-Hook and OFF-Hook	Input level 0dBmo to -30dBmo	33	45	-	dB
	Input Level -30 to -40dBmo	27	40	-	dB
	Input Level -40 to -45dBmo	22	29	-	dB
Signal Frequency Distortion (0Hz to 12kHz)	0dBmo input, 0 Hz ≤ f ≤ 12kHz	28	45	-	dB
Single Frequency Distortion (0Hz to 4kHz)	0dBmo Input, 1004Hz ≤ f ≤ 1024Hz	40	50	-	dB
Intermodulation Distortion, 2-Wire to 4-Wire, 4-Wire to 2-Wire, 4-Wire to 4-Wire (IEEE Standard 743-1984)	4-Tone Second-Order Intermodulation Products	43	50	-	dB
	4-Tone Third-order Intermodulation Products	44	62	-	dB
Idle Channel Noise, 2-Wire (Note 5)	C-Message, Forward Active, Low Battery Enabled	-	10.0	13.0	dBrnc
Idle Channel Noise, 4-Wire (Note 5)	C-Message, Forward Active, Low Battery Enabled	-	10.0	13.0	dBrnc
DC PARAMETERS					
OFF-Hook Loop Current Limit	Programming Accuracy (1% External Resistor)	-8.5	1.0	+8.5	%
	Programming Range	15	-	45	mA
OFF-Hook Transient Current Limit	Programming Accuracy	-10	-	+10	%
	Programming Range	40	-	100	mA
Loop Current During Low Power Standby	Forward Polarity Only (R_L = 600Ω)	-	24	-	mA
Open Circuit Voltage (|Tip - Ring|) Forward and Reverse Active modes	V_{BL} = -16V	-	7.0	-	V_{DC}
	V_{BL} = -24V	13.5	14.5	16.5	V_{DC}
	V_{BH} > -60V	43	48	-	V_{DC}
Open Circuit Voltage (|Tip-Ring|) LPS	V_{BH} > -60V	43	51	-	V_{DC}
Absolute Open Circuit Voltage (Relative to GND)	V_{RG} in FA, V_{TG} in RA, V_{BH} > -60V	-	-53	-56	V_{DC}
Absolute Open Circuit Voltage	V_{RG} in LPS	-	-52	-56	V_{DC}
TEST ACCESS FUNCTIONS					
Loopback Max Battery		-	-	52	V
LOOP DETECTORS AND SUPERVISORY FUNCTIONS					
Switch Hook Programming Range		5	-	15	mA
Switch Hook Programming Accuracy	Assumes 1% External Programming Resistor	-10	-	+10	%
Dial Pulse Distortion		-	1.0	-	%
Ring Trip Comparator Threshold		2.3	2.60	2.9	V
Ring Trip Programming Current Accuracy		-10	-	+10	%
Thermal Shutdown Threshold	IC Junction Temperature	-	175	-	°C
LOGIC INPUTS (F0, F1, F2, BSEL)					
Input Low Voltage		-	-	0.8	V
Input High Voltage		2.0	-	-	V
Input Low Current (F0, F1, F2)	V_{IL} = 0.4V	-	7.5	20	µA
Input Low Current (BSEL)	V_{IL} = 0.4V	-	1.0	-	µA
Input High Current (F0, F1, F2, BSEL)	V_{IH} = 2.4V	-	0.01	-	µA
LOGIC OUTPUT ($\overline{\text{DET}}$)					
Output Low Voltage	I_{OL} = 5mA	-	0.15	0.4	V
Output High Voltage	I_{OH} = 100µA	2.4	3.2	3.5	V
SUPPLY CURRENTS					
Low Power Standby, BSEL = 2.0V, V_{BH} = -75V to -100V	I_{CC}	-	3.2	5.0	mA
	I_{BH}	-	0.65	0.9	mA
Forward or Reverse, BSEL =.8V	I_{CC}	-	5.0	6.5	mA
	I_{BL}	-	1.5	2.5	mA

Electrical Specifications Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -100V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω, 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. These parameters apply generically to each product offering. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Active, BSEL = 2.0V, V_{BH} = -100V	I_{CC}	-	7.0	9.0	mA
	I_{BL}	-	1.4	2.0	mA
	I_{BH}	-	1.8	3.0	mA
Forward Active, BSEL = 2.0V, V_{BH} = -85V	I_{CC}	-	6.6	8.5	mA
	I_{BL}	-	1.35	2.0	mA
	I_{BH}	-	1.60	2.75	mA
Forward Active, BSEL = 2.0V, V_{BH} = -75V	I_{CC}	-	6.3	8.0	mA
	I_{BL}	-	1.25	2.0	mA
	I_{BH}	-	1.45	2.5	mA
Ringing, BSEL = 2.0V, V_{BH} = -100V	I_{CC}	-	7.4	10.0	mA
	I_{BL}	-	1.5	2.0	mA
	I_{BH}	-	2.2	3.0	mA
Ringing, BSEL = 2.0V, V_{BH} = -85V	I_{CC}	-	6.80	9.25	mA
	I_{BL}	-	1.36	2.0	mA
	I_{BH}	-	2.1	3.0	mA
Ringing, BSEL = 2.0V, V_{BH} = -75V	I_{CC}	-	6.4	8.5	mA
	I_{BL}	-	1.26	2.0	mA
	I_{BH}	-	2.0	3.0	mA
Forward Loopback, BSEL = 0.8V, V_{BL} = -24V	I_{CC}	-	10.3	13.5	mA
	I_{BL}	-	23.0	32.0	mA
Tip Open, BSEL = 2.0V	I_{CC}	-	3.2	-	mA
	I_{BL}	-	0.1	-	mA
Power Denial, BSEL = 0.8V or 2.0V	I_{CC}	-	3.4	6.0	mA
	I_{BL}	-	0.22	0.50	mA
ON HOOK POWER DISSIPATION (Note 6)					
Forward or Reverse	V_{BL} = -24V	-	57	-	mW
Low Power Standby	V_{BH} = -100V	-	83	-	mW
	V_{BH} = -85V	-	70	-	mW
	V_{BH} = -75V	-	64	-	mW
Ringing	V_{BH} = -100V	-	294	-	mW
	V_{BH} = -85V	-	236	-	mW
	V_{BH} = -75V	-	206	-	mW
OFF HOOK POWER DISSIPATION (Note 6)					
Forward or Reverse	V_{BL} = -24V, I_{LIM} = 25mA, R_L = 300Ω	-	305	-	mW
POWER SUPPLY REJECTION RATIO					
V_{CC} to 2-Wire, BSEL = 0.8V	f = 50kHz	-	50	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	45	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	28	-	dB
V_{CC} to 4-Wire, BSEL = 0.8V	f = 50Hz	-	70	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	55	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	40	-	dB
V_{BL} to 2-Wire, BSEL = 0.8V	f = 50Hz	-	25	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	38	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	28	-	dB
V_{BL} to 4-Wire, BSEL = 0.8V	f = 50Hz	-	27	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	36	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	23	-	dB
V_{BH} to 2-Wire, BSEL = 2.0V	f = 50Hz	-	27	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	35	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	23	-	dB

Electrical Specifications Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -100V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω, 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. These parameters apply generically to each product offering. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{BH} to 4-Wire, BSEL = 2.0V	f = 50Hz	-	76	-	dB
	f = 300Hz ≤ f ≤ 3400Hz	-	55	-	dB
	f = 8kHz ≤ f ≤ 16kHz	-	42	-	dB

NOTES:

2. These parameters are controlled via design and Statistical Process Control and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
3. Input voltage = 0.636V_{RMS} for V_{BH} = -100V, 0.530V_{RMS} for V_{BH} = -85V and 0.460V_{RMS} for -75V devices.
4. Tested per IEEE455-1985, with 368Ω resistors connected to the Tip and Ring terminals.
5. These parameters are tested 100% at room temperature, and are guaranteed but not tested across the full temperature range via statistical characterization and design.
6. The power dissipation is based on actual device measurements and will be less than worst case calculations based on data sheet supply current limits.
7. Characterized with 2 x 10us and 10 x 1000us first level lightning surge waveform (GR-1089-CORE).

Design Equations

Refer to Figure 14 for programming resistor connections.

Loop Supervision Thresholds

SWITCH HOOK DETECT

The desired switch hook detect threshold current (I_{SH}) is set by a single external resistor, R_{SH} as follows

$$R_{SH} = 615/I_{SH} \quad \text{(EQ. 1)}$$

The loop current threshold programming range is from 5mA to 15mA.

RING TRIP DETECT

The ring trip detect threshold (I_{RT}) is set by a single external resistor, R_{RT} as follows.

$$R_{RT} = 1800/I_{RT} \quad \text{(EQ. 2)}$$

I_{RT} should be set between the peak ringing current and the peak off hook current while still ringing. In addition, the ring trip current must be set below the transient current limit including tolerances. The ringing signal filter capacitor C_{RT}, in parallel with R_{RT} sets the ring trip response time.

LOOP CURRENT LIMIT

The DC loop current limit (I_{LIM}) is programmed by the external resistor R_{IL} as follows.

$$R_{IL} = \frac{1760}{I_{LIM}} \quad \text{(EQ. 3)}$$

The loop current limit programming range is from 15mA to 45mA.

Impedance Matching

The AC source impedance of the SLIC is programmed with the external impedance network Z_S as described next. To synthesize and match Resistive line terminations the programming network is simply a resistor (R_S) as shown in Figure 14. For complex line terminations such as the one illustrated in Figure 1, a complex programming network is required.

RESISTIVE IMPEDANCE SYNTHESIS

The AC source resistance of the SLIC is synthesized with a single external resistor R_S as follows:

$$R_S = Z_0 \times \left(\frac{400}{3}\right) = 133.3(Z_0) \quad \text{(EQ. 4)}$$

The synthesized resistance (Z_0) is determined by the characteristic line resistance and protection resistors as shown in Equation 5.

$$Z_O = R_L - (RP_1 + RP_2) \quad \text{(EQ. 5)}$$

COMPLEX IMPEDANCE SYNTHESIS

A complex network is used in place of R_S when the termination impedance of the line is complex as shown in Figure 1.

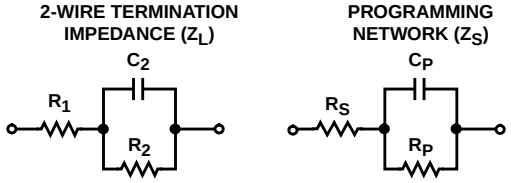


FIGURE 1. COMPLEX PROGRAMMING NETWORK

The component R_S has a different design equation than the R_S used for resistive impedance synthesis. The design equations for each component are provided below where RP1 and RP2 are the protection resistors and R_P is a component of the programming network.

$$R_S = 133.3 \times (R1 - RP_1 - RP_2) \quad \text{(EQ. 6)}$$

$$R_P = 133.3 \times R_2 \quad \text{(EQ. 7)}$$

$$C_P = C_2/133.3 \quad \text{(EQ. 8)}$$

$$Z_O = (R1 - RP1 - RP2) + R2||C2 \quad \text{(EQ. 9)}$$

4-WIRE TO 2-WIRE GAIN

The 4-wire to 2-wire gain (G_{42}) is defined as the receive gain. It is a function of the terminating impedance, synthesized impedance and protection resistors. The gain is defined from the Receive input terminals (V_{RXP}, V_{RXM}) to the terminating impedance (Z_L) on the 2-wire side, and is illustrated in Figure 12.

$$G_{42} = -2.8\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 10)}$$

When the device source impedance and the protection resistors equal the terminating impedance, the receive gain equals 2.92dB and is inverted with respect to the input.

2-WIRE TO 4-WIRE GAIN

The 2-wire to 4-wire gain (G_{24}) is the gain from tip and ring to the transmit differential output. The transmit gain is given by Equation 11. Note that V_{TR} is defined on the line side of the protection resistors (reference Figure 13). With Z_L set to 600 ohms, the protection resistors set to 50Ω/terminal and $Z_0 = Z_L$-2RP the Transmit gain equals -0.833 (-1.59dB) and is inverted with respect to the 2-wire input (V_{TR}).

$$G_{24} = -2\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 11)}$$

TRANSHYBRID GAIN

The transhybrid gain is defined as the 4-wire to 4-wire gain (G_{44}) and is given by Equation 12 (Reference Figure 14)).

$$G_{44} = -2.8\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 12)}$$

Transient Current Limit

The drive current capability of the output amplifiers is determined by an externally programmable output current limit circuit which is separate from the DC loop current limit function. The transient current limit is programmed with a resistor to ground at the TL pin. The current limit circuit works in both the source and sink direction, with an internally fixed offset to prevent the current limit functions from turning on simultaneously. The current limit function is provided by sensing line current and reducing the voltage drive to the load when the externally set threshold is exceeded, hence forcing a constant source or sink current.

SOURCE CURRENT PROGRAMMING

The source current is externally programmed as shown in Equation 13.

$$R_{TL} = \frac{1780}{I_{SRC}} \quad \text{(EQ. 13)}$$

For example, a source current limit setting of 50mA is programmed with a 35.6kΩ resistor connected from pin 16 of the device to ground. This setting determines the maximum amount of current which flows from Tip to Ring during an off hook event until the DC loop current limit responds. In addition this setting also determines the amount of current which will flow from Tip or Ring when external battery faults occur.

SINK CURRENT PROGRAMMING

The sink current limit is internally offset 20% higher than the externally programmed source current limit setting.

$$I_{SNK} = 1.20 \times I_{SRC} \quad \text{(EQ. 14)}$$

If the source current limit is set to 50mA, the sink current limit will be 60mA. This setting will determine the amount of current which flows into Tip or Ring when external ground faults occur.

FUNCTIONAL DESCRIPTION

Each amplifier is designed to limit source current and sink current. The diagram below shows the functionality of the circuit for the case of limiting the source current. A similar diagram applies to the sink current limit with current polarity changed accordingly.

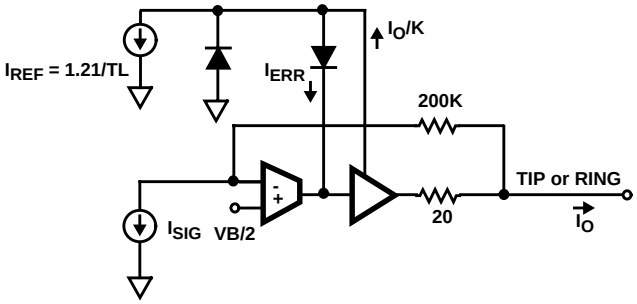


FIGURE 2. CURRENT LIMIT FUNCTIONAL DIAGRAM

During normal operation, the error current (I_{ERR}) is zero and the output voltage is determined by the signal current (I_{SIG}) multiplied by the 200K feedback resistor. With the current polarity as shown for I_{SIG}, the output voltage moves positive with respect to half battery. Assuming the amplifier output is driving a load at a more negative potential, the amplifier output will source current.

During excessive output source current flow, the scaled output current (I_O/K) exceeds the reference current (I_{REF}) forcing an error current (I_{ERR}). With the polarity as shown the error current subtracts from the signal current, which reduces the amplifier output voltage. By reducing the output voltage the source current to the load is decreased and the output current is limited.

DETERMINING THE PROPER SETTING

Since this feature programs the maximum output current of the device, the setting must be high enough to allow for detection of ring trip or programmed off hook loop current, whichever is greater.

To allow for proper ring trip operation, the transient current limit setting should be set at least 25% higher than the peak ring trip current setting. Setting the transient current 25% higher should account for programming tolerances of both the ring trip threshold and the transient current limit.

If loop current is larger than ring trip current (low REN applications) then the transient current limit should be set at least 35% higher than the loop current setting. The slightly higher offset accounts for the slope of the loop current limit function.

Attention to detail should be exercised when programming the transient current limit setting. If ring trip detect does not occur while ringing, then re-examine the transient current limit and ring trip threshold settings.

Low Power Standby Mode

Overview

The low power standby mode (LPS, 000) should be used in conjunction with the high battery during idle line conditions. The SLIC is designed to operate from the high battery during this mode so MTU compliance can be met. Most of the internal circuitry is powered down, resulting in low power dissipation. If MTU compliance is not required during idle line conditions, the device may be operated from the low battery which will decrease the standby power dissipation.

TABLE 1. DEVICE INTERFACES DURING LPS

INTERFACE	ON	OFF	NOTES
Receive	-	x	AC transmission, impedance matching and ringing are disabled during this mode.
Ringing	-	x	
Transmit	-	x	
2-Wire	x	-	Amplifiers disabled.
Loop Detect	x	-	Switch hook.

2-Wire Interface

In the LPS mode, the 2-wire interface is maintained with internal switches, resistors, and voltage references. The Tip and Ring amplifiers are turned off to conserve power. The device will provide MTU compliance, loop current, and loop supervision. Figure 2 represents the internal circuitry providing the 2-wire interface when in this mode of operation.

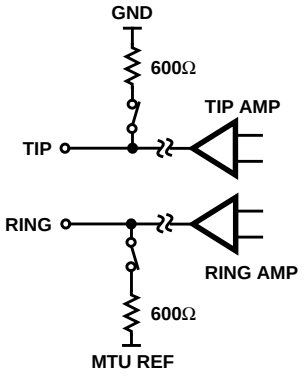


FIGURE 3. LPS 2-WIRE INTERFACE CIRCUIT DIAGRAM

MTU Compliance

Maintenance Termination Unit or MTU compliance places DC voltage requirements on the 2-wire terminals during idle line conditions. The minimum idle voltage for compliance is 42.75V. The high side of the MTU range is 56V. The voltage is expressed as the difference between Tip and Ring.

The Tip voltage is held near ground through a 600Ω resistor and switch. The Ring voltage is nominally limited to -49V by the MTU reference. A switch and 600Ω resistor connect the MTU reference to the Ring terminal. When the high battery voltage exceeds the MTU reference of -49V, the Ring terminal will be clamped by the internal reference. The same Ring relationships apply when operating from the low battery. For operating battery voltages (V_{BH}) less than or equal to the internal MTU reference, the Ring voltage will be approximately 4.5 volts more positive than V_{BH}.

Loop Current

In the LPS mode, the device is capable of providing DC current to a load through a path of resistors and switches. The current available for switch hook detect is a function of the off hook loop resistance (R_{LOOP}). This includes the off hook phone resistance and copper loop resistance. The current available during LPS is given by Equation 15.

$$I_{LOOP} = (-1-(-49))/(600+600+R_{LOOP}) \quad \text{(EQ. 15)}$$

Internal current limiting of the standby switches will limit the maximum current to approximately 23mA. The longitudinal current capability is guaranteed to be greater than or equal to $10mA_{RMS}$ per pin. When longitudinal currents exceed this level, false off hook detection may occur. The reduction in longitudinal current capability with respect to the Forward Active mode is a result of turning off the Tip and Ring amplifiers.

On Hook Power Dissipation

The on hook power dissipation of the SLIC in the LPS mode is determined by the operating voltages and quiescent currents and is calculated below.

$$P_{LPS} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 16)}$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an on hook mode. Some applications may specify a standby current. The standby current may be a charging current required for modern telephone electronics.

Standby Current Power Dissipation

Any standby line current, I_{SLC}, introduces an additional power dissipation term P_{SLC}. Equation 17 illustrates the power contribution is zero when the standby line current is zero.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| - 49 + 1 + I_{SLC} x 1200) \quad \text{(EQ. 17)}$$

If the battery voltage is less than -49V (the MTU clamp is off), the standby line current power contribution reduces to Equation 18.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| + 1 + I_{SLC} x 1200) \quad \text{(EQ. 18)}$$

Most applications do not specify charging current requirements during standby. When specified, the typical charging current may be as high as 5mA.

Forward Active Mode

Overview

The Forward Active mode (FA, 001) is the primary AC transmission mode of the SLIC. On hook transmission, DC loop feed and voice transmission are supported during this mode. The device may be operated from either high or low battery for on-hook transmission and from low battery for loop feed.

Loop supervision is provided by the switch hook detector at the $\overline{DET}$ output. When $\overline{DET}$ goes low, the low battery should be selected for DC loop feed and voice transmission.

On-Hook Transmission

The primary purpose of on hook transmission will be to support caller ID and other advanced signalling features. The transmission over load level while on hook is $3.1V_{PEAK}$.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 19.

$$V_{RING} = V_{BH} + 4.5V \quad \text{(EQ. 19)}$$

Feed Architecture

The SLIC design implements a voltage feed current sense architecture. The voltage across Tip and Ring is controlled by sensing the load current. Resistors are placed in series with the Tip and Ring outputs to provide the current sensing function. The diagram below illustrates the concept.

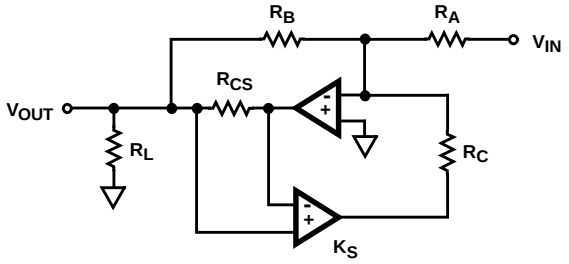


FIGURE 4. VOLTAGE FEED CURRENT SENSE DIAGRAM

By monitoring the current at the amplifier outputs, a negative feedback mechanism sets the output voltage for a defined load. The amplifier closed loop gains are set by internal resistor ratios (R_A, R_B, R_C) providing all the performance benefits of matched resistors. The internal sense resistor R_{CS}, is much smaller than the gain resistors and are typically 20Ω. The feedback mechanism, K_S, represents the gain configuration providing negative feedback to the loop.

DC Loop Feed

The feedback mechanism for monitoring the DC portion of the loop current is contained within the loop detector block. A low pass filter is used in the feedback loop to block voice and other signals from interfering with the loop current limit function. The pole of the low pass filter is set by the external 4.7µF capacitor (C_{DC}) and an internal 8KΩ resistor. The DC feed characteristic of the SLIC will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{VBL} + 4.5V. Most applications will operate the device from low battery while off hook. The following diagram depicts the DC feed characteristic.

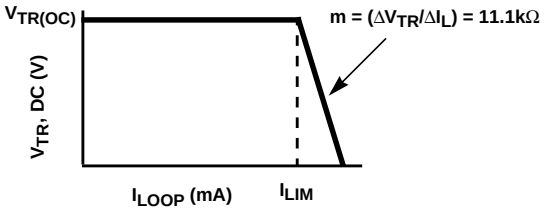


FIGURE 5. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 9 \quad \text{(EQ. 20)}$$

The curve of Figure 5 shows the loop current for a given set of loop conditions. The loop conditions are determined by the low battery voltage and the DC loop resistance. The DC loop resistance is the sum of the protection resistance, copper resistance (ohms/foot) and the telephone off hook DC resistance.

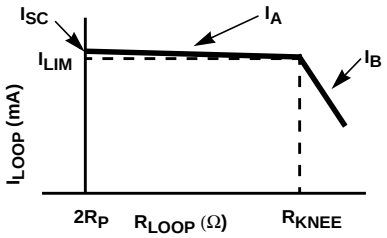


FIGURE 6. I_{LOOP} VERSUS R_{LOOP} LOAD CHARACTERISTIC

The slope of the feed characteristic and the battery voltage define the maximum loop current on the shortest possible loop as the short circuit current I_{SC}.

$$I_{SC} = I_{LIM} + \frac{V_{TR(OC)} - 2R_P I_{LIM}}{1.1e4} \quad \text{(EQ. 21)}$$

The term I_{LIM} is the programmed current limit, $1760/R_{IL}$. The line segment I_A represents the constant current region of the loop current limit function.

$$I_A = I_{LIM} + \frac{V_{TR(OC)} - R_{LOOP} I_{LIM}}{1.1e4} \quad \text{(EQ. 22)}$$

The maximum loop resistance for a programmed loop current is defined as R_{KNEE}.

$$R_{KNEE} = \frac{V_{TR(OC)}}{I_{LIM}} \quad \text{(EQ. 23)}$$

When R_{KNEE} is exceeded, the device will transition from constant current feed to constant voltage, resistive feed. The line segment I_B represents the resistive feed portion of the load characteristic.

$$I_B = \frac{V_{TR(OC)}}{R_{LOOP}} \quad \text{(EQ. 24)}$$

Power Dissipation

The power dissipated by the SLIC in the Forward Active mode while on hook is strictly a function of the quiescent currents for each supply.

$$P_{FAQ} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 25)}$$

Off hook power dissipation is increased above the quiescent power dissipation by the DC load. If the loop length is less than or equal to R_{KNEE}, the device is providing constant current ($I_{A)}$, and the power dissipation is calculated using Equation 26.

$$P_{FA(IA)} = P_{FA(Q)} + (V_{BL} x I_A) - (R_{LOOP} x I^2_A) \quad \text{(EQ. 26)}$$

If the loop length is greater than R_{KNEE}, the device is operating in the constant voltage, resistive feed region. The power dissipated in this region is calculated using Equation 27.

$$P_{FA(IB)} = P_{FA(Q)} + (V_{BL} x I_B) - (R_{LOOP} x I^2_B) \quad \text{(EQ. 27)}$$

Since the current relationships are different for constant current versus constant voltage, the region of device operation is critical to valid power dissipation calculations.

Reverse Active Mode

Overview

The reverse active mode (RA, 011) provides the same functionality as the forward active mode. On hook transmission, DC loop feed, and voice transmission are supported. Loop supervision is provided by the switch hook detector. The device may be operated from either high or low battery.

When in the Reverse Active mode the Tip and Ring DC voltage characteristics exchange roles. That is, Ring is typically 4V below ground and Tip is typically 4.5V more positive than battery.

Silent Polarity Reversal

Changing from forward active to reverse active or vice versa is referred to as polarity reversal. Many applications require control of the polarity reversal transition time. Requirements range from minimizing cross talk to protocol signalling.

The SLIC uses an external low voltage capacitor, C_{POL}, to set the reversal time. The capacitor is isolated from the AC loop so that loop stability is not influenced by its selection. Once C_{POL} is set, the reversal time will remain nearly constant over various load conditions.

The internal circuitry used to set the polarity reversal time is shown in Figure 7. During Forward Active the switch is open and the current from source I1 charges the external timing capacitor C_{POL}. The internal resistor provides a clamping function for the voltage at the POL node. When the Reverse Active mode is initiated the switch closes and the difference current (I2-I1) discharges the timing capacitor. The voltage at the POL node drives one side of a transistor differential pair which forces the Forward or Reverse condition on the Tip and Ring amplifiers. The forward/reverse transition time is given by Equation 28, where Δtime is the required reversal time.

$$C_{POL} = \frac{\Delta time}{75000} \quad \text{(EQ. 28)}$$

Polarized capacitors may be used for C_{POL}. The low voltage at the POL pin and minimal voltage excursion in the order of $\pm$0.75V, are well suited for polarized capacitors.

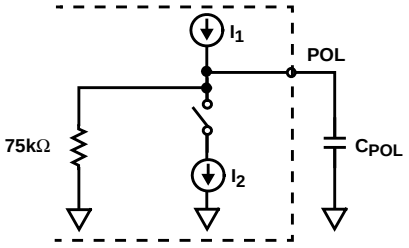


FIGURE 7. REVERSAL TIMING CONTROL

Power Dissipation

The power dissipation equations for forward active operation also apply to the reverse active mode.

Ringing

Overview

The Ringing mode (RNG, 100) provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The SLIC provides linear amplification to the differential signal applied to the ringing inputs (V_{RSP}, V_{RSM}). The differential ringing gain of the device is 100V/V. The circuit model for the ringing path is shown in Figure 8.

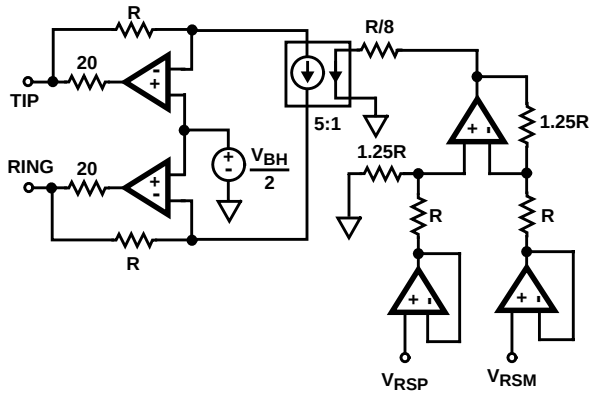


FIGURE 8. LINEAR RINGING MODEL

The voltage gain from the differential ringing input to the Tip output is 50V/V. The resistor ratios provide a gain of 10 and the current mirror provides a gain of 5. The voltage gain from the differential input to the Ring output is -50V/V. The equations for the Tip and Ring outputs during ringing are provided below.

$$V_T = \frac{V_{BH}}{2} + (50 \times V_{DIF}) \quad \text{(EQ. 29)}$$

$$V_R = \frac{V_{BH}}{2} - (50 \times V_{DIF}) \quad \text{(EQ. 30)}$$

When the differential input signal is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs is available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input Terminals

The differential terminals feature high input impedance which allows the use of low value capacitors for AC coupling the ring signal if necessary. The Ringing input is enabled only during the ringing mode, therefore a free running oscillator may be connected at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum differential signal swing between V_{RSP} and V_{RSM} to achieve full scale ringing is approximately $1.9V_{P-P}$.

Logic Control

Ringing patterns consist of silent and ringing intervals. The ringing to silent pattern is called the ringing cadence. During the silent portion of ringing, the device can be programmed to any other operating mode. The most likely candidates are low power standby or forward active. Depending on system requirements, the low or high battery may be selected.

Loop supervision is provided with the ring trip detector. The ring trip detector senses the change in loop current when the phone is taken off hook. The loop detector full-wave rectifies the ringing current, which is then filtered with external components R_{RT} and C_{RT}. The resistor R_{RT} sets the trip threshold and the capacitor C_{RT} sets the trip response time. Most applications will require a trip response time less than 150ms.

Three very distinct actions occur when the device detects a ring trip. First, the $\overline{DET}$ output is latched low. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the Ringing inputs are disabled, removing the ring signal from the line. Third, the device is internally forced to the forward active mode.

Power Dissipation

The power dissipation during ringing is dictated mostly by the load driving requirements and the ringing waveform. The key to valid power calculations is the correct definition of average and RMS currents. The average current defines the high battery supply current. The RMS current defines the load current.

The cadence provides a time averaging reduction in the peak power. The total power dissipation consists of ringing power, P_r, and the silent interval power, P_S.

$$P_{RNG} = P_r \times \frac{t_r}{t_r + t_s} + P_s \times \frac{t_s}{t_r + t_s} \quad \text{(EQ. 31)}$$

The terms t_R and t_S represent the cadence. The ringing interval is t_R and the silent interval is t_S. A typical cadence ratio t_R:t_S is 1:2.

The quiescent power of the device in the Ringing mode is defined in Equation 32.

$$P_{r(Q)} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 32)}$$

The total power during the ringing interval is the sum of the quiescent power and loading power:

$$P_r = P_{r(Q)} + V_{BH} \times I_{AVG} - \frac{V_{RMS}^2}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 33)}$$

For sinusoidal waveforms, the average current, I_{AVG}, is defined in Equation 34.

$$I_{AVG} = \left(\frac{2}{\pi}\right)\frac{V_{RMS} \times \sqrt{2}}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 34)}$$

The silent interval power dissipation will be determined by the quiescent power of the selected operating mode.

Forward Loop Back Mode

Overview

The Forward Loop Back mode (FLB, 101) provides test capability for the SLIC. An internal signal path is enabled allowing for both DC and AC verification by the connection of an internal 600 ohm resistor across Tip and Ring. This internal terminating resistor has a tolerance of ±10% at room temperature. The device is intended to operate from only the low battery during this mode.

Architecture

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers as shown below.

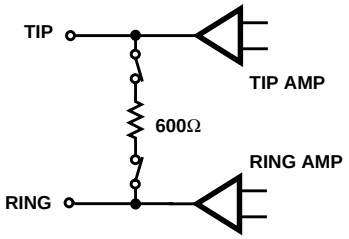


FIGURE 9. FORWARD LOOP BACK INTERNAL TERMINATION

DC Verification

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{DET}$ low, indicating the presence of loop current. In addition to verifying device functionality, toggling the logic output verifies the interface to the system controller.

AC Verification

The entire AC loop of the device is active during the forward loop back mode. Therefore a 4-wire to 4-wire level test capability is provided. Depending on the transhybrid balance implementation, test coverage is provided by a one or two step process.

System architectures which cannot disable the transhybrid function would require a two step process. The first step would be to send a test tone to the device while on hook and not in forward loop back mode. The return signal amplitude would be the test signal amplitude times the gain of the transhybrid amplifier. Since the device would not be terminated in the on hook mode, cancellation would not occur. The second step would be to program the device to FLB mode and resend the test tone. The return signal would be much lower in amplitude than the first step, indicating the device was active and the internal termination attenuated the return signal.

System architectures which can disable the transhybrid function would achieve test coverage with a signal step. Once the transhybrid function is disabled the SLIC can be programmed to the FLB mode and the test tone can be sent. The return signal level is determined by the 4-wire to 4-wire gain of the SLIC times the amplitude of the signal sent.

Tip Open/Ground Start Mode

Overview

The Tip Open mode (TO, 110) is intended for compatibility with PBX type interfaces. The device does not provide transmission capability in this mode which is intended for idle line conditions. Loop supervision is provided by the switch hook detector and either high or low battery operation is supported.

Functionality

During Tip Open operation, the Tip switch is disabled and the Ring switch is enabled. The minimum Tip impedance is 30kΩ. The only active path through the device will be through the Ring switch.

In keeping with the MTU characteristics of the device, Ring will not exceed -56V when operating from the high battery. Though MTU does not apply to Tip Open, safety requirements are satisfied.

Power Denial

Overview

The power denial mode (111) will shutdown the entire device except for the logic interface. Loop supervision is not provided. This mode may be used as a sleep mode or to shut down the SLIC in the presence of fault conditions. Switching between high and low battery will have no effect during power denial.

Functionality

During power denial, both the Tip and Ring amplifiers are disabled, presenting high impedances to the line. The voltages at both outputs are near ground.

Thermal Shutdown

In the event the safe die temperature is exceeded due to a fault condition the device will automatically shut down. The thermal shutdown threshold is approximately 170^{o}C.When the device cools to a temperature below the thermal threshold it will power back up automatically. If the fault persists the part will continue to go in and out of thermal shutdown which can be observed as an oscillation on Tip or Ring. Programming power denial will shut down the device and stop the self cooling cycle.

Battery Switching

Overview

The integrated battery switch selects between high battery and low battery operation. The battery switch is controlled with the logic input BSEL. When BSEL is a logic high, the high battery (V_{BH}) is selected. A logic low will enable the low battery (V_{BL}). All operating modes of the SLIC will function from high or low battery, but it is strongly recommended Forward Loop Back be enabled only with the low battery.

Functionality

The logic control is independent of the operating mode decode. Independent logic control provides the most flexibility and will support all application configurations.

When changing device operating states, battery switching should occur simultaneously with or prior to changing the operating mode. In most cases, this will minimize overall power dissipation and prevent glitches on the $\overline{\text{DET}}$ output.

The only external component required to support the battery switch is a diode in series with the V_{BH} supply lead. In the event that high battery is removed, the diode allows the device to transition to low battery operation.

Low Battery Operation

All off hook operating conditions should use the low battery to minimize power dissipation. A typical low battery operating voltage for the SLIC is -24V, however this may be increased to support longer loop lengths or high loop current requirements. Standby conditions may also operate from the low battery if MTU compliance is not required, further reducing standby power dissipation.

High Battery Operation

Other than ringing, the high battery should be used for standby conditions which must provide MTU compliance. During standby operation the power consumption is typically 85mW with -100V battery. If ringing requirements do not require full 100V operation, then a lower battery will result in lower standby power.

High Voltage Decoupling

The 100V rating of the SLIC dictates a capacitor of higher voltage rating be used for decoupling. Suggested decoupling values for all device pins are 0.1µF. If the protection scheme shown in Figure 15 is implemented the V_{BH} decoupling capacitor should be increased to 0.47uF. This is done to minimize the turn-on time of the battrax device during negative surge transients. Standard surface mount ceramic capacitors are rated at 100V. For applications driven by low cost and small size, the decoupling scheme shown in Figure 10 could be implemented.

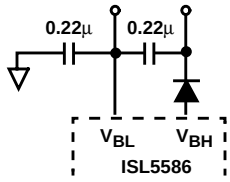


FIGURE 10. ALTERNATE DECOUPLING SCHEME

It is important to place an external diode between the V_{BH} pin and the decoupling capacitor. Connecting the decoupling capacitor directly to the V_{BH} pin will degrade the reliability of the device. Refer to Figure 15 for the proper arrangement. This applies to both single and stacked and decoupling schemes.

If V_{BL} and V_{BH} are tied together the battery switch function is overridden. In this case the external diode is not needed and the decoupling capacitor may be attached directly to V_{BH} pin.

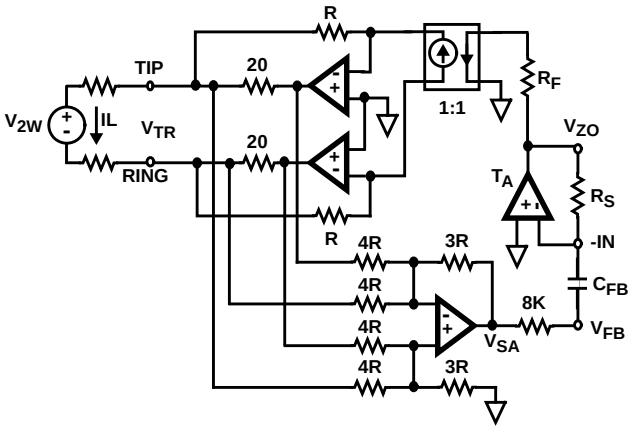


FIGURE 11. IMPEDANCE SYNTHESIS

Impedance and Gain Derivations

The feedback mechanism for monitoring the AC portion of the loop current consists of two amplifiers, the sense amplifier (SA) and the transmit amplifier (TA). The AC feedback signal is used for impedance synthesis. A detailed model of the AC feed back loop is provided below

Impedance Programming Resistor Derivation

The gain of the transmit amplifier, set by R_S, determines the programmed resistance of the SLIC. For complex line terminations R_S is replaced with a complex network Z_S (Figure 1). The capacitor C_{FB} blocks the DC component of the loop current. Figure 11 illustrates the impedance synthesis loop. Note that the ground symbols shown in Figures 11 through 14 represent AC grounds, not necessarily actual DC potentials.

The receiver block provides a single-ended to differential conversion with a voltage gain of 2. The voltage at Tip and Ring due to the feedback from V_{ZO} is shown in Equation 35.

$$VTR = -2 \times V_{ZO} \quad \text{(EQ. 35)}$$

The Feedback amplifier (TA) provides the programmable gain required for impedance synthesis to the Receiver block. The output voltage (V_{ZO}) is a function of the Sense Amplifier output voltage and the gain of the feedback amplifier, which can be substituted for V_{ZO}.

$$VTR = -2 \times V_{SA} \times \left(\frac{R_S}{8K\Omega}\right) \quad \text{(EQ. 36)}$$

The sense amplifier shown in Figure 11 is configured as a 4 input differential amplifier with a gain of 3/4. The output voltage, V_{SA}, is a function of the voltage across the Tip and Ring sense resistors (20Ω each) which can also be expressed in terms of loop current.

$$V_{SA} = -2 \times 20 \times IL \times (3/4) \quad \text{(EQ. 37)}$$

Substituting Equation 37 into Equation 35 and rearranging terms yields Z_0, the SLIC's synthesized 2-wire impedance. Rearranging and solving for R_S, Equation 39 shows the relationship between the impedance programming resistor and the programmed impedance.

$$Z_0 = \frac{V_{TR}}{IL} = 4 \times 20 \times IL \times \frac{3}{4} \times \frac{R_s}{8K\Omega} = 60 \times \frac{R_s}{8K\Omega} \quad \text{(EQ. 38)}$$

$$R_S = 133.3 \times Z_0 \quad \text{(EQ. 39)}$$

4-WIRE TO 2-WIRE GAIN

The 4-wire to 2-wire gain is defined as the gain from the differential receive input to the 2-wire load Z_L. The gain is a function of the terminating impedance, synthesized impedance and protection resistors and is illustrated in Figure 12. The input current to the receiver block Irx4w comes from the difference of the V_{RX} input current and the V_{ZO} feedback current. This current is fed to the Tip and Ring amplifiers and yields the relationship shown in Equation 40.

$$V_{TR} = -2 \times (V_{rx} - V_{ZO}) \quad \text{(EQ. 40)}$$

The voltage $V_{ZO,}$ is a function of the sense amplifier output voltage $V_{SA.}$

$$V_{Z0} = -V_{SA} \times \frac{R_S}{8K\Omega} \quad \text{(EQ. 41)}$$

V_{SA} can be expressed in terms of loop current as shown in Equation 42.

$$V_{SA} = -IL \times 2 \times 20 \times \frac{3}{4} \quad \text{(EQ. 42)}$$

Substituting Equation 42 into Equation 41 gives Equation 43.

$$V_{Z0} = -IL \times 2 \times 20 \times \frac{3}{4} \times \frac{R_S}{8K\Omega} \quad \text{(EQ. 43)}$$

The V_{Z0} term in Equation 40 can now be replaced by Equation 43 yielding Equation 44.

$$V_{TR} = -2 \times V_{rx} - 2\left(IL \times 2 \times 20 \times \frac{3}{4}\right) \times \left(\frac{R_S}{8K\Omega}\right) \quad \text{(EQ. 44)}$$

A loop equation can be derived for the 2-wire side that replaces V_{TR} as shown in the equation below.

$$V_{2W} + IL \times 2R_p = -2V_{rx} - IL\left(4 \times 20 \times \frac{3}{4}\right) \times \left(\frac{R_S}{8K\Omega}\right) \quad \text{(EQ. 45)}$$

Expressing IL in terms of V_{2W}/Z_L, rearranging, and solving for V_{2W} yields the relationship between the 2-wire voltage and the output of the Receive amplifier.

$$V_{2W} = -2V_{rx} \times \left(\frac{Z_L}{Z_L + Z_0 + 2R_P}\right) \quad \text{(EQ. 46)}$$

The differential voice input is configured for a gain of 1.4. The relationship between V_{RX} and the voice input is shown in Equation 47. Substituting for V_{RX}, the 4-2-Wire gain is shown in Equation 48. Note that the differential voice input is outside the impedance synthesis loop, so the gain of the receive amplifier has no effect on the SLIC's impedance.

$$V_{rx} = 1.4 \times (V_{RXP} - V_{RXM}) = 1.4 \times V_{RX4W} \quad \text{(EQ. 47)}$$

$$\frac{V_{2W}}{V_{RX4W}} = -2.8\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 48)}$$

When the combination of the device source impedance and the protection resistors equal the terminating impedance, the receive gain equals 2.92dB and is inverted with respect to the 4-wire input.

2-WIRE TO 4-WIRE GAIN

The 2-wire to 4-wire gain (G_{24}) is defined as the gain from the Tip and Ring terminals (V_{TR}) to the V_{TX} differential output.

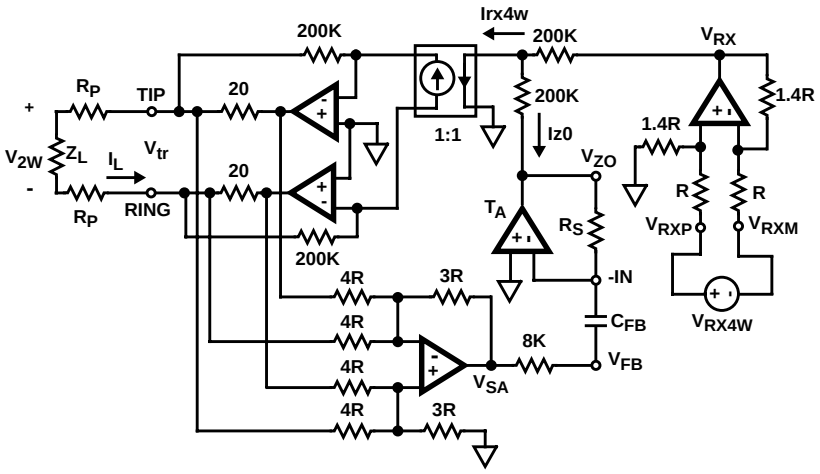


FIGURE 12. SCHEMATIC FOR 4-WIRE TO 2-WIRE GAIN DERIVATION

Note that in Figure 13, V_{TR} is referenced on the line side of the protection resistors.

On the 2-wire side, solving for IL in terms of V_{IN} gives Equation 49. Equations 50 and 51 show the relationship of V_{IN} to the outputs of the Sense Amplifier (V_{SA}) and the Feedback Amplifier (V_{Z0}) respectively.

$$IL = \left(\frac{V_{IN}}{Z_L + Z_0 + 2R_P}\right) \quad \text{(EQ. 49)}$$

$$V_{SA} = -\left(\frac{V_{IN}}{Z_L + Z_0 + 2R_P}\right) \times 2 \times 20 \times \left(\frac{3}{4}\right) \quad \text{(EQ. 50)}$$

$$V_{Z0} = -\left(\frac{V_{IN}}{Z_L + Z_0 + 2R_P}\right) \times 2 \times 20 \times \left(\frac{3}{4}\right) \times \frac{R_S}{8K\Omega} \quad \text{(EQ. 51)}$$

Simplifying Equation 51 in terms of Z_0 gives the following equation.

$$V_{Z0} = -\left(\frac{V_{IN}}{Z_L + Z_0 + 2R_P}\right) \times \frac{Z_0}{2} \quad \text{(EQ. 52)}$$

The resulting differential output voltage V_{TX4W}, is shown in Equation 53.

$$V_{TX4W} = V_{TXP} - V_{TXM} = V_{Z0} - (-V_{Z0}) = 2V_{Z0} \quad \text{(EQ. 53)}$$

Note that the gain from V_{Z0} to the differential output is outside the impedance synthesis loop and will have no effect on the SLIC's programmed impedance.

Substituting Equation 53 into Equation 52 and rearranging terms gives the gain from the 2-wire source (V_{IN}) to the differential output of the Transmit Amplifier.

$$\frac{V_{TX4W}}{V_{IN}} = -\left(\frac{Z_0}{Z_L + Z_0 + 2R_P}\right) \quad \text{(EQ. 54)}$$

If the combination of the protection resistors and the programmed impedance of the SLIC are equal to Z_L the voltage V_{TR} will be 1/2 V_{IN}. The 2-wire to 4-wire gain is defined by Equation 55.

$$\frac{V_{TX4W}}{V_{TR}} = -\left(\frac{2Z_0}{Z_L + Z_0 + 2R_P}\right) \quad \text{(EQ. 55)}$$

4-WIRE TO 4-WIRE GAIN

The 4-Wire to 4-Wire gain is defined in Equation 56 and is illustrated in Figure 14.The first term is identical to Equation 48.

$$\frac{V_{TX4W}}{V_{RX4W}} = \frac{V_{2W}}{V_{RX4W}} \times \frac{V_{TX4W}}{V_{2W}} \quad \text{(EQ. 56)}$$

The second term is derived in a similar manner as the 2-wire to 4-wire gain starting with Equation 57.

$$V_{2W} = IL \times Z_L \quad \text{(EQ. 57)}$$

Moving around the loop from the 2-wire side to the 4-wire output we solve for V_{SA} and V_{ZO}.

$$V_{SA} = -IL \times 2 \times 20 \times \frac{3}{4} = \frac{V_{2W}}{Z_L} \times 40 \times \frac{3}{4} \quad \text{(EQ. 58)}$$

$$V_{Z0} = \frac{V_{2W}}{Z_L} \times \left(\frac{R_S}{8K\Omega}\right) \times 40 \times \frac{3}{4} = \frac{V_{2W}}{Z_L} \times \frac{Z_0}{2} \quad \text{(EQ. 59)}$$

The relationship between V_{Z0} and the 4-wire output is shown in Equation 53. Substituting Equation 59 into Equation 53 yields Equation 60, the second term in Equation 56.

$$\frac{V_{TX4W}}{V_{2W}} = \frac{Z_0}{Z_L} \quad \text{(EQ. 60)}$$

Equations 48 and 60 can be combined to re-write the 4-wire to 4-wire gain equation.

$$\frac{V_{TX4W}}{V_{RX4W}} = -2.8\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right)\times\frac{Z_0}{Z_L} \quad \text{(EQ. 61)}$$

Simplifying the above yields the 4-wire to 4-wire gain.

$$\frac{V_{TX4W}}{V_{RX4W}} = -2.8\left(\frac{Z_0}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 62)}$$

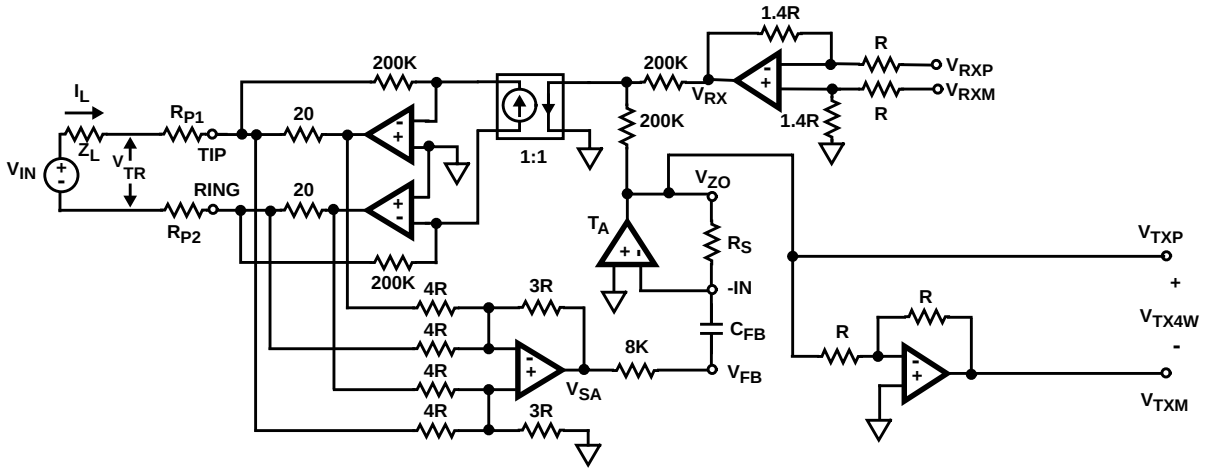


FIGURE 13. SCHEMATIC FOR 2-WIRE TO 4-WIRE GAIN DERIVATION

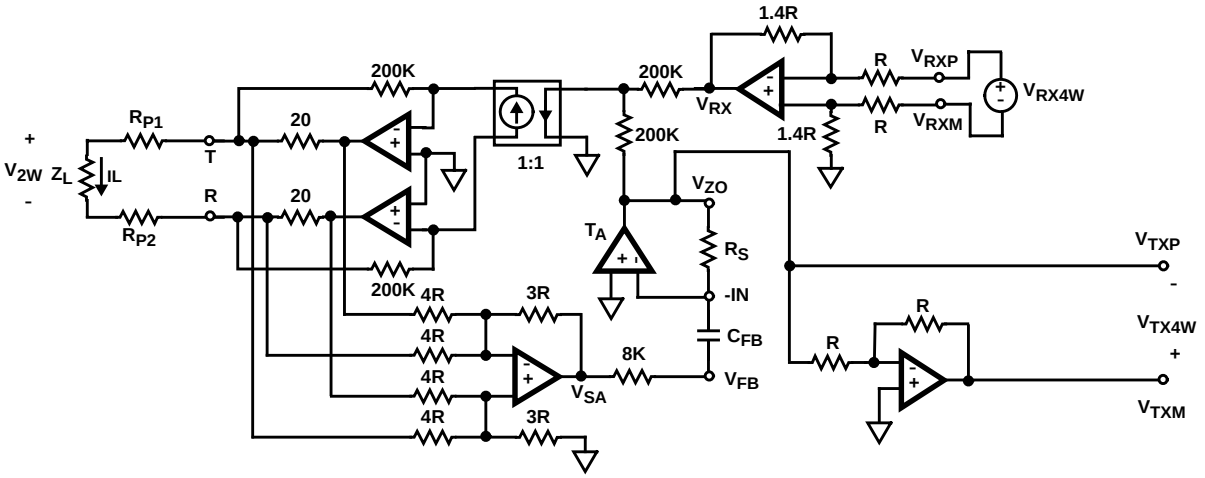


FIGURE 14. SCHEMATIC FOR 4-WIRE TO 4-WIRE GAIN DERIVATION

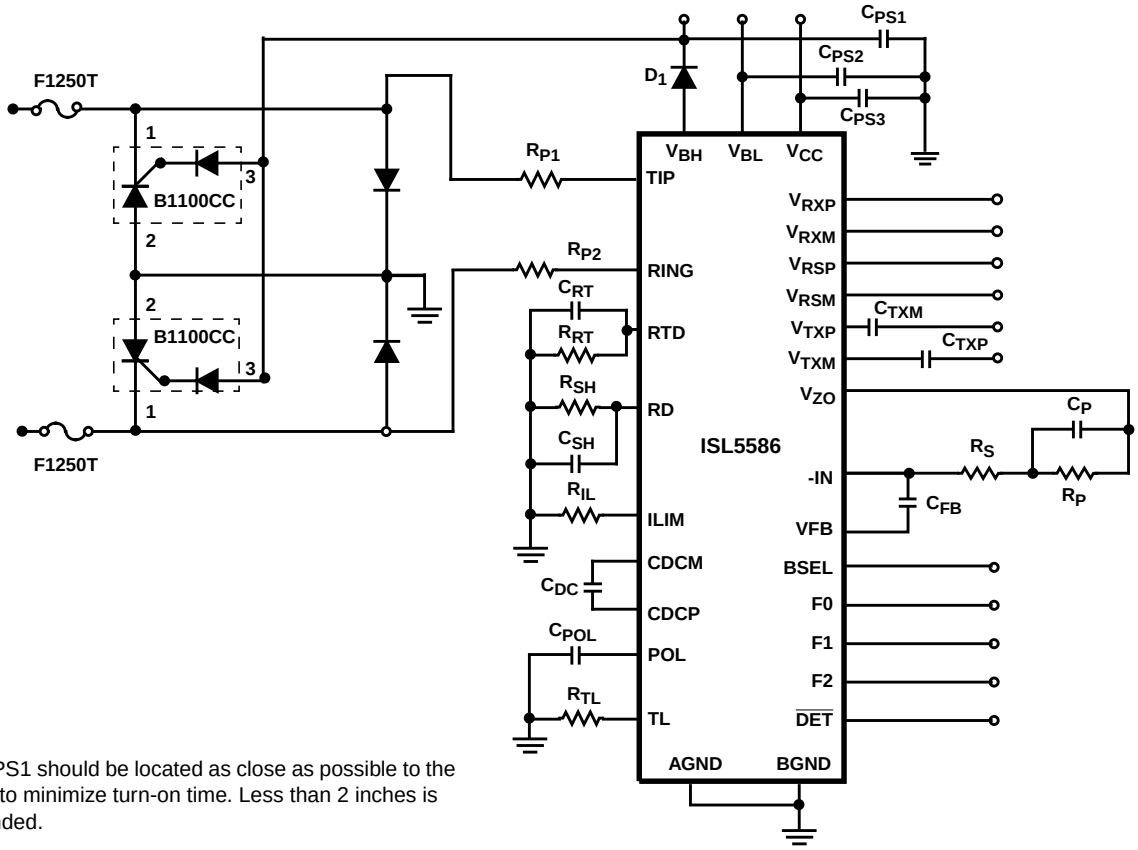
Pin Descriptions

PLCC	SYMBOL	DESCRIPTION
1	TIP	TIP Power Amplifier Output.
2	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND and SGND but should be connected to the same potential as AGND & SGND.
3	V_{BL}	Low Battery Supply Connection.
4	V_{BH}	High Battery Supply Connection.
5	BSEL	Selects between high and low battery, with a logic “1” selecting the high battery and logic “0” the low battery.

Pin Descriptions (Continued)

PLCC	SYMBOL	DESCRIPTION
6	F2	TTL Mode Control Input - MSB.
7	F1	TTL Mode Control Input.
8	F0	TTL Mode Control Input - LSB.
9	DET	Detector Output - This TTL output provides on-hook/off-hook status of the loop based upon the selected operating mode. The detected output will either be switch hook or ring trip.
10	V_{RSP}	Non-Inverting Ringing Signal Input - Analog input for driving 2-wire interface while in Ring Mode.
11	V_{RSM}	Inverting Ringing Signal Input - Analog input for driving 2-wire interface while in Ring Mode.
12	V_{TXP}	Transmit Output Voltage - AC couples to CODEC.
13	V_{TXM}	Transmit Output Voltage - AC couples to CODEC.
14	AGND	Analog Ground Reference. This pin should be externally connected to BGND.
15	POL	An External Capacitor on this pin sets the polarity reversal time.
16	V_{RXP}	Non-Inverting Analog Receive Voltage - 4-wire analog audio input voltage.
17	V_{RXM}	Inverting Analog Receive Voltage - 4-wire analog audio input voltage.
18	V_{ZO}	Connection Terminal for impedance matching programming resistor
19	-IN	Connection Terminal for high pass filter capacitor and impedance matching components.
20	V_{FB}	Connection Terminal for high pass filter capacitor and impedance matching components.
21	TL	Transient Current Limit Programming Resistor Connection Terminal.
22	V_{CC}	Positive Voltage Power Supply, +5V +/-5%.
23	C_{DCP}	DC Biasing Filter Capacitor - Positive Terminal.
24	C_{DCM}	DC Biasing Filter Capacitor - Negative Terminal.
25	RTD	Ring Trip Filter Network Connection Terminal.
26	I_{LIM}	Loop Current Limit programming resistor connection terminal.
27	RD	Switch Hook Detection threshold programming resistor connection terminal.
28	RING	RING Power Amplifier Output.

Basic Application Circuit



NOTE: CPS1 should be located as close as possible to the B1100CC to minimize turn-on time. Less than 2 inches is recommended.

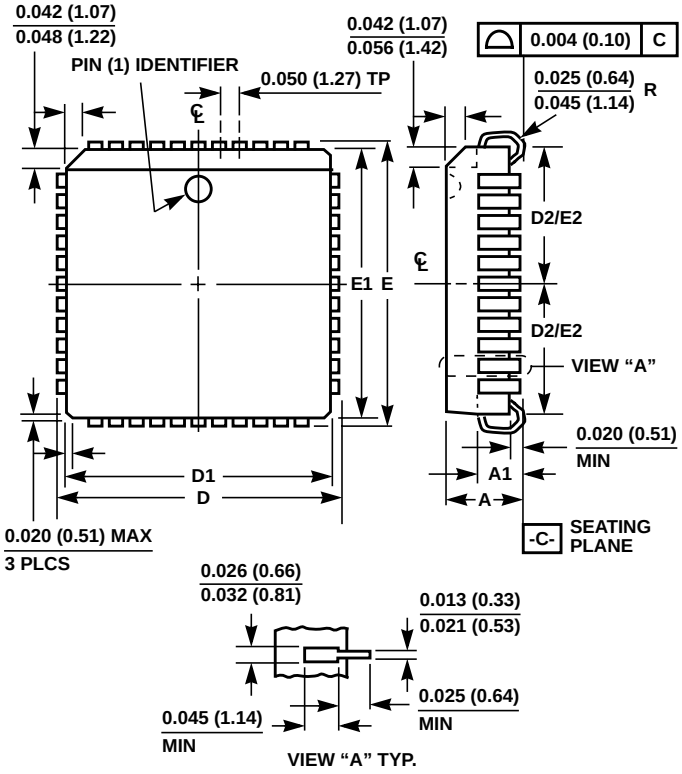
FIGURE 15. ISL5586 BASIC APPLICATION CIRCUIT

TABLE 2. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - Ringing SLIC	ISL5586	N/A	N/A
R_{TL}	17.8kΩ	1%	0.1W
R_{RT}	22.1kΩ	1%	0.1W
R_{SH}	40kΩ	1%	0.1W
R_{IL}	71.5kΩ	1%	0.1W
R_S	66.5kΩ	1%	0.1W
R_P	0Ω	1%	0.1W
C_P	Not Populated	20%	10V
C_{RT}, C_{POL}, C_{SH}, C_{TXP}, C_{TXM}	0.47µF	20%	10V
CFB	1.0µF	20%	10V
C_{DC}	4.7µF	20%	10V
C_{PS1}	0.47µF	20%	>100V
C_{PS2}, C_{PS3}	0.1µF	20%	100V
D_1	1N400X Type with Breakdown > 100V.		
$D_{2,}D_3$	1N4935 Type		
R_{P1}, R_{P2}	Protection resistor values are application dependent and will be determined by protection requirements. Standard applications will use ≥ 49Ω per side.		

Design Parameters: Ring Trip Threshold = 81mA_{PEAK}, Switch Hook Threshold = 15mA, Loop Current Limit = 24.6mA, Synthesize Device Impedance = (3*66.5kΩ)/400 = 498.8Ω, protection resistors = 50Ω, impedance across Tip and Ring terminals = 599Ω. Transient current limit = 100mA.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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