Preliminary

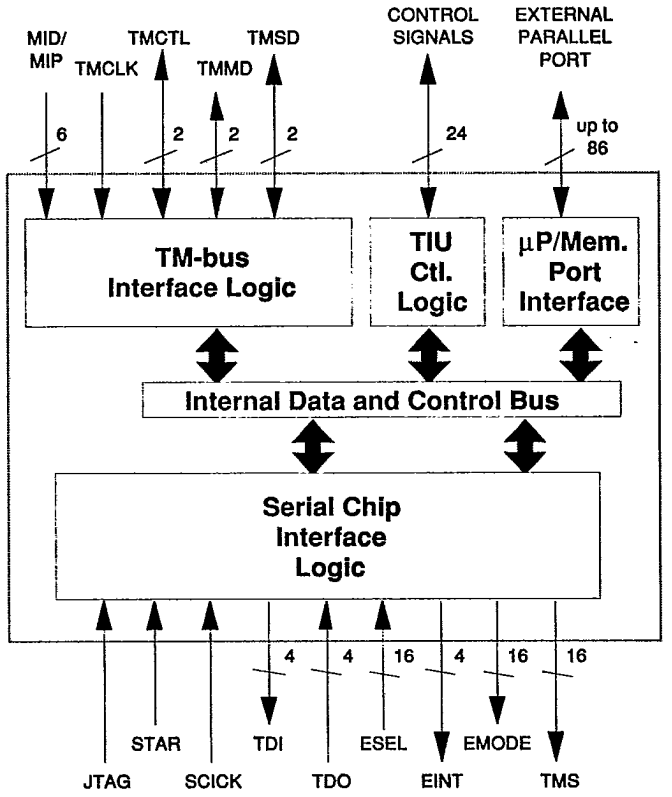
TEST-BUS INTERFACE UNIT

HTIU2000

T-52-33-05

FEATURES

- Connects to VHSIC Backplane TM-bus
  - TM-bus Specification, Version 3.0
  - TM-Bus Master or Slave Operation
  - 6.25 MHz Operation
- Chip Test-Port Supports
  - ETM Ring or Star Configurations
  - JTAG and IEEE 1149.1
- Selectable ETM/IEEE 1149.1 Configurations
  - Single Star Configuration (ETM only)
  - Quad Ring Configuration (up to 128 chips)
- External Processor/Memory Port
  - Motorola 68020
  - PACE 1750A
- Fully Self-testing
- IEEE-1076 VHDL Simulation Models Available
- PGA and Surface Mount Packages
- Low-Cost Design Kits Available



HTIU2000 - Internal Block Diagram

GENERAL DESCRIPTION

Honeywell's Test-bus Interface Unit (HTIU2000) is an easy to use, single-chip solution to the problem of interfacing with a test and maintenance hierarchy. The HTIU2000 provides complete protocol and hardware support for interfacing between the VHSIC Test and Maintenance (TM) bus and either the VHSIC Element Test and Maintenance (ETM) bus or the proposed IEEE 1149.1 (P1149.1) Joint Test Action Group (JTAG) bus.

The HTIU2000 meets all requirements as either a TM-bus master or slave as specified by the VHSIC Phase 2 Interoperability standards, TM-bus Specification, Version 3.0; all requirements of an ETM-bus controller as specified by the ETM-bus Specification, Version 3.0; and all requirements of the IEEE 1149.1/JTAG bus. The standard implementation of the HTIU2000 on maintenance and application modules lowers the program development risks and reduces the software needed on the maintenance module. In addition, using the HTIU2000 across the entire system encourages consistently maintainable modules.

Any combination of ports on the HTIU2000 can be used in an application—from low pincount, serial only applications to full parallel port applications. The HTIU2000 is available in a variety of packaging options, including leaded chip carriers, leadless chip carriers, and pin grid array packages.

The HTIU2000 is focused at Department of Defense applications. It supports VHSIC standard buses and is modeled with VHDL. The HTIU2000 chip is fabricated on a CMOS 1.2µm process. Full military screening and packaging are available.

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HTIU2000 allows system developers the capability to control at the module through component levels of test and maintenance hierarchy. The parallel port on HTIU2000 TM-bus master is the gateway to TM-bus mastery in the backplane environment. The complete set of VHSIC 3.0 TM-Bus core commands is implemented in the master and slave mode of operations. This basic set of commands is enhanced by a large application command set to optimize communication activity for test and maintenance. The application command set includes features for DMA transfer of commands and data to the TM-Bus and IEEE1149.1/ETM bus.

The HTIU2000 is not limited to a fixed set of commands on the IEEE1149.1/ETM bus. HTIU2000's flexible approach allows test and maintenance commands, specific to modules or components, to be encoded in its software and transmitted to the targeted device.

For non-intrusive monitoring, the HTIU2000 provides eight discrete input lines. These inputs can sample logic levels in an application without affecting function. Similarly, there are eight discrete outputs on the HTIU2000. These outputs can be used for maintenance purposes (i.e., selection of redundant busses), as drivers for indicators, or for any number of other purposes.

COMMAND
BYPASS
EXTEST
SAMPLE
INTEST
RUNBIST
IDCODE

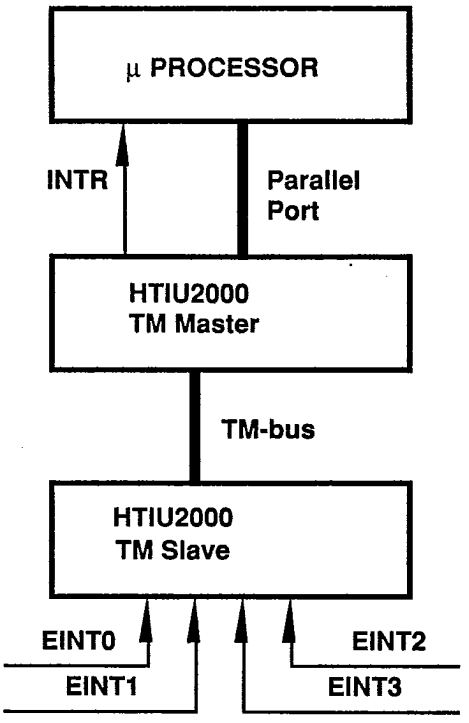
IEEE1149.1 Public Commands

Not only does the HTIU2000 furnish pathways for testing, but it has a Built-In-Self-Test (BIST) feature that can be invoked through either the parallel port or the TM port. As a TM-bus master, HTIU2000's BIST is executed by command from the parallel port. As a TM-bus slave, BIST is executed by command from the TM-bus master.

Interrupt handling is accommodated by the EINT inputs of the ETM bus. These interrupts are available in any configuration and can be passed upward through the TM-bus to the control processor via the interrupt output on the parallel port.

COMMAND FIELD	COMMAND
0000000	READ STATUS
0000001	INITIALIZE MODULE
0000010	RESET SLAVE
0000011	CONTEND FOR BUS
0000100	MULTICAST SELECT 0
0000101	MULTICAST SELECT 1
0000110	MULTICAST SELECT 2
0000111	MULTICAST SELECT 3
0001000	ENABLE INTERRUPT
0001001	DISABLE INTERRUPT
0001010	RESERVED COMMAND
0001011	RESERVED COMMAND
0001100	RESERVED COMMAND
0001101	RESERVED COMMAND
0001110	RESERVED COMMAND
0001111	RESERVED COMMAND

VHSIC 3.0 Core Commands



Interrupt Hierarchy

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ABSOLUTE MAXIMUM RATINGS *

Parameter	Description	Ratings		Units
		Min.	Max.	
V_{DD}	DC Supply Voltage (referenced to VSS)	-0.3	6.5	V
V_I	Voltage on Any Pin (referenced to VSS)	-0.3	VDD+0.3	V
I_I	DC Input Current	-10	10	mA
T_S	Storage Temperature	-65	+150	°C

* Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at theses levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Limits			Units
		Min.	Nom.	Max.	
V_{DD}	DC Supply Voltage (referenced to Vss)	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature	-55	25	+125	°C

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{DD} ≤ 5.5V)

Parameter	Description	Limits		Units	Test Conditions
		Min.	Max.		
V_{IL}	Low Level Input Voltage		0.8	V	VDD = 4.5 V
V_{IH}	High Level Input Voltage	2.0		V	VDD = 4.5 V
V_{OL}	Low Level Output Voltage		0.4	V	IOL = 5 mA VDD = 4.5 V
V_{OH}	High Level Output Voltage	4.2		V	IOL = 5 mA VDD = 4.5 V
I_{IL}	Leakage Current	-10	+10	µA	VSS≤ VI≤VDD
I_{OZ}	Output Leakage Current	-10	+10	µA	VSS≤VIO ≤ VDD Output = High Z
PD	Power Dissipation		1.5	W	VIH = VDD, VIL = VSS COut = 50 pF, Fclk = max

AC CHARACTERISTICS FOR CLOCKS (-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{DD} ≤ 5.5V)

Parameter	Description	Limits		Units	Test Conditions
		Min.	Max.		
F_{PCLK}	PCLK Clock Frequency		12.5	MHz	-55°C≤T_A≤+125°C 4.5V≤V_{DD}≤5.5V
F_{TMCLK}	TMCLK Clock Frequency		6.25	MHz	-55°C≤T_A≤+125°C 4.5V≤V_{DD}≤5.5V
F_{SCICK}	SCICK Clock Frequency		6.25	MHz	-55°C≤T_A≤+125°C 4.5V≤V_{DD}≤5.5V

AC CHARACTERISTICS FOR PARALLEL PORT

Extensive AC timing characteristics and timing diagrams for the parallel port are available upon request from Honeywell. Please specify Motorola 68020, Pace 1750A and /or memory DMA configurations .

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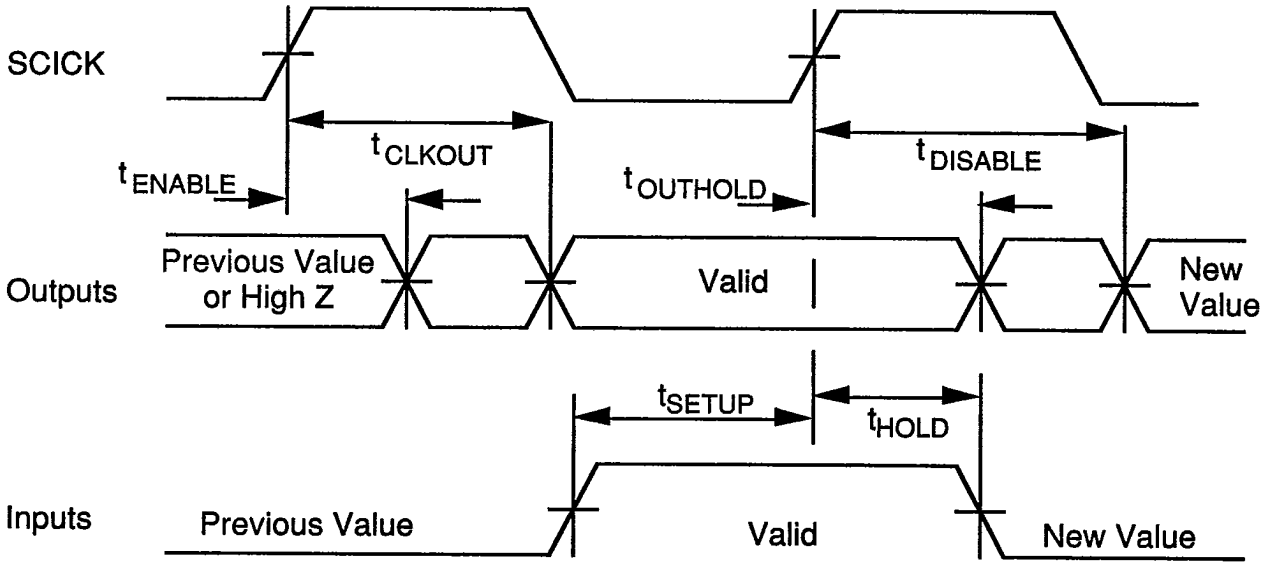
AC ELECTRICAL SPECIFICATIONS FOR SCI SIGNALS

Symbol	Parameter	Min.	Max.	Units
tCLKOUT Clock to output delay (CL = 50 pF)	TDI[3:0]		100	ns
	TMS[15:0]		65	ns
	ESEL[15:0]		65	ns
	EMODE[15:0]		65	ns
tOUTHOLD Output hold time from clock (CL =25 pF)	TDI[3:0]	10		ns
	TMS[15:0]	10		ns
	ESEL[15:0]	10		ns
	EMODE[15:0]	10		ns
tENABLE Enable delay from clock	TDI[3:0]	10		ns
tDISABLE Disable delay from clock	TDI[3:0]		100	ns
tSETUP Input setup time to clock	TDO[3:0]	25		ns
	EINT[3:0]	10		ns
tHOLD Input hold time to clock	TDO[3:0]	5		ns
	EINT[3:0]	5		ns



SCI Port Timing Diagram

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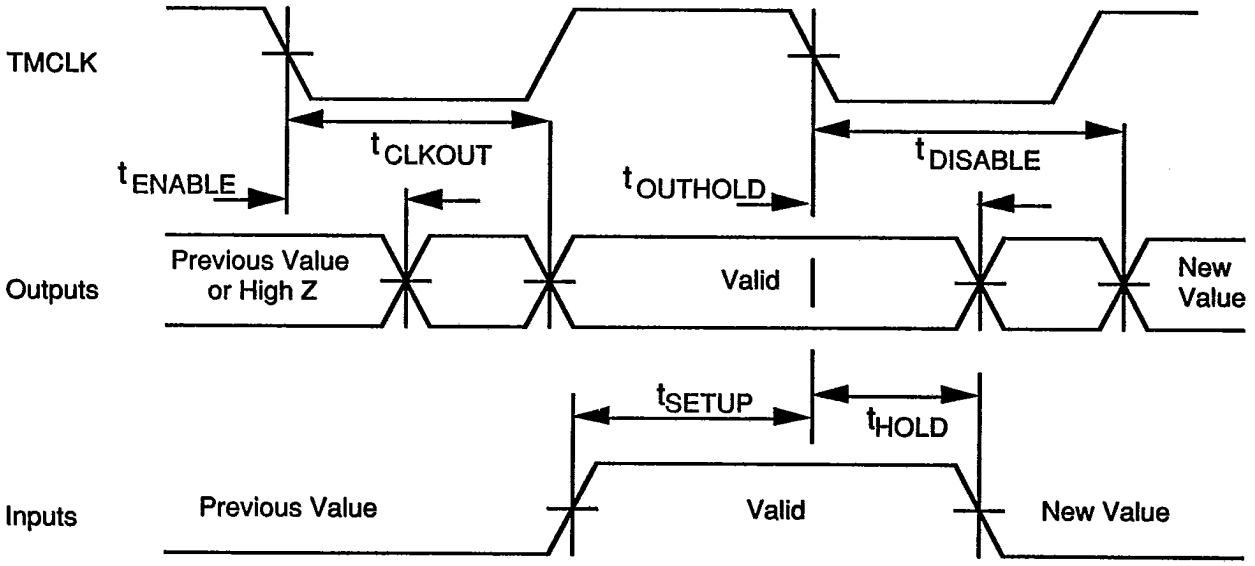
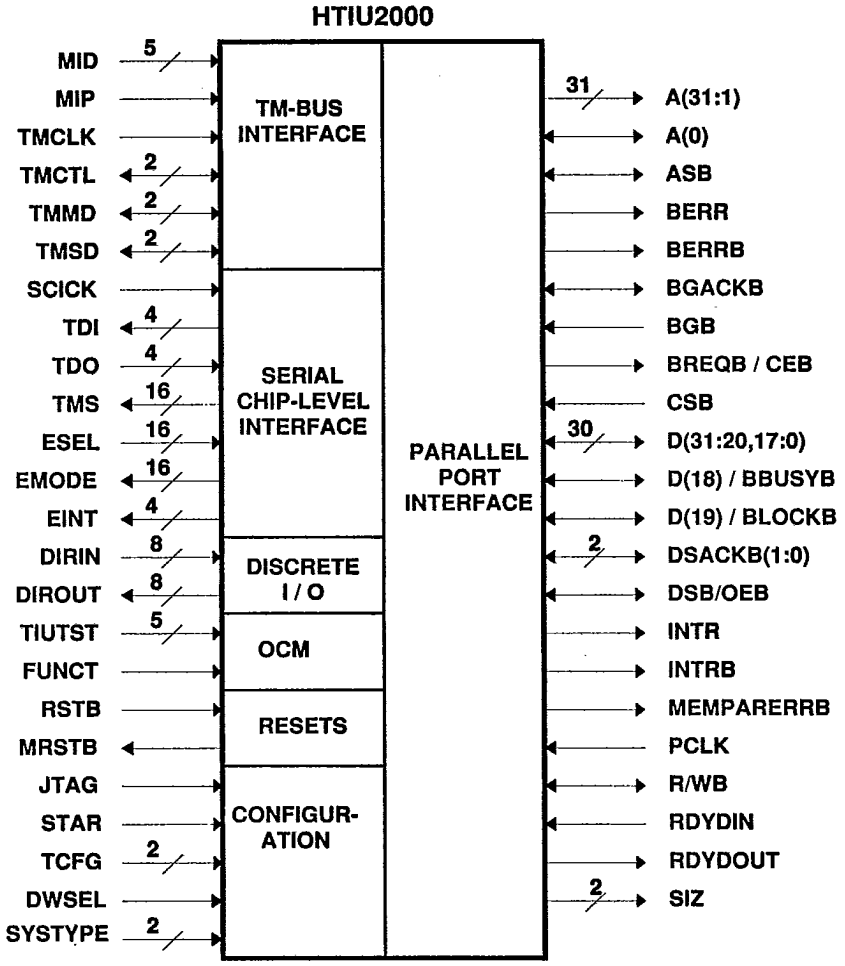
AC ELECTRICAL SPECIFICATIONS FOR TMI SIGNALS

Symbol	Parameter	Min.	Max.	Units
tCLKOUT Clock to output delay (CL = 50 pF)	TMCTL[1:0]		60	ns
	TMMD[1:0]		100	ns
	TMSD[1:0]		100	ns
tOUTHOLD Output hold time from clock (CL =25 pF)	TMCTL[1:0]	10		ns
	TMMD[1:0]	10		ns
	TMSD[1:0]	10		ns
tENABLE Enable delay from clock	TMCTL[1:0]	10		ns
	TMMD[1:0]	10		ns
	TMSD[1:0]	10		ns
tDISABLE Disable delay from clock	TMCTL[1:0]		60	ns
	TMMD[1:0]		100	ns
	TMSD[1:0]		100	ns
tSETUP Input setup time to clock	TMCTL[1:0]	65		ns
	TMMD[1:0]	65		ns
	TMSD[1:0]	35		ns
tHOLD Input hold time to clock	TMCTL[1:0]	10		ns
	TMMD[1:0]	10		ns
	TMSD[1:0]	10		ns



TMI Port Timing Diagram

SIGNAL AND I/O PORT DEFINITIONS



Test-bus Interface Unit–Signal Diagram

TM BUS CONFIGURATION

TCFG[1:0] — TM Configuration (TCFG) signals indicate whether the HTIU2000 is a TM-bus master or TM-bus slave and whether or not the secondary TM-bus port (port 1) is to be used in the system design. When TCFG[1] is connected to VDD, the HTIU2000 acts as a TM-bus master. When TCFG[1] is connected to VSS or is unconnected, the HTIU2000 is configured as a slave on the TM-bus. When TCFG[0] is connected to VDD, the secondary TM-bus port will be ignored. When TCFG[0] is connected to VSS or is unconnected, the secondary TM-is available.

TM-BUS INTERFACE

MID[4:0] — The TM-bus Module Identification inputs are used to set individual TM-bus slave addresses. (See VHSIC 3.0 TM-bus Specification section 4.2.2.5)

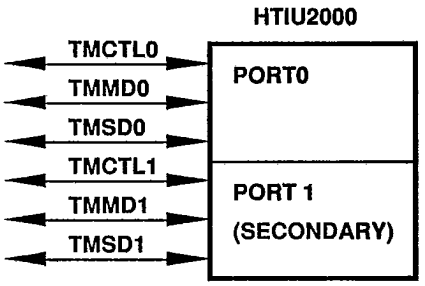
MIP — The TM-bus Module Identification Parity signals must be set such that the modulo-2 sum of the MID and MIP lines is equal to 1. (See VHSIC 3.0 TM-bus Specification section 4.2.2.5)

TMCLK — The TM-bus CLOCK signal synchronizes all control and data transfer operations. The HTIU2000 will support TM-bus CLOCK frequencies up to 6.25 MHz.

TMCTL[1:0] — The TM-bus (ports 1 and 0) CONTROL signals indicate whether the TM-bus is in the data transfer or pause/idle state. These signals are outputs for the master configuration and inputs for the slave configuration.

TMMD[1:0] — The TM-bus (ports 1 and 0) MASTER DATA signals are used to transmit slave addresses, instructions, and data from the TM-bus Master to the TM-bus Slave. These signals also indicate whether the bus is in the pause or idle state when between data packets. These signals are outputs for the master configuration and inputs for the slave configuration.

TMSD[1:0] — The TM-bus (ports 1 and 0) SLAVE DATA signals are used to transmit acknowledgements, data, and/or interrupts from the TM-bus Slave to the TM-bus Master. These signals are outputs for the slave configuration and inputs for the master configuration.



TM-BUS PORT PIN ASSIGNMENTS

SERIAL CONFIGURATION

JTAG — The JTAG signal configures the HTIU2000 as either an IEEE1149.1/ETM bus controller or as only an ETM-bus controller. When JTAG is set to VSS, the chip is a dedicated ETM Controller. When JTAG is connected to VDD or is unconnected, the HTIU2000 drives both IEEE 1149.1 and ETM bus control signals.

STAR — The STAR signal indicates whether the HTIU2000 is connected as an ETM-bus controller in a single star configuration or whether it is to be connected as controller of four (4) serial rings. When STAR is connected to VSS or is unconnected, the HTIU2000 controls up to 4 ETM-bus or IEEE 1149.1 bus rings. When STAR is connected to VDD, the HTIU2000 controls up to 32 ETM-bus slaves in a star configuration.

SERIAL INTERFACE

SCICK — The IEEE 1149.1 or ETM bus test clock, SCICK, signal. The HTIU2000 will support the full range of IEEE 1149.1 and ETM bus clock frequencies, from zero (0) to 6.25 MHz. If the HTIU2000 is used as a controller of a ETM-bus in the ring configuration, then the SCICK must match the TM-bus clock frequency.

TDI[3:0] — The serial chip-level bus (IEEE 1149.1 or ETM bus) test data in, TDI, signal transmits data from the HTIU2000 to the elements on the bus. In the star configuration, all TDI signals have the same data. In the ring configuration, TDI[3:0] are connected to rings 3 down to 0, respectively.

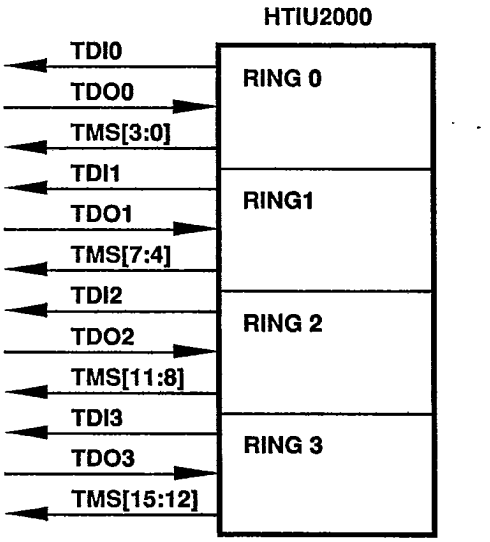
TDO[3:0] — The serial chip-level bus (IEEE 1149.1 bus or ETM) test data out, TDO, signal receives data from the elements on the bus. In the star configuration, the high-impedance TDO signals from the bus elements are grouped by eight in order to reduce loading requirements on each element. In the ring configuration, the TDO signal from the last element on the ring for rings 3 down to 0, are connected to TDO[3:0], respectively.

TMS[15:0] — The test mode select (TMS) signal for IEEE1149.1 bus. The TMS[15:0] signals drive IEEE 1149.1 elements when in a JTAG/IEEE ring configuration, ETM-bus elements when in an ETM-bus star configuration, and are tri-stated when in the ETM-bus only ring configuration.

ESEL[15:0] — The ETM-bus SELECT signal. In the ETM star configuration, these signals comprise 16 of the 32 ETM-bus select signals (along with the TMS signals). In ring configurations, four bits of the ESEL bus drive each ring.

EMODE[15:0] — The ETM-bus MODE signal. In the star configuration, only EMODE[3:0] are used and all four EMODE signals are the same. In ring configurations, all EMODE signals are used and are the same.

EINT[3:0] — The ETM-bus INTERRUPT signal. The HTIU2000 supports asynchronous operation of the EINT[3:0] signals. These interrupts are also available to users of the IEEE 1149.1 bus.



PIN ASSIGNMENTS FOR IEEE149.1 RINGS

DISCRETE INPUTS AND OUTPUTS

DIRIN[7:0] — The direct input signals may be read by the user from either the TM-bus or microprocessor port. These general-purpose signals may be used for any number of purposes.

DIROUT[7:0] — The direct output signals may be set by the user from either the TM-bus or microprocessor port. These general-purpose signals may be used to select from redundant buses, drive indicators, or any other purpose.

ON-CHIP-MONITOR (OCM)

TIUTST[4:0] — The HTIU2000 test signals are used only during manufacture component or board-level testing. The TIUTST[4:0] are the HTIU2000's IEEE 1149.1 test port and provide another way to access the HTIU2000's self-test as well as all on-chip test techniques.

FUNCT — The functional mode signal overrides the TIUTST[4:0] signals, forcing those signals internally to values consistent with functional mode. When the FUNCT signal is connected to VDD, the TIUTST signals need not be connected.

RESET SIGNALS

RSTB — The active-low HTIU2000 reset signal resets the entire HTIU2000. This reset signal is typically asserted during power-up.

MRSTB — The active-low Module Reset signal is asserted when it receives the standard TM-bus Initialize Module command or when the HTIU2000's RSTB signal is asserted.

EXTERNAL PARALLEL PORT

A[31:1] — The Address output signals are used for HTIU2000's direct access of memory.

A[0] — The bidirectional Address signal is used as an output for direct addressing of memory and as an input so that a microprocessor may address either the HTIU2000's data or status register. During microprocessor read and writes of the HTIU2000, a zero on A[0] (VSS) addresses the PPI status register and a one on A[0] (VDD) addresses the PPI data register.

ASB — The active-low, bidirectional Address Strobe indicates whether a valid address is on the bus. This signal is used for interfacing to the MC68020 and memory.

BERR — The Bus Error signal is asserted if there has been an error in transferring data over the parallel bus.

BERRB — The active-low Bus Error signal is the inverse of the BERR signal.

BGACKB — The bidirectional, active-low Bus Grant Acknowledge signal indicates that the HTIU2000 has assumed mastership of the parallel bus.

BGB — The active-low Bus Grant input signal indicates that the microprocessor has granted control of the parallel bus to the HTIU2000.

BREQB/CEB — The active-low Bus Request signal is generated by the HTIU2000 to request control of the parallel bus from the microprocessor and is an active-low Chip Enable output for controlling memory accesses when the HTIU2000 is configured without microprocessor.

CSB — The active-low Chip Select signal selects the HTIU2000 for an operation on the parallel bus.

D[31:20],D[17:0] — The bidirectional Data bus may be configured for 16- or 32-bit width by the DWSEL signal when used in a Motorola system. In a Pace 1750A system, only D[16:0] are used.

D[18] / BBUSYB — This is a Data bus signal when used with a MC68020 and is reconfigured as an active-low Bus Busy signal when used with the 1750A. The BBUSYB signal establishes the beginning and ending of a bus cycle.

D[19] / BLOCKB — This is a Data bus signal when used with a MC68020 and is reconfigured as an active-low Bus Lock signal when used with the 1750A. The BLOCKB is asserted by the device controlling the bus (including the HTIU2000) to lock out the bus from other devices.

DSACKB[1:0] — The active-low Data Strobe Acknowledge signals are used to interface to the MC68020 and to memory in a Motorola system. The HTIU2000 drives the data strobe acknowledge line when it is being accessed by the microprocessor and listens to data strobe acknowledge when it is performing a bus cycle in DMA mode..

DSB / OEB — This signal is an active-low bidirectional Data Strobe, DSB, when connected to a microprocessor and an active-low Output Enable, OEB, when configured with memory only. The DSB signal indicates that valid data has been placed on the bus. The OEB signal initiates memory reads.

INTR — The Interrupt signal is generated by the HTIU2000 to interrupt the microprocessor. Once asserted, it remains active until the PPI status register is read.

INTRB — The active-low Interrupt signal is the inverse of the INTR signal.

MEMPARERRB — The active-low Memory Parity Error is generated by the HTIU2000 to indicate to the microprocessor that a memory parity error has been detected.

PCLK — The parallel port clock signal synchronizes parallel port operations. The HTIU2000 support PCLK frequencies up to 12.5 MHz.

R/WB — The bidirectional, Read / Write signal indicates the direction of data transfer on the parallel bus. HTIU2000 listens to the read/write signal when it is being accessed by the microprocessor and drives the read/write signal when it is performing a bus cycle in DMA mode.

RDYDIN — The Ready Data In input interfaces to the PACE 1750A system memory. HTIU2000 listens to this signal when it performs bus cycles to memory in DMA mode.

RDYDOUT — The Ready Data Out signal interfaces to the PACE 1750A. HTIU2000 drives the signal in response to a data strobe when it is being accessed by the processor.

SIZ[1:0] — The Size signals indicate the size of the data word output by the HTIU2000 in a Motorola system to memory in DMA mode. Since HTIU2000 only communicates in 16-bit words, SIZ[1:0] is always driven to 10 (binary).

PARALLEL PORT CONFIGURATION

DWSEL — The Data Width Select signal selects between 16-bit (DWSEL = VSS) and 32-bit (DWSEL=VDD) data word widths.

SYSTYPE[1:0] — The System Type signals indicate to the HTIU2000 whether it is connected to memory, a PACE 1750A, or a MC68020.

TM-BUS INTERFACE

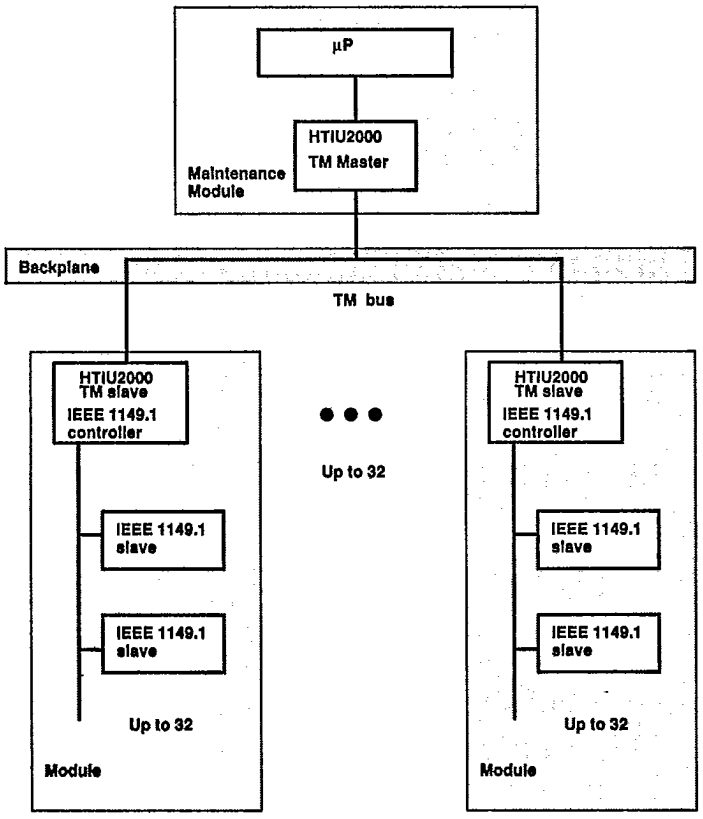
The HTIU2000 's TM-bus port is fully compliant to the VHSIC TM-bus Specification, Version 3.0 and allows the HTIU2000 to participate on the TM-bus as either a master or a slave. The HTIU2000 has two TM-bus ports and can be configured to use either of the ports.

The TM-bus is intended to reduce the cost of developing maintainable subsystems by providing an interoperable test interface to modules from different vendors. The TM-bus, dedicated to test and maintenance functions, may be used to enhance the maintainability of systems that use any number of parallel system buses (e.g., Pi-bus, FutureBus, etc.). The TM-bus was developed by representatives of the VHSIC Phase 2 contractors (Honeywell, IBM, and TRW) in response to the DoD's requirement for interoperability.

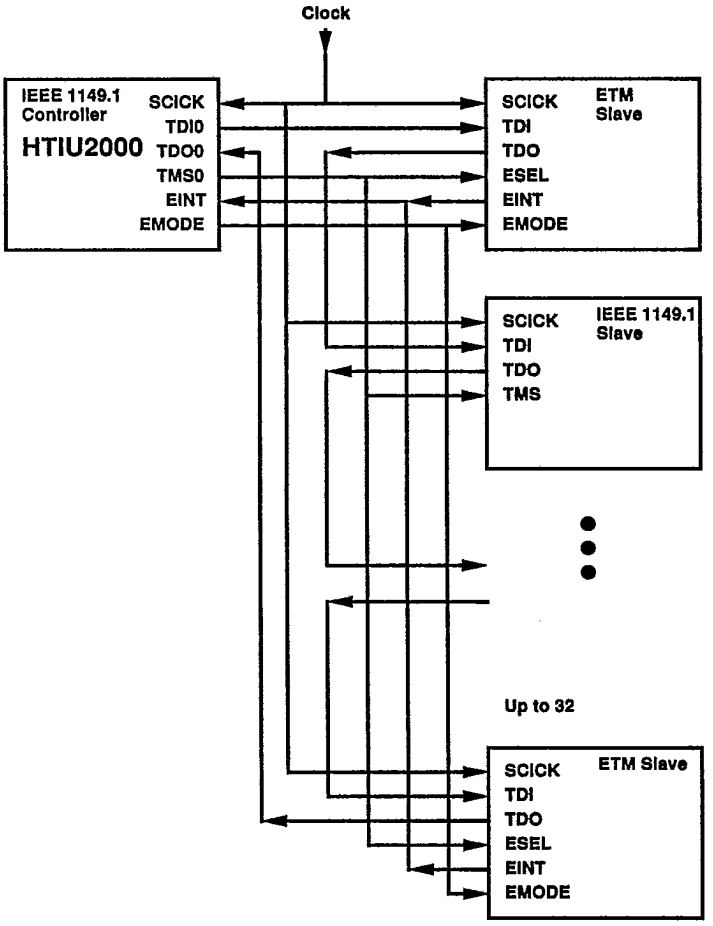
SERIAL INTERFACE

The serial interface port on the HTIU2000 communicates with the chip level test and maintenance bus. This port is fully compatible with the IEEE 1149.1/JTAG bus and the ETM-bus. The HTIU2000 supports the asynchronous interrupt capability specified by the VHSIC ETM-bus. The ring configuration is supported for both busses and the star configuration is supported for the ETM bus. The HTIU2000 is capable of handling up to four serial loops (rings) of 32 elements each (128 maximum). Both 1149.1/JTAG and ETM compatible components are allowed on the same ring.

1149.1/JTAG/ETM-bus Ring Configuration: In this configuration, signals are replicated to provide four complete 1149.1/JTAG/ETM-bus ports which support the ring configuration. The signal number indicates the 1149.1/JTAG/ETM-bus ring port (0 to 3).



TM - IEEE 1149.1 Hierarchy



IEEE 1149.1 Bus Ring Configuration

IEEE 1149.1 / ETM Bus Ring Configuration

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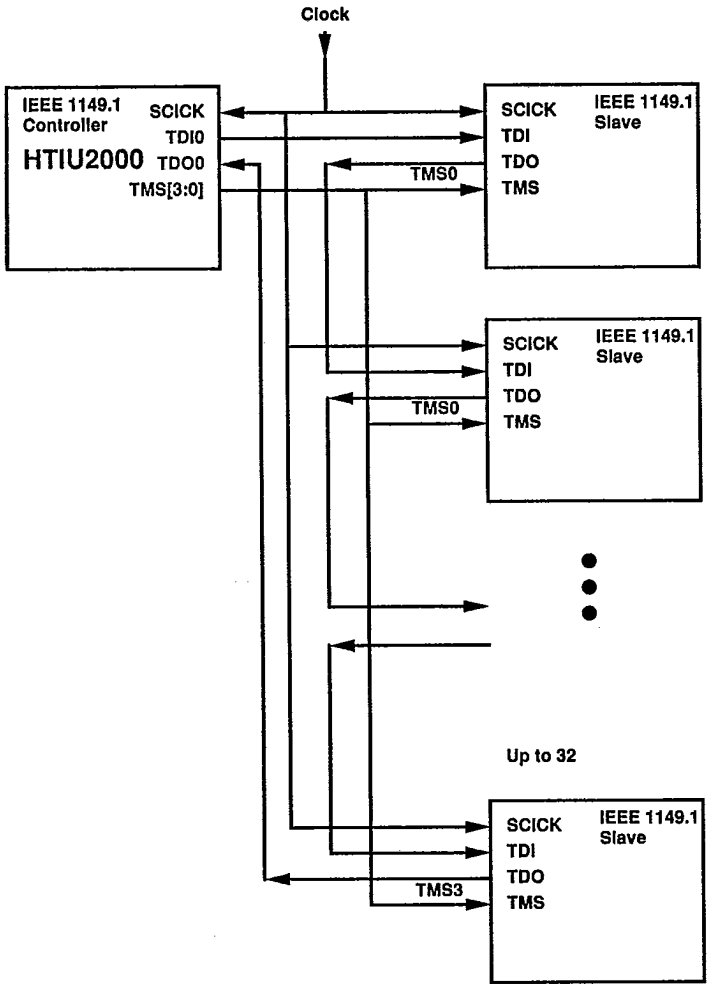
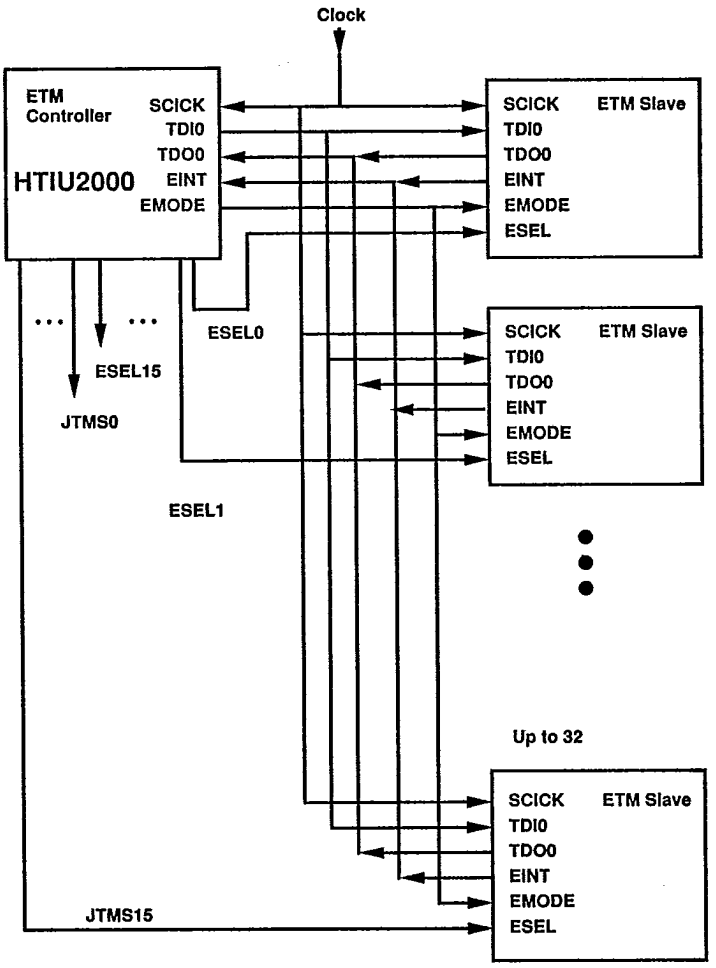
IEEE 1149.1 (only) Configuration: In this configuration, TMS is replicated as four sets (TMS[15:12], TMS[11:8], TMS[7:4] and TMS[3:0]) for four rings in order to decrease the drive requirements for the signal which could be connected to as many as 32 elements.



IEEE 1149.1 Ring Configuration

ETM Star Configuration: In this configuration, some signals are replicated (four each of TDI, TDO, ESEL, and EMODE) in order to decrease the drive requirements for the signals which would normally be connected to as many as 32 elements.



ETM-Bus Star Configuration

External Parallel Port

The parallel port of the HTIU2000 allows the device to access external memory and/or a microprocessor or microcontroller. This feature of the HTIU2000 can be used to substantially reduce traffic on the TM-bus.

The HTIU2000 supports the Motorola 68020 and the PACE 1750A (made by Performance Semiconductor Corporation). By connecting the parallel port to a processor, the HTIU2000 can effectively be controlled by the processor.

The parallel port can also be connected to external standard memory and access the memory in a normal method (read or write to the memory) or to test the memory.

TYPICAL APPLICATIONS

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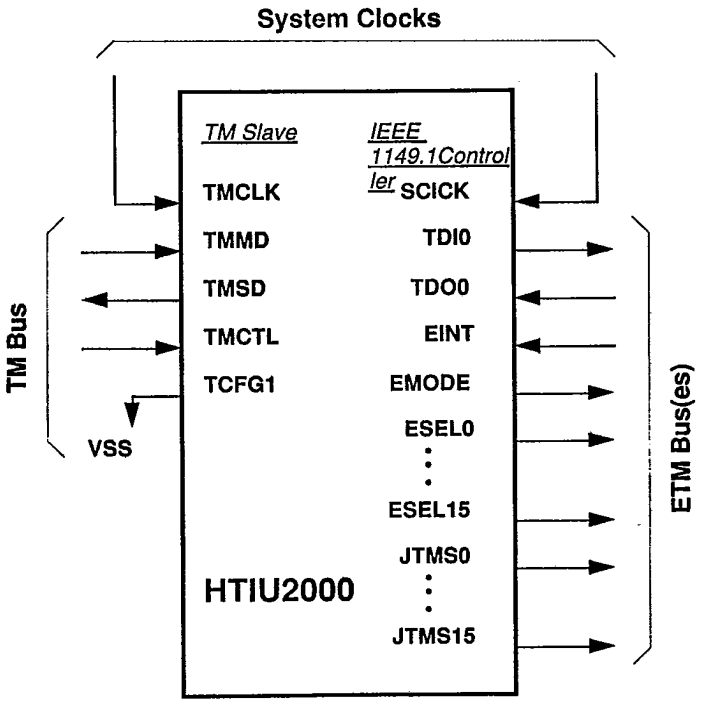
TM to IEEE 1149.1/ETM-Bus Translation

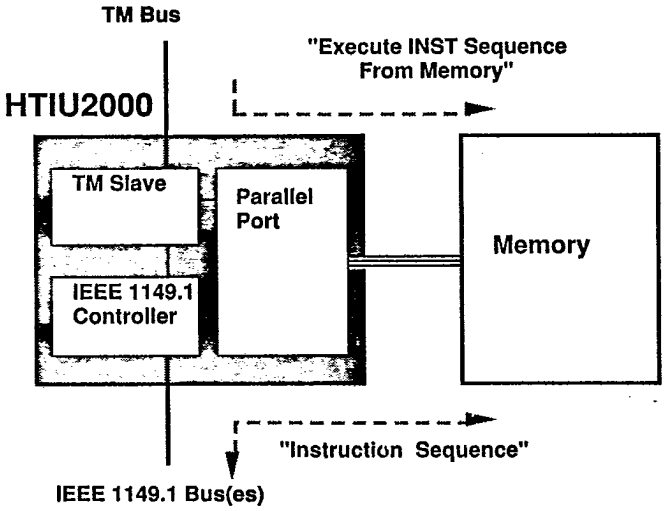
The HTIU2000 may be used without any external memory or micro-controller to provide complete TM-bus to IEEE 1149.1/ETM-bus translation. In this configuration, all element instructions and data must be transmitted over the TM-bus. The HTIU2000 fully supports "Blank" scan operations where the IEEE 1149.1/ETM-bus is held in the scan mode and the select signal is asserted for the indicated number of clock cycles. This "Blank" scan operation is sometimes necessary to control self-test or system multiple clock stepping.



TM to IEEE 1149.1/ETM-Bus Translation

IEEE 1149.1/ETM-Bus Controller

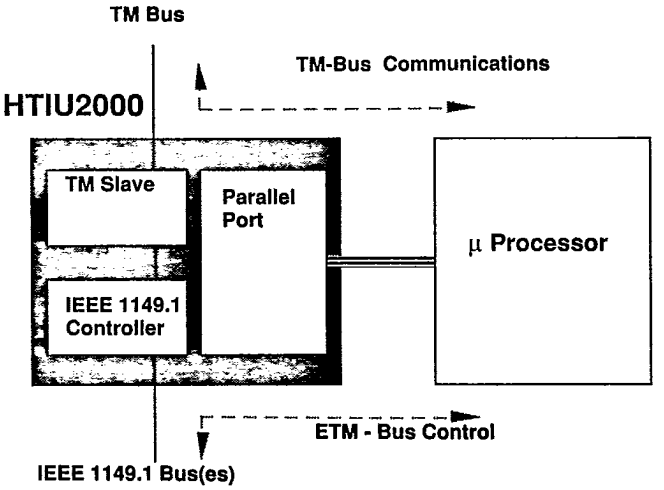
An external memory may be connected to the HTIU2000's parallel port which can substantially reduce the amount of TM-bus traffic. In this configuration, a TM-bus command can instruct the HTIU2000 to "dump" one or more IEEE 1149.1/ETM-bus operations from the external memory. The target for the operation on the IEEE 1149.1/ETM-bus and the location of the instruction sequence is specified by the TM-bus command. This configuration is particularly useful for executing initial program load and self-test sequences. The test-bus interface unit and memory combination may also be used to save the state of the IEEE 1149.1/ETM-bus elements.



IEEE 1149.1 - Bus Controller Configuration

Test Processor

An external microprocessor may be connected (with or without external memory) to provide complete remote test processing capability. In this configuration, the microcontroller could be connected to additional components such as non-volatile memory and a Time-Stress Measurement Device.



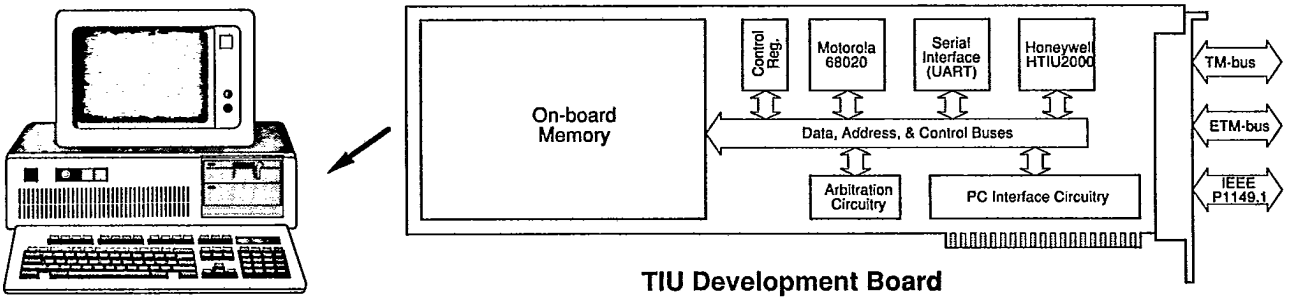
Test Processor Configuration

HTIU2000KT DESIGN KIT

Honeywell has assembled everything needed to evaluate the HTIU2000 into a single design kit, the HTIU2000KT. This kit includes:

- Six (6) HTIU2000 samples packaged in Pin Grid Array (PGA) packages.
- Two (2) Zero Insertion Force (ZIF) sockets.
- A two-day training class on integrating design-for-test using the HTIU2000.
- An HTIU2000 development board for IBM-compatible personal computers. Using the system developer's software, this board will turn a personal computer into a development system or serial tester capable of controlling IEEE 1149.1, ETM, and TM-bus ports.
- HTIU2000 documentation including HTIU2000 Users' Guide and application notes.
- Applications support to aid the design-in.

In addition to the HTIU2000KT design kit, full IEEE 1076 VHDL models are available for the HTIU2000 at an additional cost. These VHDL models will allow the simulation of behavior of the HTIU2000 in the module design.



TIU Development Board

For more information on the HTIU2000 or other Honeywell products contact:

Jerry Sperling
Honeywell Inc.
Solid State Electronics Center
12001 State Highway 55
Plymouth, MN 55441
(612) 541-2694