BUF-01

PRECISION BUFFER/VOLTAGE FOLLOWER WITH OVERVOLTAGE PROTECTION

FEATURES

- **Output Error Fully Specified** ..... **250μV Maximum**
- **Low Input Offset Voltage** ..... **60μV Typical**
- **Pin Compatible with LM110**
- **Drives 10kΩ Load to ±10V**
- **Low Voltage Gain Error** **0.001%**
- **Excellent Power Supply Rejection Ratio** ..... **106dB Typical**
- **Low Output Impedance** ..... **0.03Ω Typical**
- **Low Input Noise Voltage** ..... **0.8μV_{p-p} Maximum**

GENERAL DESCRIPTION

The BUF-01 is the first precision voltage follower tested and guaranteed with a **Maximum Output Error** specification. **Maximum Output Error** includes errors introduced by offset voltage, input bias current, gain, CMRR and output loading. This ensures that the TOTAL output error will not exceed the maximum under any combination of input or output.

Pin compatible with the LM110, the BUF-01 features low output impedance (0.03Ω typical), high gain and excellent power supply rejection (106dB typical) with extremely low input voltage noise.

Fabricated with Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation™ Process," the BUF-01 utilizes on-chip zener-zap trimming to achieve very low offset voltage with excellent long-term stability. This eliminates the need for offset nulling in all but the most stringent applications.

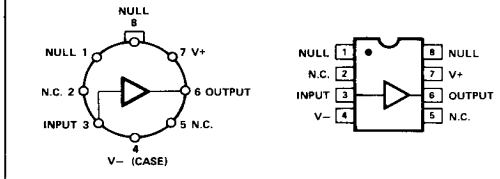
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	HERMETIC PACKAGE TO-99 8-PIN	HERMETIC PACKAGE DIP 8-PIN	OPERATING TEMPERATURE RANGE
100	BUF01AJ*	BUF01AZ*	MIL
100	BUF01EJ	BUF01EZ	COM
150	BUF01BJ*	BUF01BZ*	MIL
150	BUF01FJ	BUF01FZ	COM

* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

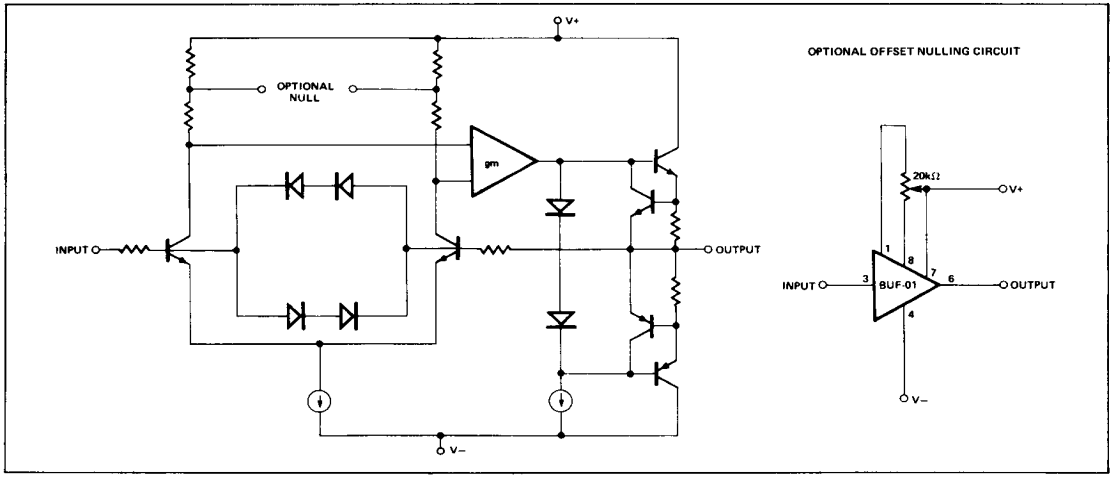
PIN CONNECTIONS



TO-99 (J-Suffix)

8 PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
BUF-01A, BUF-01B ..... −55°C to +125°C
BUF-01E, BUF-01F ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

Package Type	Maximum Ambient Temperature Rating	Derate Above Maximum Ambient Temperature
TO-99(J)	80°C	7.1mW/°C
8 PIN HERMETIC DIP (Z)	75°C	6.7mW°C

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, T_A = + 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-01A BUF-01E MIN	TYP	MAX	BUF-01B BUF-01F MIN	TYP	MAX	UNITS
Maximum Output Error	OUT_{error}	V_{IN} = +10V, 0V, −10V R_S = 0 to 20kΩ $R_L \geq$ 10KΩ (in all combinations.)	—	0.1	0.25	—	0.2	0.5	mV
Input Offset Voltage	V_{OS}	V_{IN} = 0V, R_S = 50Ω	—	60	100	—	80	150	µV
Input Current	I_{IN}		—	±2.0	±7.0	—	±2.0	±7.0	nA
Input Resistance	R_{IN}		—	10^{11}	—	—	10^{11}	—	Ω
Large-Signal Voltage Gain Error	A_{VE}	$R_L \geq$ 10kΩ, V_O = ±10V	—	0.001	0.0025	—	0.001	0.005	%
Output Resistance	R_O	V_O = 0, I_O = 0	—	0.03	—	—	0.03	—	Ω
Input Voltage Range	V_{IN}		±12.0	±13.0	—	±12.0	±13.0	—	V
Output Current	I_O	$-5V \leq V_O \leq +5V$	—	±13	—	—	±13	—	mA
Power Supply Rejection Ratio	PSRR	$\pm 3V \leq V_S \leq \pm 18V$	—	5	20	—	7	32	µV/V
Small Signal Bandwidth	BW	(Note 1)	0.4	0.7	—	0.4	0.7	—	MHz
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 2)	—	0.5	0.8	—	0.5	0.8	$\mu V_{p\text{-}p}$
Input Noise Current	$i_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 2)	—	15	40	—	15	40	$pA_{p\text{-}p}$
Slew Rate	SR	$R_L \geq$ 10kΩ (Note 1)	0.1	0.2	—	0.1	0.2	—	V/µs
Power Consumption	P_d	V_S = ± 15V, V_O = 0 V_S = ± 3V, V_O = 0	— —	75 6	120 —	— —	80 8	150 —	mW

ELECTRICAL CHARACTERISTICS at V_S = ± 15V, − 55°C ≤ T_A ≤ + 125°C for BUF-01A and FUB-01B, 0°C ≤ T_A ≤ + 70°C for BUF-01E and BUF-01F, unless otherwise noted.

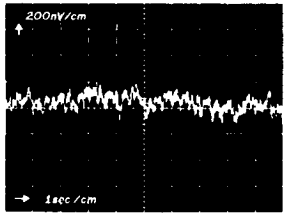
PARAMETER	SYMBOL	CONDITIONS	BUF-01A BUF-01E MIN	TYP	MAX	BUF-01B BUF-01F MIN	TYP	MAX	UNITS
Maximum Output Error	OUT_{error}	V_{IN} = +10V, 0V, −10V; R_S = 0 to 20kΩ $R_L \geq$ 10kΩ (in all combinations)	—	0.2	0.35	—	0.4	0.8	mV
Input Offset Voltage	V_{OS}	V_{IN} = 0V, R_S = 50Ω	—	80	280	—	120	400	µV
Large-Signal Voltage Gain Error	A_{VE}	$R_L \geq$ 10kΩ, V_O = ±10V	—	0.002	0.0035	—	0.002	0.008	%
Average Input Offset Voltage Drift	TCV_{OS}	(Note 2)	—	0.2	1.8	—	0.3	2.5	µV/°C
Input Current	I_{IN}		—	—	±12	—	—	±12	nA
Average Input Current Drift	TCI_{IN}	(Note 2)	—	10	120	—	12	120	pA/°C
Input Voltage Range	V_{IN}		±11.5	±12.6	—	±11.0	±12.6	—	V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	7	32	—	10	51	µV/V
Power Consumption	P_d	V_O = 0	—	80	150	—	90	180	mW

NOTES:

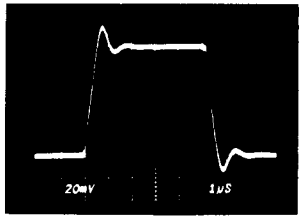
1. Guaranteed by design.
2. Sample tested.

TYPICAL PERFORMANCE CURVES

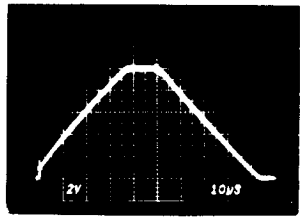
BUF-01 LOW FREQUENCY NOISE



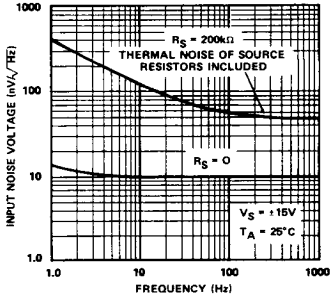
SMALL-SIGNAL TRANSIENT RESPONSE



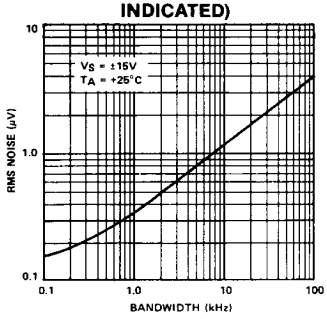
LARGE-SIGNAL TRANSIENT RESPONSE



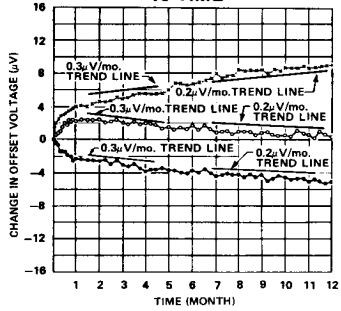
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



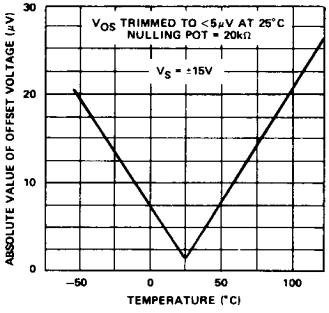
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



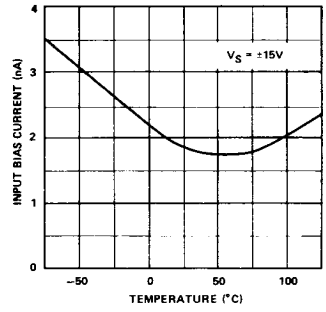
OFFSET VOLTAGE STABILITY vs TIME



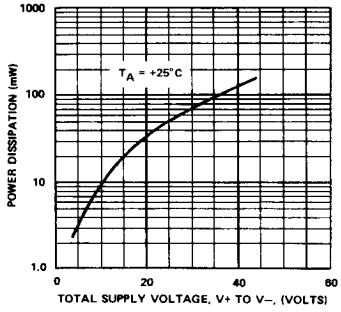
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

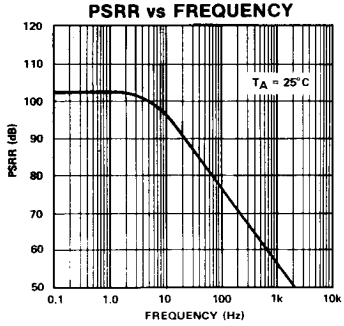


POWER CONSUMPTION vs POWER SUPPLY

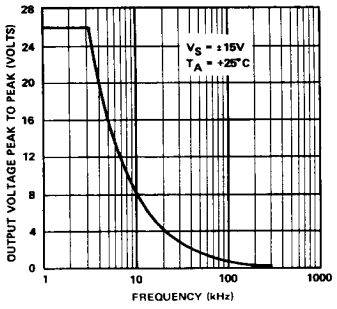


TYPICAL PERFORMANCE CURVES

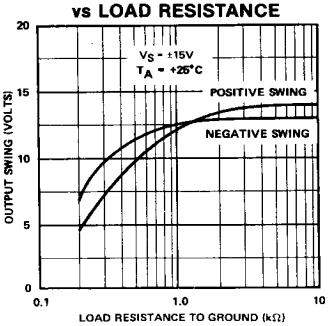
PSRR vs FREQUENCY



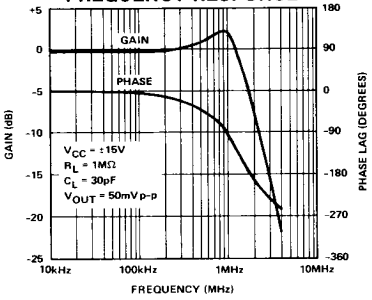
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



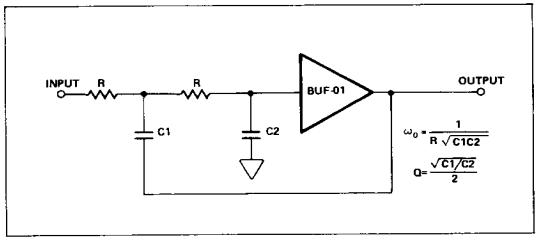
OUTPUT VOLTAGE vs LOAD RESISTANCE



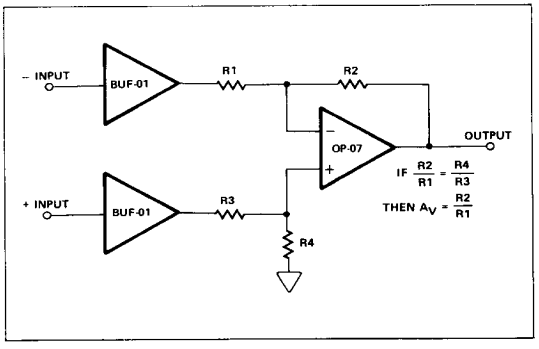
GAIN AND PHASE vs FREQUENCY RESPONSE



SECOND-ORDER LOWPASS FILTER

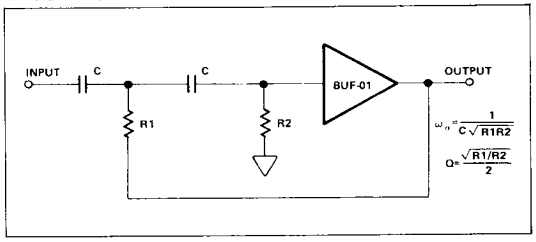


HIGH-IMPEDANCE DIFFERENTIAL AMPLIFIER

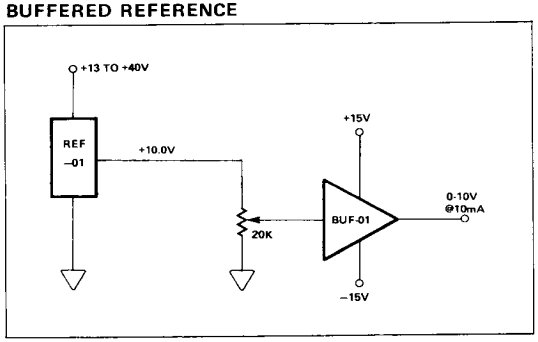


TYPICAL APPLICATIONS

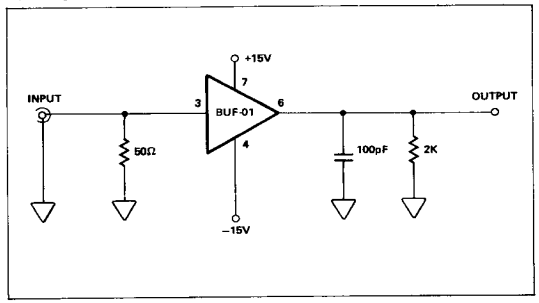
SECOND-ORDER HIGHPASS FILTER



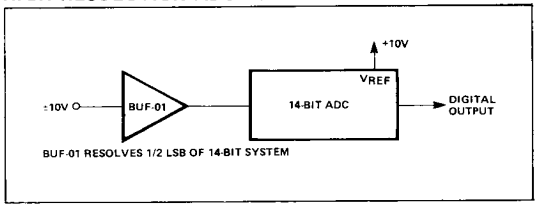
BUFFERED REFERENCE



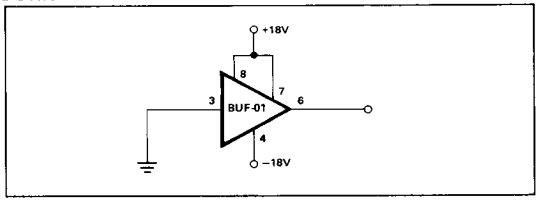
TRANSIENT RESPONSE TEST CIRCUIT



HIGH RESOLUTION ADC INPUT BUFFER



BURN-IN CIRCUIT



MAXIMUM OUTPUT ERROR

The **Maximum Output Error** specification combines errors introduced by offset voltage, input bias current, gain, CMRR, and device output impedance. The specification is 100% tested for a given combination of source resistance, load resistance, and input voltages. The tedious chore of performing a worst case summation of component error terms is not necessary.

To assist the designer who has a specific application, the individual parameters of offset voltage, input current, voltage gain and PSRR are also given.

It should be noted that an error analysis may yield a figure higher than the Maximum Output Error specification. This is due to the potential cancellation of the effects of one error source by another. In situations such as this, the Maximum Output Error specification supersedes results from any error analysis.