ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16821FT

LOW-VOLTAGE 20-BIT D-TYPE FLIP-FLOP WITH 3.6V TOLERANT INPUTS AND OUTPUTS

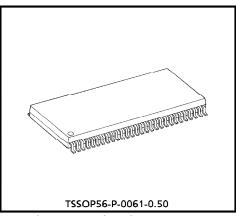
The TC74VCX16821FT is a high performance CMOS 20-bit D-TYPE FLIP-FLOP. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. The twenty flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CK) transition.

When the OE input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge. PRELIMINARY



Weight: 0.25g (Typ.)

FEATURES

Low Voltage Operation : $\nabla_{CC} = 1.8 \sim 3.6 \text{V}$

High Speed Operation : $t_{pd} = TBD \text{ (max.)}$ at $V_{CC} = 3.0 \sim 3.6 \text{V}$

: $t_{pd} = TBD \text{ (max.)} \text{ at } V_{CC} = 2.3 \sim 2.7 \text{V}$

: $t_{pd} = TBD (max.)$ at $V_{CC} = 1.8V$

3.6V Tolerant inputs and outputs.

Output Current : $I_{OH}/I_{OL} = \pm 24mA \text{ (min.)}$ at $V_{CC} = 3.0V$

: $I_{OH}/I_{OL} = \pm 18mA \text{ (min.)}$ at $V_{CC} = 2.3V$

: $I_{OH}/I_{OL} = \pm 6mA \text{ (min.)}$ at $V_{CC} = 1.8V$

Latch-up Performance : ±300mA

ESD Performance : Human Body Model > ±2000V

: Machine Model > ±200V

Package

(Thin Shrink Small Outline Package)

Power Down Protection is provided on all inputs and outputs.

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SYMBOL PIN ASSIGNMENT 56 1CK 10E 10E EN2 56 1CK **-** C1 55 1D1 1Q1 28 2OE EN4 1Q2 54 1D2 29 2CK GND 53 GND **>** C3 2____ 1Q1 55 52 1D3 1D 1Q3 1D1 -2▽ 3____ 1Q2 54 1Q4 51 1D4 1D2 52 VCC50 VCC - 1Q3 1D3 · 6 1Q4 51 1Q5 1D5 49 1D4 49 8 1Q6 1D6 48 1D5 — 1Q5 48 1Q7 1D7 47 10 1D6 — 1Q6 10 1Q7 47 GND 46 GND 1D7 12 1Q8 45 1Q8 45 1D8 1D8 13 1Q9 44 1Q9 44 1D9 13 1D9 43 14 1Q10 1Q10 43 1D10 1D10 15 2Q1 42 42 2D1 2Q1 15 2D1 3D 4▽ 16 2Q2 41 202 41 2D2 2D2 · 17 2Q3 40 40 2D3 2Q3 2D3 19 2Q4 39 GND GND 18 RELIMIT 20 2Q5 38 2D 2Q4 19 21 2Q6 36 2Q5 20 2D4 37 2D6 -34 23 2Q6 36 2D6 – 2Q7 2D7 33 24 V_{CC} 22 35 V_{CC} — 2Q8 2D8 26 2Q9 31 34 2D7 2Q7 23 2D9 27 2Q10 30 33 2D8 2Q8 2D10 GND 32 GND 2Q9 26 31 2D9 2Q10 27 30 2D10 20E 29 2CK 28 (TOP VIEW)

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The information contained herein is subject to change without notice.

TRUTH TABLE

INPUT			OUTPUT
1 OE	1CK	1D1-1D10	1Q1-1Q10
Н	Х	Х	Z
L	ا ا	Х	Qn
L		L	L
L		Н	Н

INPUT			OUTPUT
2 OE	2CK	2D1-2D10	2Q1-2Q10
Н	Х	Х	Z
L	7_	Х	Qn
L		L	┙
L		Н	Н

X : Don't Care Z : High impedance Qn : No change

SYSTEM DIAGRAM

