#### TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

### 524,288 WORDS × 8 BIT STATIC RAM

### **DESCRIPTION**

The TC554001FI/FTI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V±10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 85 ns.It is automatically placed in low-power mode at 200  $\mu$ A standby current (max) when chip enable (CE) is asserted high. There are two control inputs. CE is used to select the device and for data retention control, and output to provide foct memory access. This device is well suited to various microprocessor system. enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40 to 85°C, the TC554001FI/FTI can be used in environments exhibiting extreme temperature conditions. The TC554001FI/FTI is available in a standard plastic 32-pin small-outline package(SOP) and 32-pin thin-small-outline package(TSOP).

### **FEATURES**

- Low-power dissipation Operating: 55 mW/MHz (typical)
- Standby current of 200 µA (maximum)
- Single power supply voltage of  $5 \text{ V} \pm 10 \%$
- Power down features using CE
- Data retention supply voltage of 2.0 to 5.5 V
  Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of − 40° to Package: 80°C

### Access Time (maximum)

	TC5510	01FI/FTI
	-85	-10
Access Time	85 ns	100 ns
CE Access Time	85 ns	100 ns
OE Access Time	45 ns	50 ns

SOP32-P-525-1.27 (FI) TSOP II 32-P-400-1.27 (FTI)

(Weight: 1.14 g typ) (Weight: 0.51 g typ)

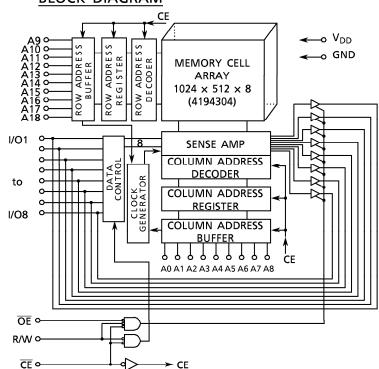
### PIN ASSIGNMENT (TOP VIEW)

○ <u>32 PIN</u> I	FI/FTI
A18 ☐ 1	32  V <sub>DD</sub>
A16 🗖 2	31 🗀 🗡 A15
A14 🔲 3	30 🗀 🗡 A17
A12 🔲 4	29  □ R/W
A7 🗌 5	28 🗀 🗡 A13
A6 🗆 6	27 🗀 🗚
A5 🗌 7	26 🗀 🗚 9
A4 🛮 8	25 🗀 🗛 11
A3 🗌 9	24 🔲 🛛 OE
A2 🔲 10	23 🗀 🗡 A10
A1 🛘 11	22 🗀 🔀
A0 🗌 12	21 🔲 1/08
I/O1 🗖 13	20 🔲 1/07
I/O2 🔲 14	19 🔲 1/06
I/O3 🗖 15	18 🗀 1/05
GND 🗆 16	17 🔲 1/04

### **PIN NAMES**

	_
A0 to A18	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE	Chip Enable
I/O1 to I/O8	Data Input/Output
$V_{DD}$	Power (+ 5 V)
GND	Ground

### **BLOCK DIAGRAM**



- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws. The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

## **OPERATION MODE**

OPERATION MODE	CE	ŌĒ	R/W	I/O1 to I/O8	POWER
Read	L	L	Н	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	×	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Disabled	L	Н	Н	High-Z	I <sub>DDO</sub>
Standby	Н	×	×	High-Z	I <sub>DD\$</sub>

Note: × = don't care. H=logic high. L=logic low.

# **ABSOLUTE MAXIMUM RATINGS**

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	- 0.3* to 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
$P_{D}$	Power Dissipation	0.6	W
Tsolder	Soldering Temperature (10 s)	260	°C
Tstrg.	Storage Temperature	– 55 to 150	°C
Topr.	Operating Temperature	- 40 to 85	°C

<sup>\*</sup> -3.0 V when measured at a pulse width of 50 ns

# <u>DC RECOMMENDED OPERATING CONDITIONS</u> (Ta = $-40^{\circ}$ to $85^{\circ}$ C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.4	-	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	- 0.3*	-	0.6	V
$V_{DH}$	Data Retention Supply Voltage	2.0	-	5.5	V

<sup>\*</sup> -3.0 V when measured at a pulse width of 50 ns

# <u>DC CHARACTERISTICS</u> (Ta = $-40^{\circ}$ to 85 °C, $V_{DD} = 5 \text{ V} \pm 10\%$ )

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	$V_{IN} = 0 V \text{ to } V_{DD}$			-	_	± 1.0	μΔ
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V			- 1.0	-	-	mA
l <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V			2.1	-	ı	mA
llo	Output Leakage Current	$\overline{CE} = V_{IH} \text{ or } R/W = V_{IL} \text{ or } \overline{OE} = V_{IH}$ $V_{OUT} = 0 \text{ V to } V_{DD}$			ı	ı	± 1.0	μΑ
		$\overline{CE} = V_{IL}$ and R/W = $V_{IH}$	Tavala	min	1	1	80	mA
DDO1	On anothing Comment	I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	Tcycle	1 <i>μ</i> s	-	15	-	IIIA
	Operating Current	$\overline{\text{CE}} = 0.2 \text{ V} \text{ and } \text{R/W} = \text{V}_{\text{DD}} - 0.2 \text{ V}$	T1.	min	-	-	70	
I <sub>DDO2</sub>		$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$I_{OUT} = 0 \text{ mA}$ Tcycle Total Tcycle Trycle Total Trycle Try		-	10	_	mA
I <sub>DD\$1</sub>		CE = V <sub>IH</sub>		-	-	3	mA	
I <sub>DD\$2</sub>	Standby Current	$\overline{CE} = V_{DD} - 0.2 V$ $V_{DD} = 2.0 \text{ to } 5.5 \text{ V}, \text{ Ta} = -40^{\circ} \text{ to } 8$	35°C		-		200	μΑ

# <u>CAPACITANCE</u> (Ta = $25^{\circ}$ C, f = 1 MHz)

SYMBOL	PARAMETER	AMETER TEST CONDITION			
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF	
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF	

Note: This parameter is periodically sampled and is not 100% tested.

# AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = $-40^{\circ}$ to 85°C, $V_{DD} = 5 \text{ V} \pm 10\%$ )

## READ CYCLE

SYMBOL	PARAMETER	-8	35	-1	10	UNIT
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	85	-	100	-	
t <sub>ACC</sub>	Address Access Time	-	85	-	100	
t <sub>CO</sub>	Chip Enable Access Time	_	85	_	100	
t <sub>OE</sub>	Output Enable Access Time	-	45	-	50	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	_	5	-	ns
t <sub>OEE</sub>	Output Enable Low to Output Active	0	_	0	_	
t <sub>OD</sub>	Chip Enable Hige to Output High-Z	-	35	-	40	
t <sub>ODO</sub>	Output Enable Hige to Output High-Z	_	35	_	40	
t <sub>OH</sub>	Output Data Hold Time	10	_	10	_	

### WRITE CYCLE

		TC554001FI/FTI				
SYMBOL	PARAMETER	-8	35	-1	0	UNIT
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	85	_	100	_	
t <sub>WP</sub>	Write Pulse Width	55	_	60	_	
t <sub>CW</sub>	Chip Enable to End of Write	70	_	80	_	
t <sub>AS</sub>	Address Setup Time	0	_	0	-	
t <sub>WR</sub>	Write Recovery Time	0	_	0	-	ns
t <sub>ODW</sub>	R/W Low to Output High-Z	-	35	_	40	
t <sub>OEW</sub>	R/W High to Output Active	0	_	0	-	
t <sub>D\$</sub>	Data Setup Time	35	_	40	_	
t <sub>DH</sub>	Data Hold Time	0	_	0	_	

## AC TEST CONDITIONS

Output Load: 100 pF + one TTL gate

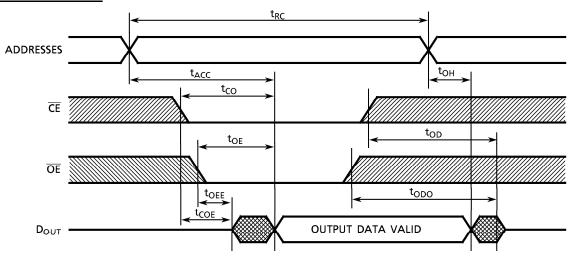
Input Pulse Level:  $0.4\,\mathrm{V},\ 2.6\,\mathrm{V}$ 

Timing Measurements: 1.5 V Reference Level: 1.5 V

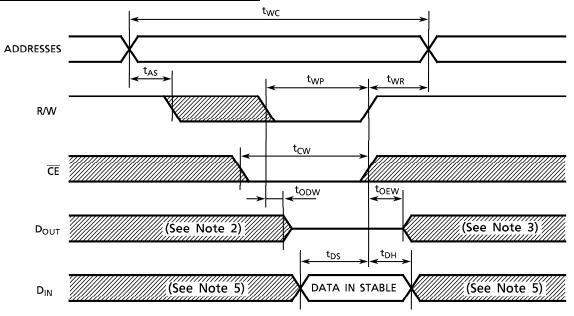
 $t_r$ ,  $t_F$ : 5 ns

### **TIMING WAVEFORMS**

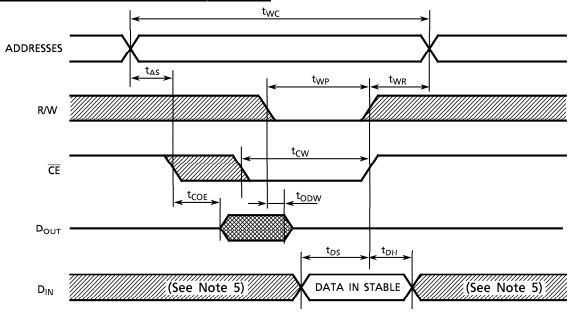
### READ CYCLE (See Note 1)



### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



### WRITE CYCLE 2 (CE CONTROLLED) (See Note 4)

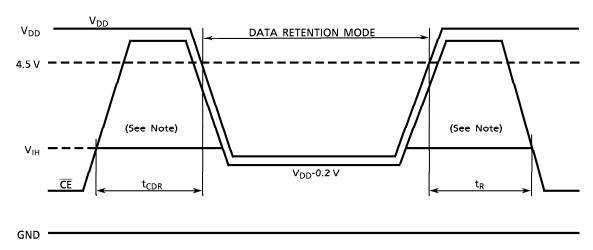


- (1) R/W remains High for Read Cycle.
- (2) If  $\overline{\text{CE}}$  goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If  $\overline{\text{CE}}$  goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF  $\overline{\text{CE}}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

## <u>DATA RETENTION CHARACTERISTICS</u> (Ta = $-40^{\circ}$ to $85^{\circ}$ C)

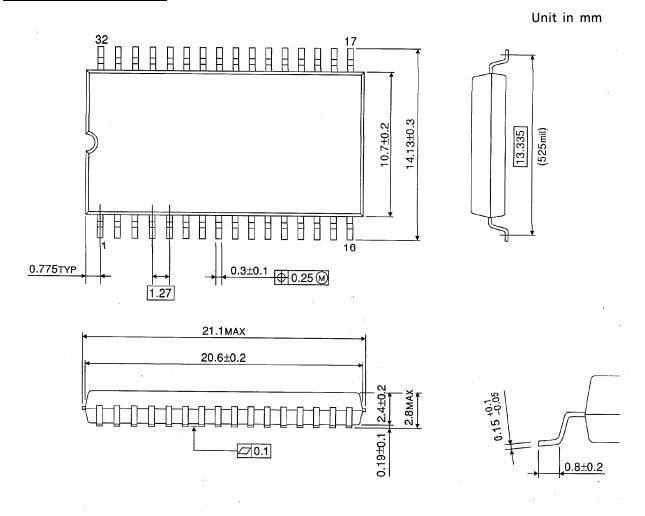
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	-	5.5	٧
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	-	-	100	μA
צטטי		V <sub>DH</sub> = 5.5 V	-	-	200	$\mu$ A
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode	Time	0	-	_	n\$
t <sub>R</sub>	Recovery Time		5	_	_	mS

### **CE** Controlled Data Retention Mode



Note: When  $\overline{CE}$  is operating at the  $V_{IH}$  level (2.4V), the standby current is given by  $I_{DDS1}$  during the transition of  $V_{DD}$  from 4.5 to 2.6V.

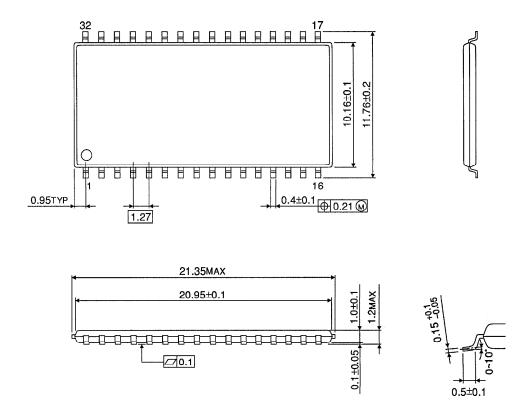
# PACKAGE DIMENSIONS (SOP32-P-525-1.27)



Weight: 1.14 g (typ)

# PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

Unit in mm



Weight: 0.51g (typ)